R&D of HV-CMOS detectors

HEP Annual Meeting, 18 May 2023

UNIVERSITY OF LIVERPOOL

Chenfan Zhang

on behalf of the HV-CMOS group

Liverpool HV-CMOS Group

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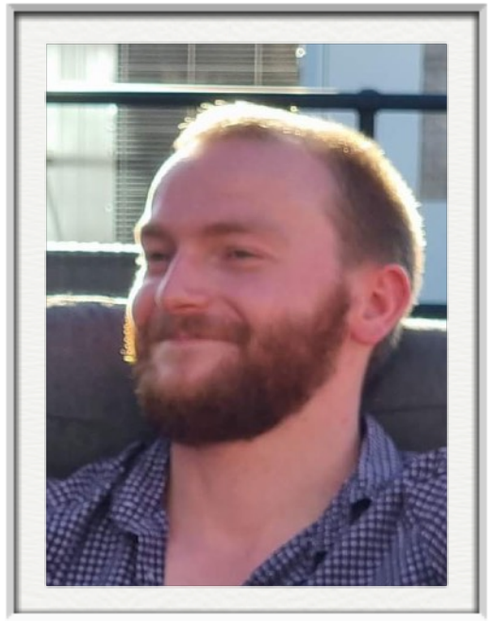
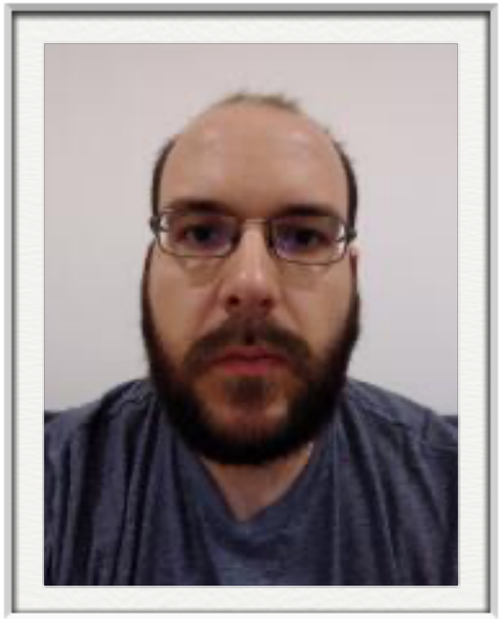


Ben

Chenfan

Eva



Jan

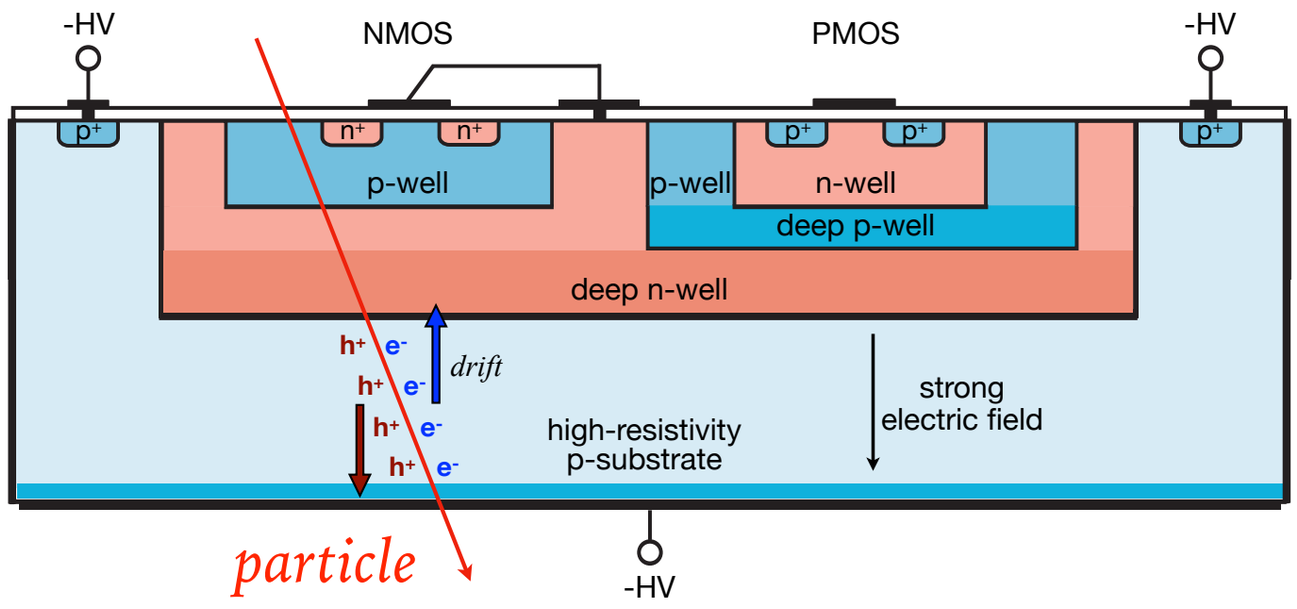
Sam

Sigrid

- Our group design advanced HV-CMOS detectors, make DAQ systems and evaluate them in lab and testbeam…

HV-CMOS: Monolithic Pixel Detectors

- Monolithic: Sensor and readout electronics in a single silicon wafer.
  - ➤ Single layer structure: **low material thickness** (50 μm);
  - ➤ No bump-bonding: **Small pixel size** ($< 50\ \mu\text{m} \times 50\ \mu\text{m}$); **reduced production cost** (~ £100k/m^2);
  - ➤ High bias voltage: **fast charge collection** by drift (~ 200 ps) and **high radiation tolerance** (5×10^{15} 1 MeV n_{eq}/cm^2).



- The Mu3e experiment has chosen HV-CMOS pixel detectors and many others are considering them: LHCb, proton EDM, PANDA. And applications fields other than HEP experiments.

Liverpool HV-CMOS development

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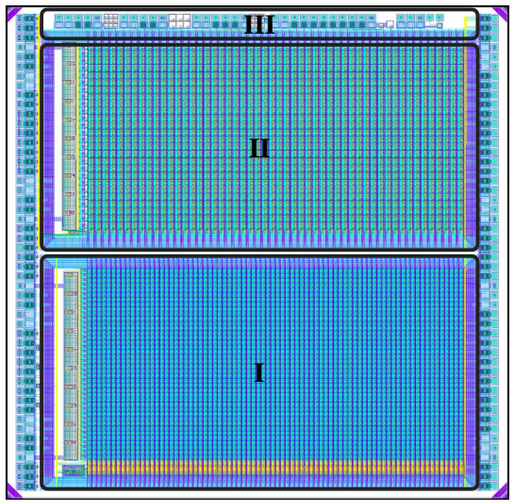
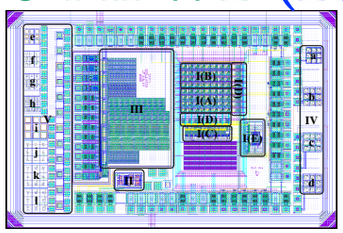
- Goals: improve radiation tolerance, time resolution and pixel granularity.

RD50 Series

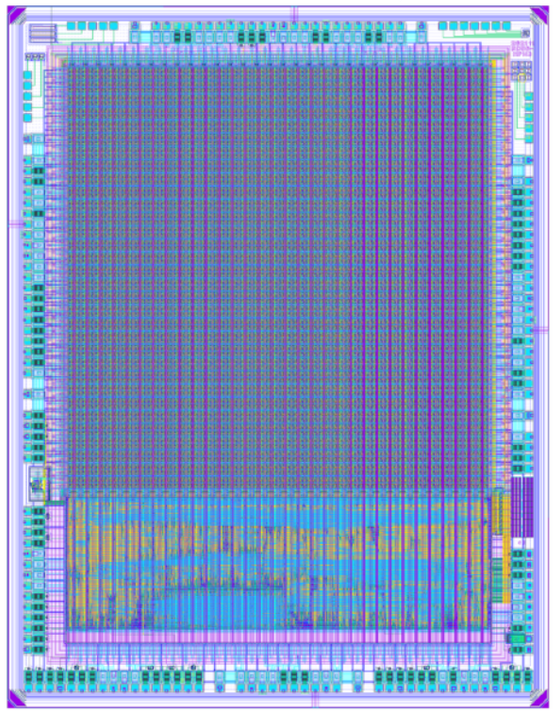
RD50-MPW1 (2018)



RD50-MPW2 (2020)

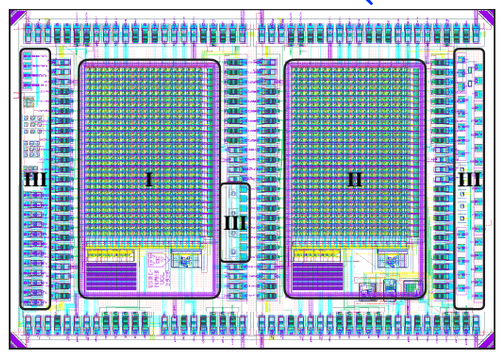


RD50-MPW3 (2022)



UKRI Series

UKRI-MPW0 (2021)



- RD50-MPW1: test the LF150 process, low V_{BD} (55 V) and high I_{Leak} ($\sim \mu$A).
- RD50-MPW2: high V_{BD} (130 V), low I_{Leak} ($\sim$ nA) and fast analog pixel.
- RD50-MPW3: implements large pixel matrices with advanced digital readout.
- UKRI-MPW0: first backside-only biased, high V_{BD} ($>$ 600 V).

Liverpool HV-CMOS development

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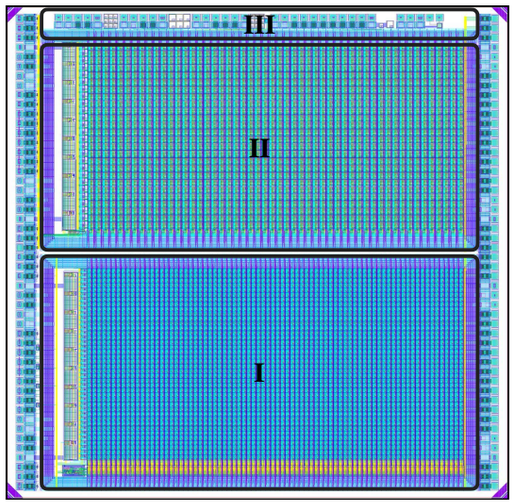
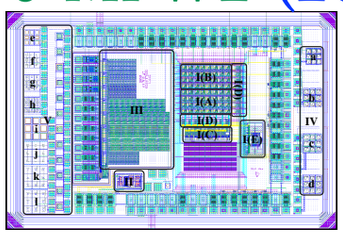
- Goals: improve radiation tolerance, time resolution and pixel granularity.

RD50 Series

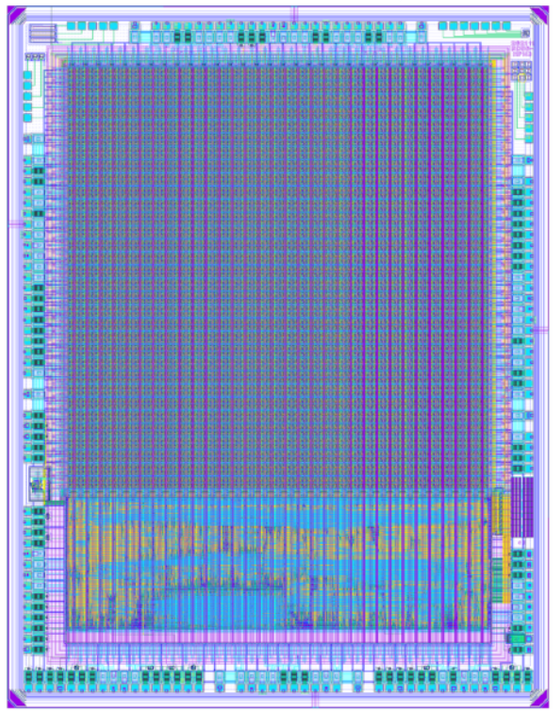
RD50-MPW1 (2018)



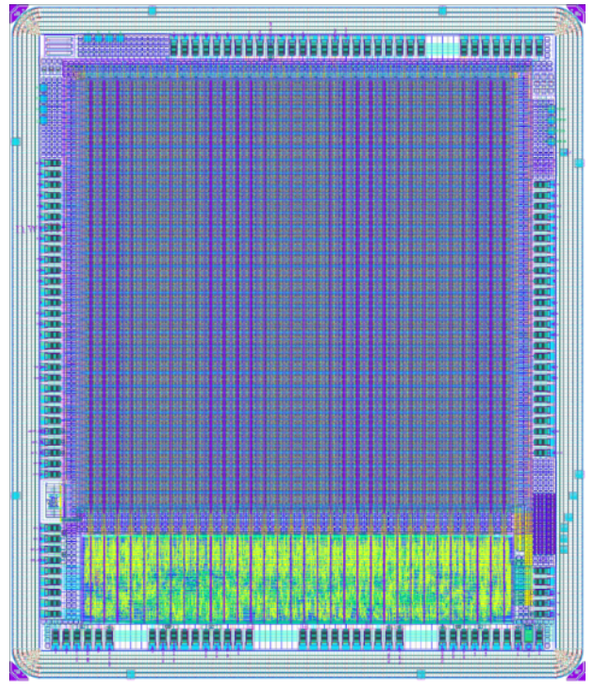
RD50-MPW2 (2020)



RD50-MPW3 (2022)

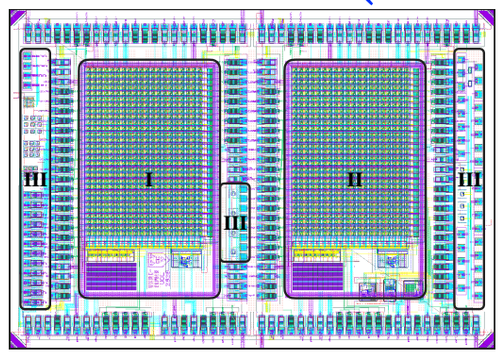


RD50-MPW4 (2023)

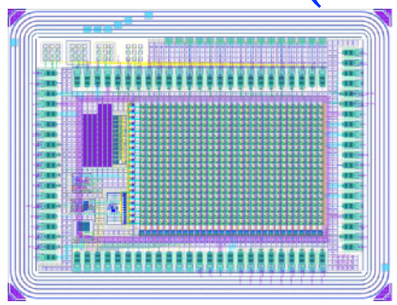


UKRI Series

UKRI-MPW0 (2021)



UKRI-MPW1 (2023)



submitted this week

- RD50-MPW1: test the LF150 process, low V_{BD} (55 V) and high I_{Leak} ($\sim \mu$A).
- RD50-MPW2: high V_{BD} (130 V), low I_{Leak} ($\sim$ nA) and fast analog pixel.
- RD50-MPW3: implements large pixel matrices with advanced digital readout.
- UKRI-MPW0: first backside-only biased, high V_{BD} (> 600 V).
- **RD50-MPW4** and **UKRI-MPW1:** fix the issues found in their predecessors.

Measurement of RD50-MPW3

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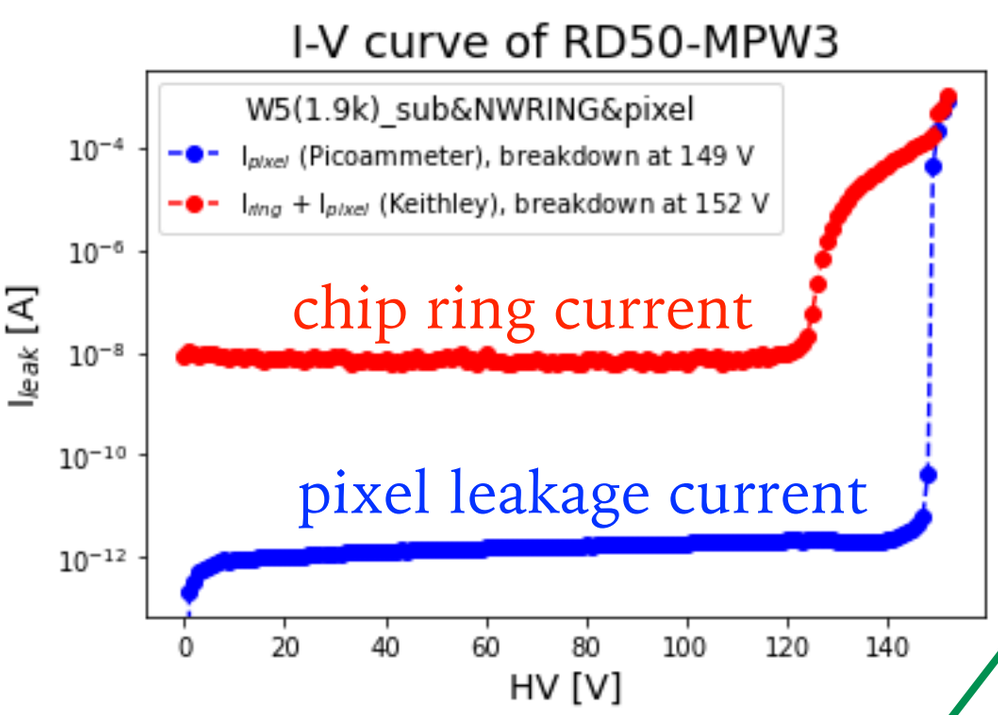
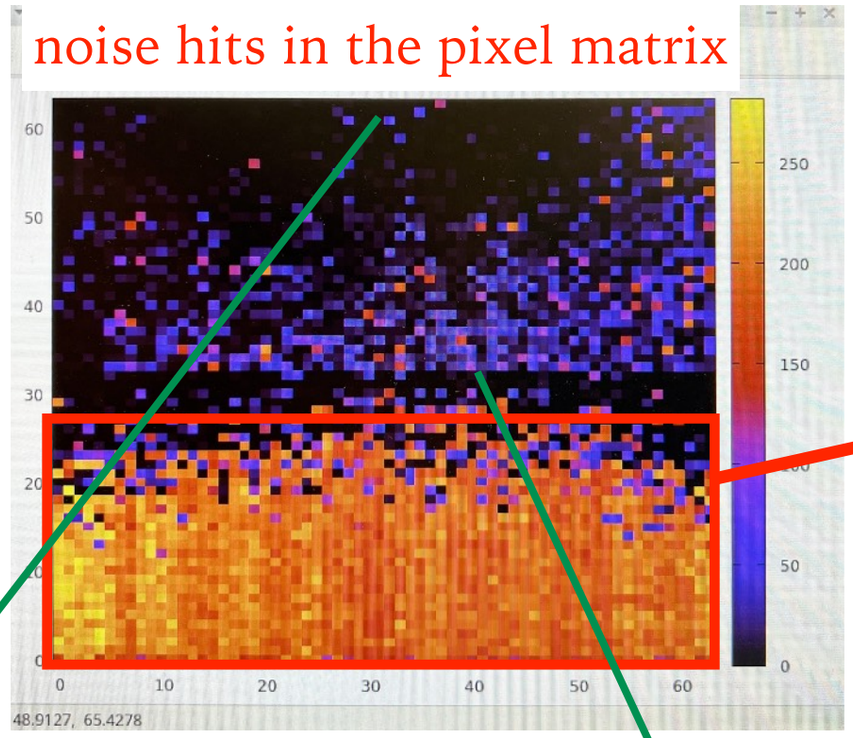
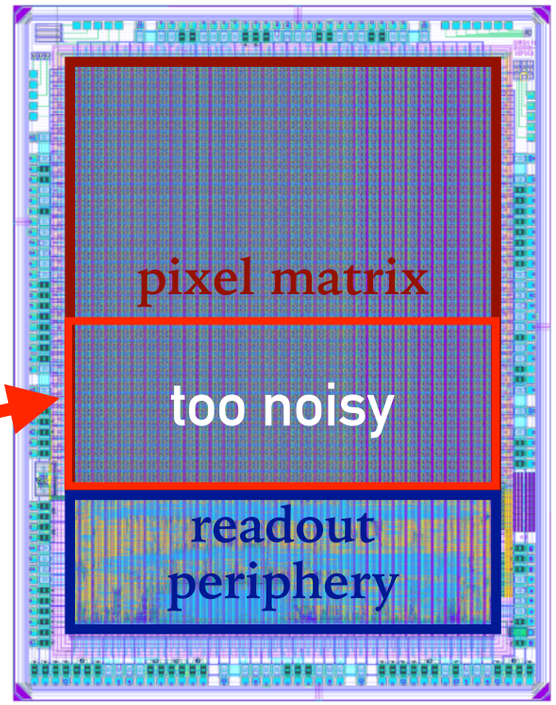
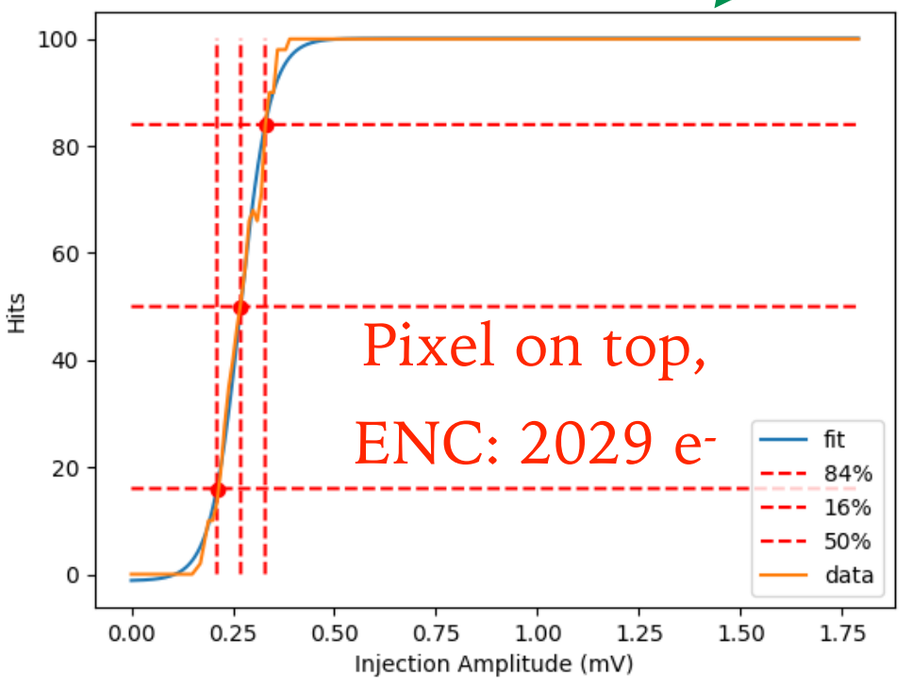
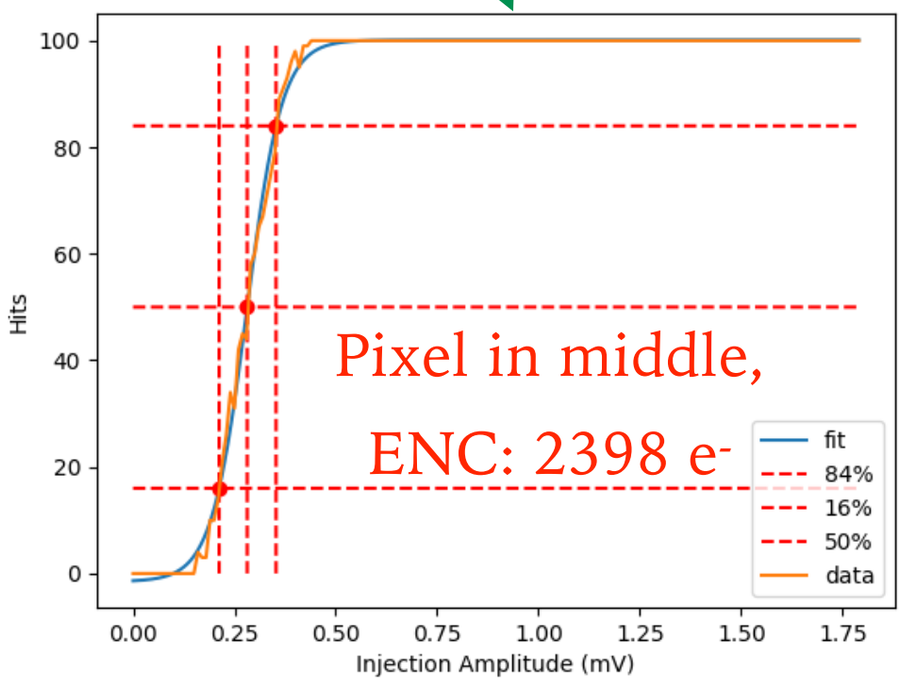
- IV measurements show its breakdown and leakage are similar to RD50-MPW2.







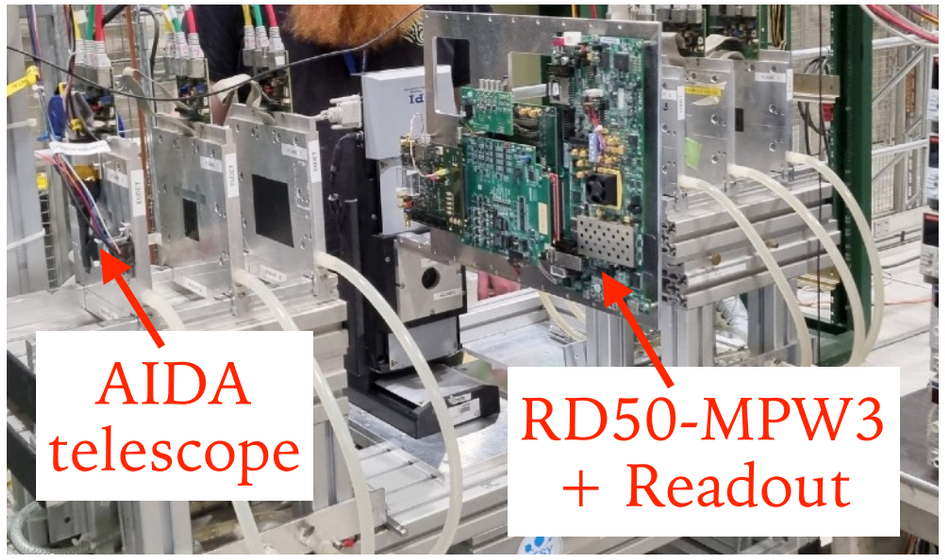


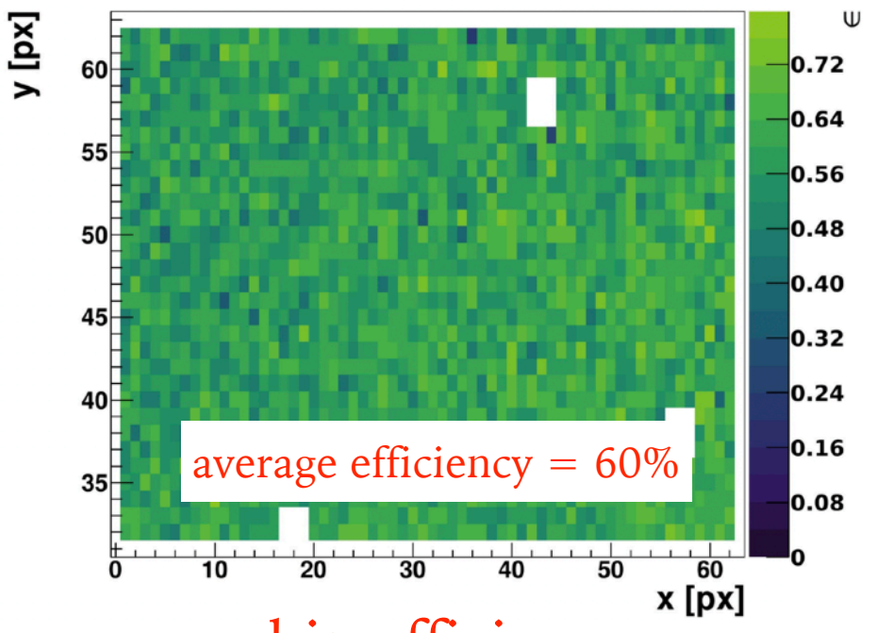


RD50-MPW2
ENC: 150 e-

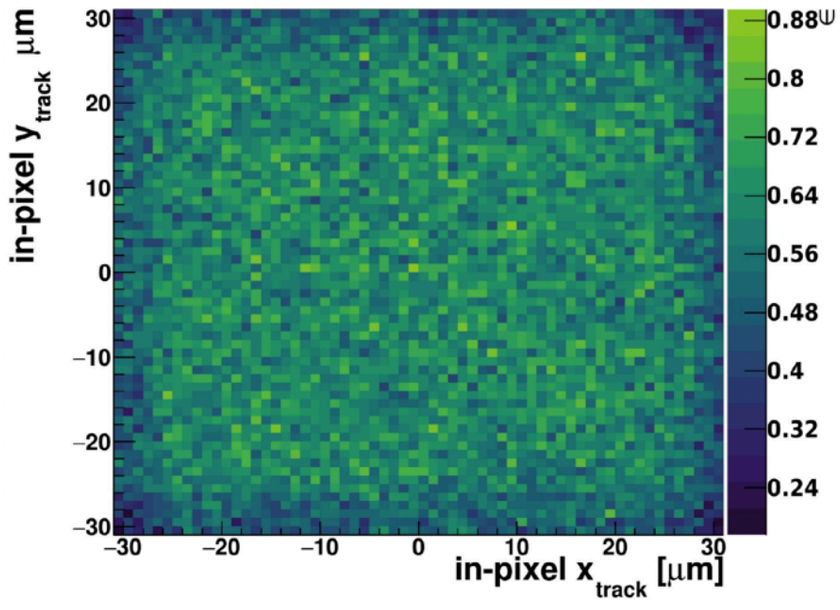
Measurement of RD50-MPW3

- Beamtest at CERN SPS in October 2022. First beamtest by RD50 to evaluate HV-CMOS detector and readout DAQ designed by RD50. (HUGE amount of work!)
- high threshold used due to the high noise -> low efficiency.





chip efficiency

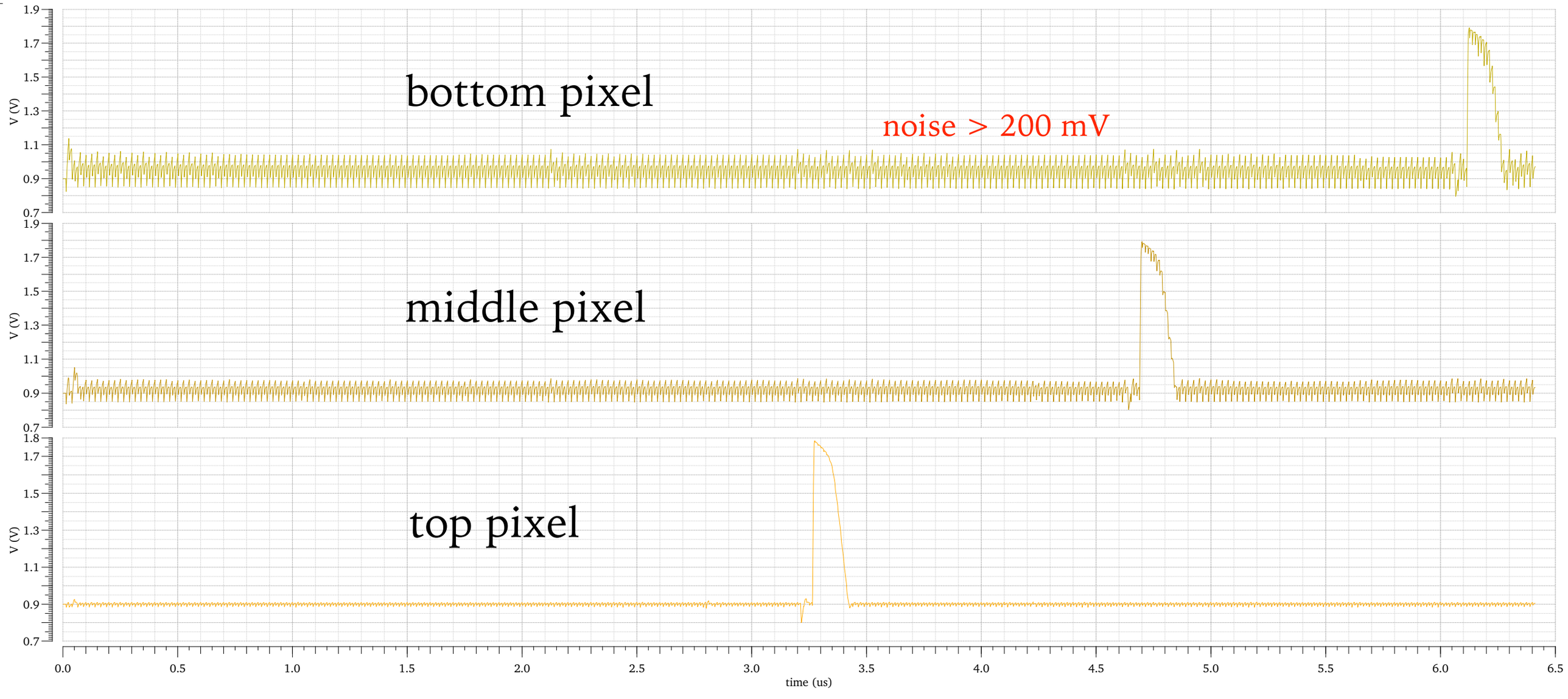


in-pixel efficiency

Noise simulation

- Suspect the noise is from the digital readout periphery. Try to simulate the noise.

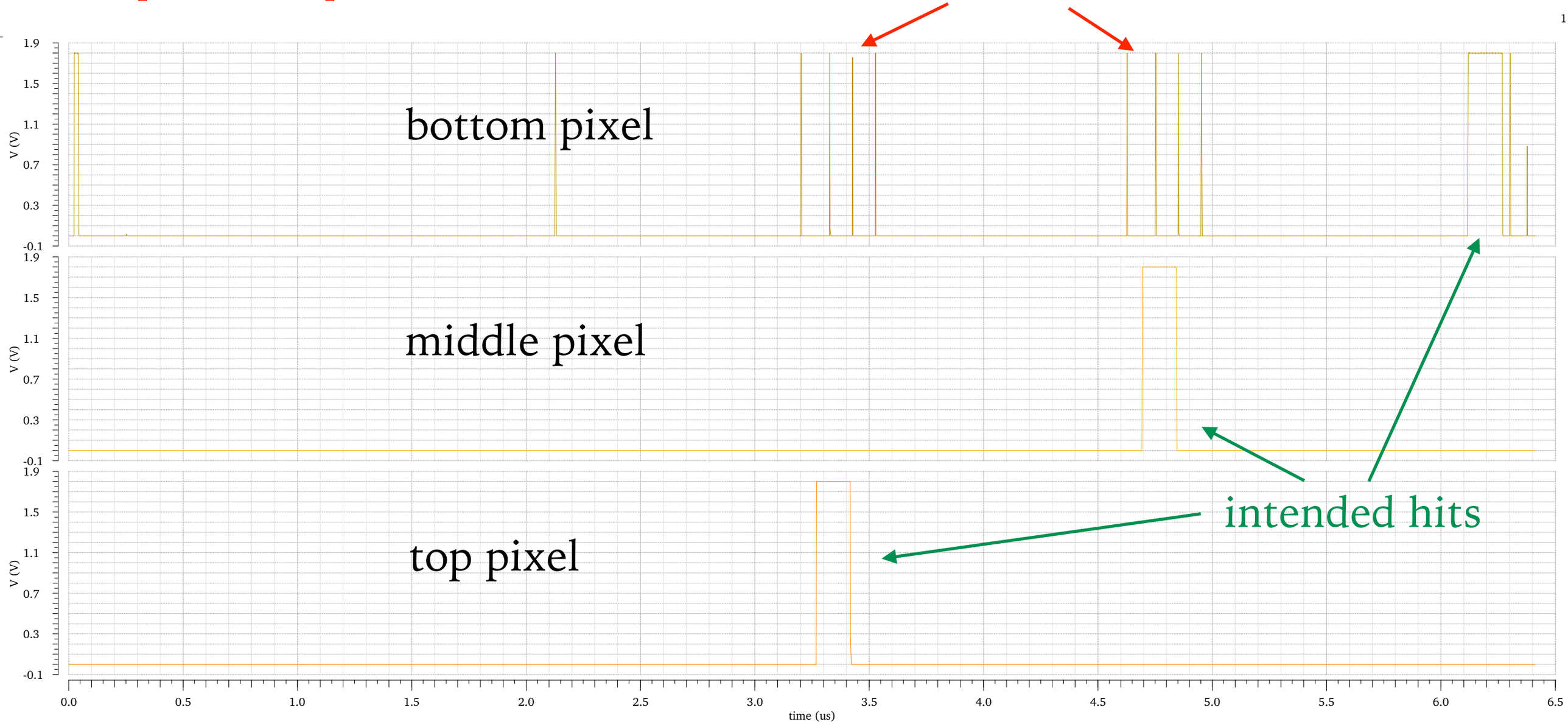
amplifier output:



Noise simulation

- Suspect the noise is from the digital readout periphery. Try to simulate the noise.

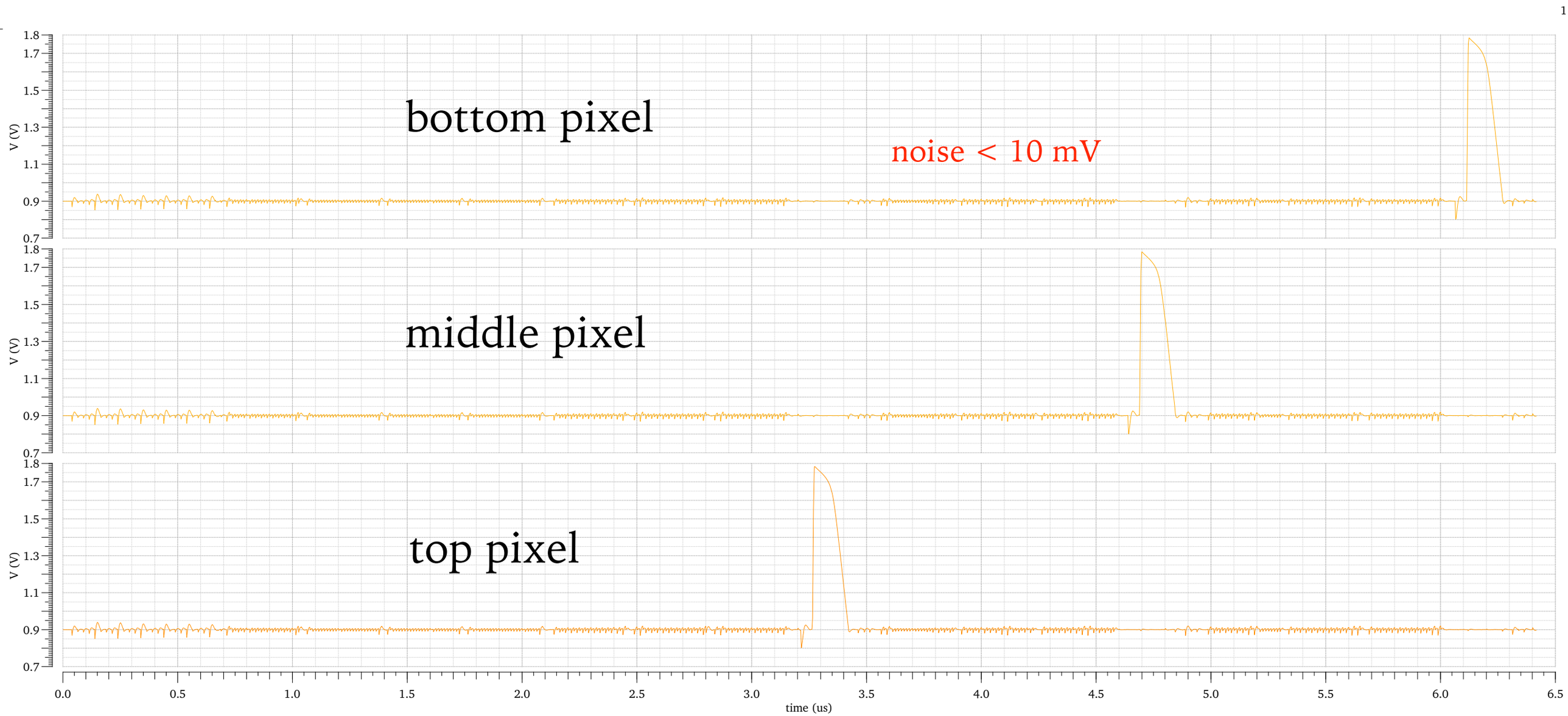
comparator output:



Noise simulation

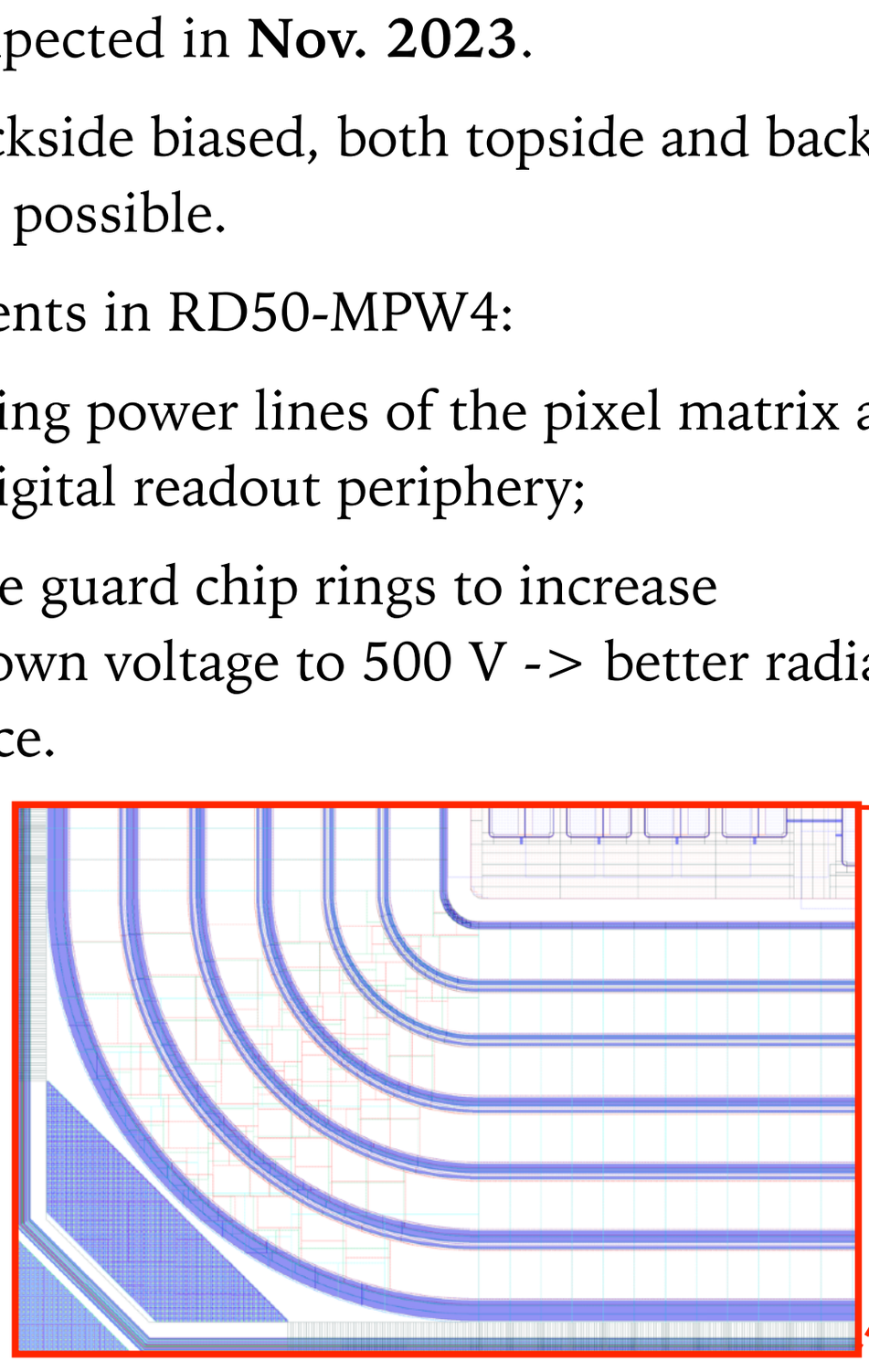
- Noise reduced after separating the power lines of pixel matrix and digital periphery.

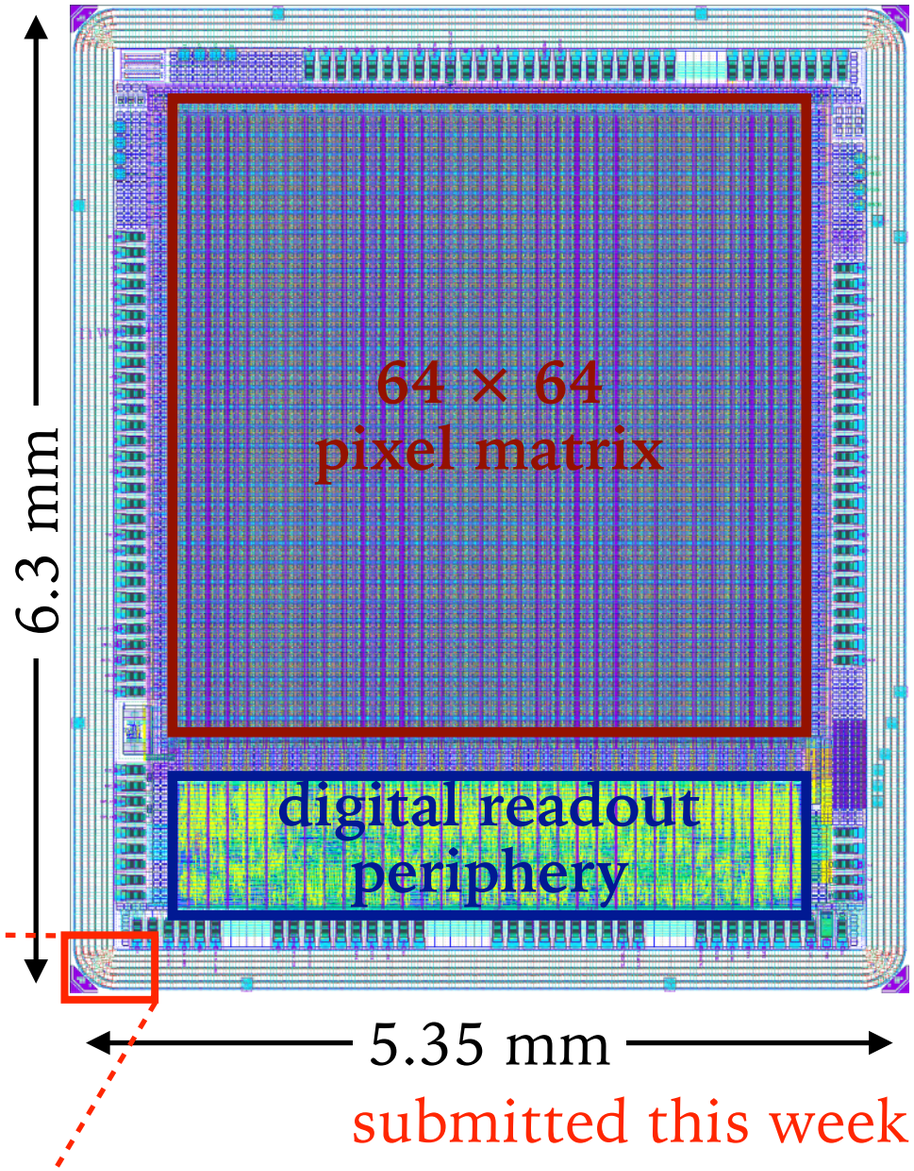
after separating power lines:



Design of RD50-MPW4

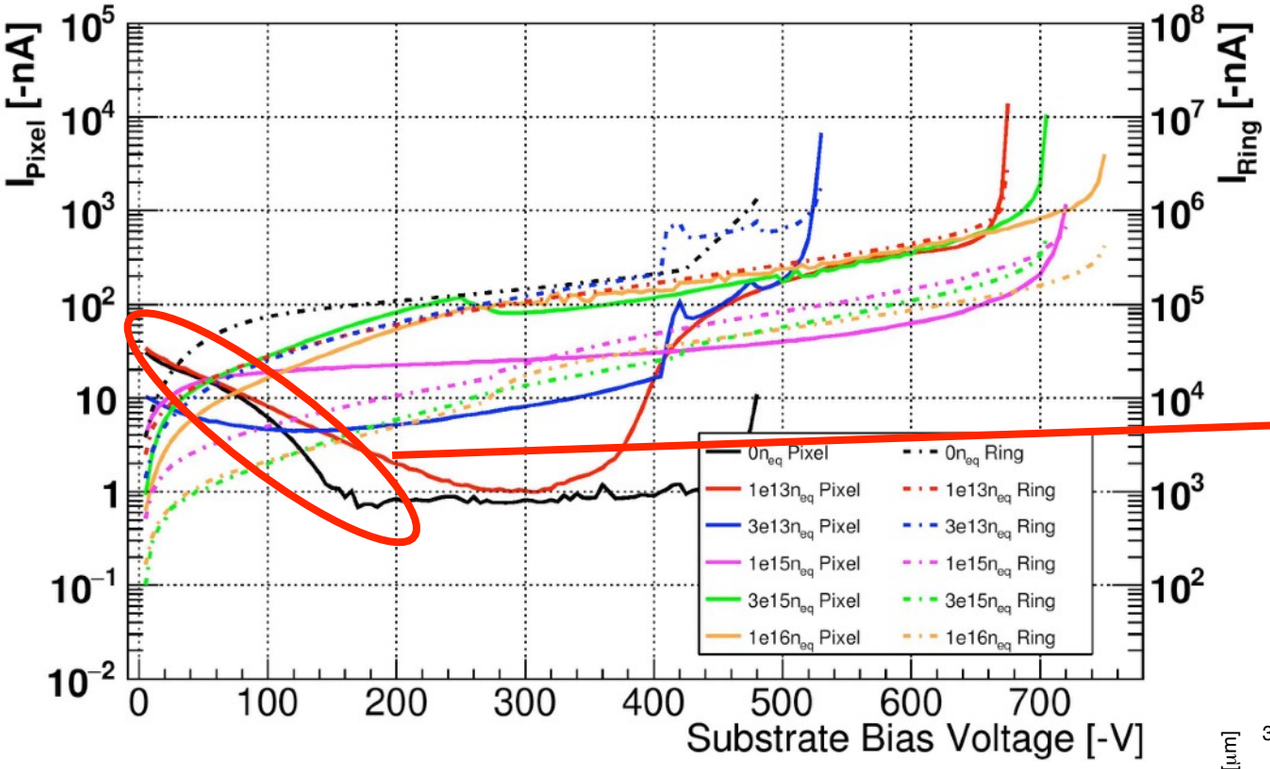
- **RD50-MPW4** submitted on Monday this week, delivery expected in **Nov. 2023**.
- Will be backside biased, both topside and backside biasing are possible.
- Improvements in RD50-MPW4:
  - ➤ separating power lines of the pixel matrix and noisy digital readout periphery;
  - ➤ multiple guard chip rings to increase breakdown voltage to 500 V -> better radiation tolerance.

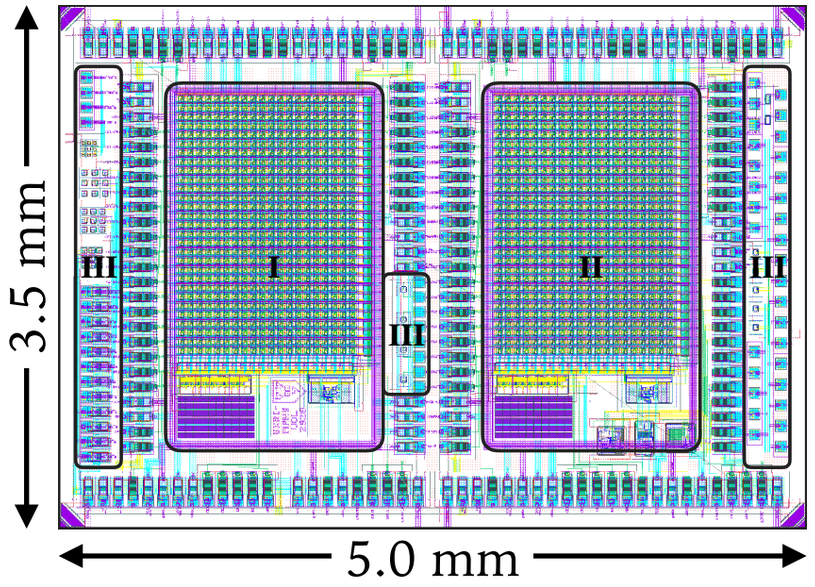


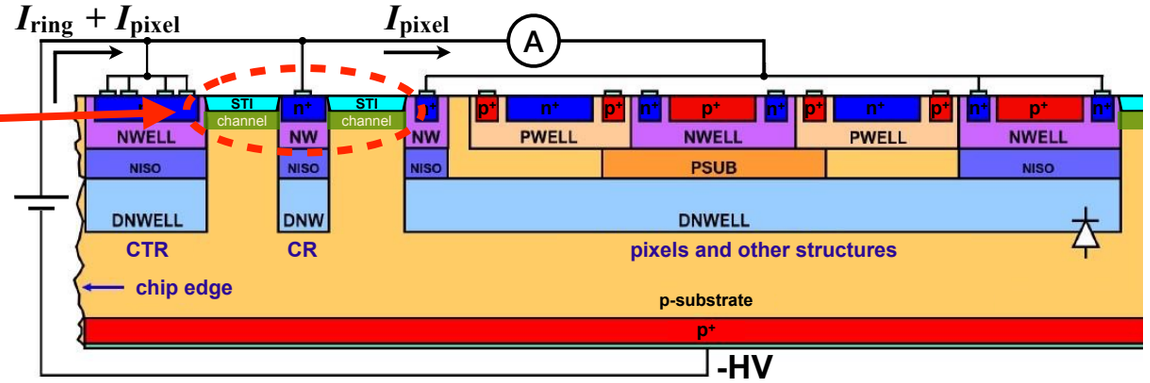


Measurement of UKRI-MPW0

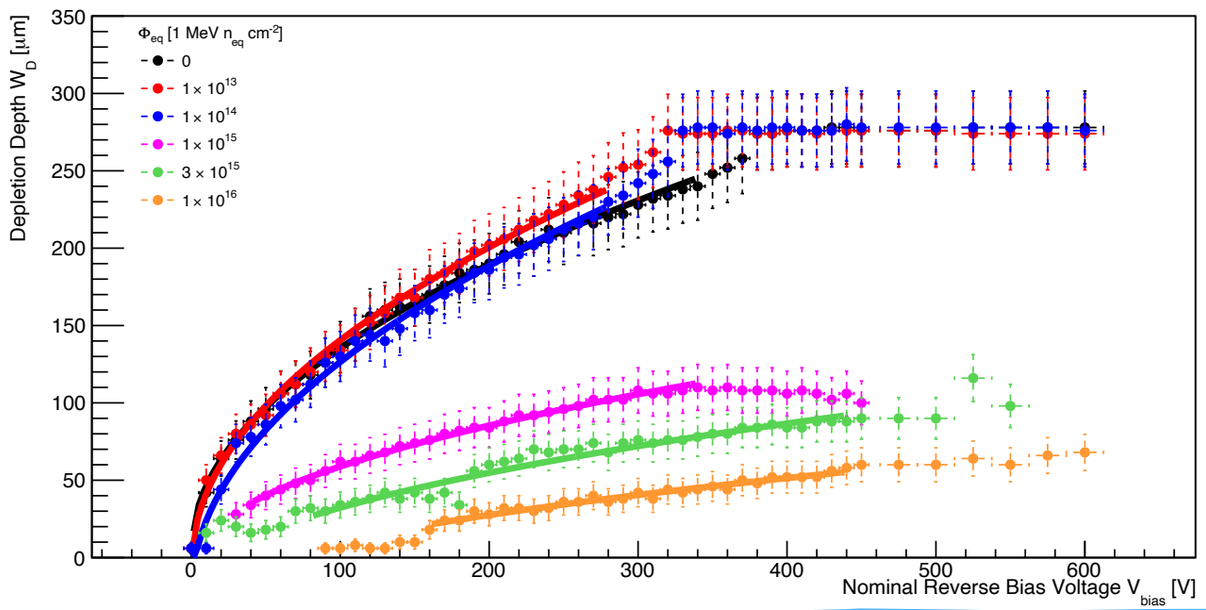
- V_{BD} > 600 V, the 'U' shape pixel leakage current I_{pixel} is due to the parasitic channel beneath STI.
- High ring current I_{ring} (~mA) is caused by edge defects.





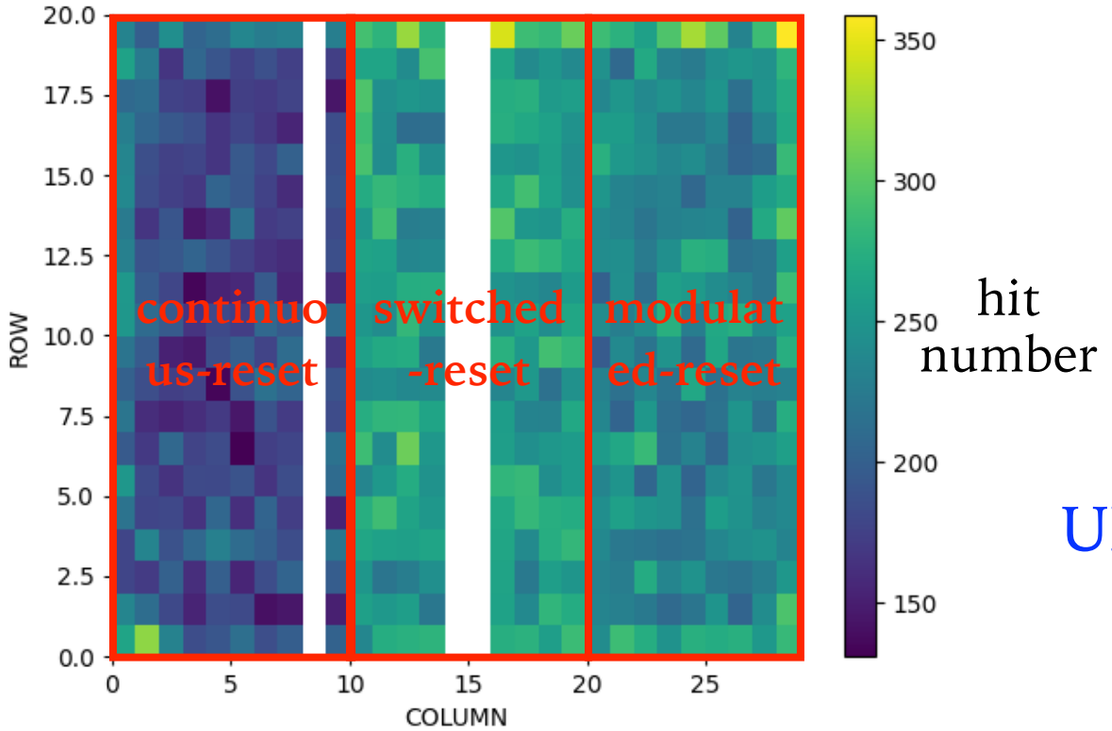


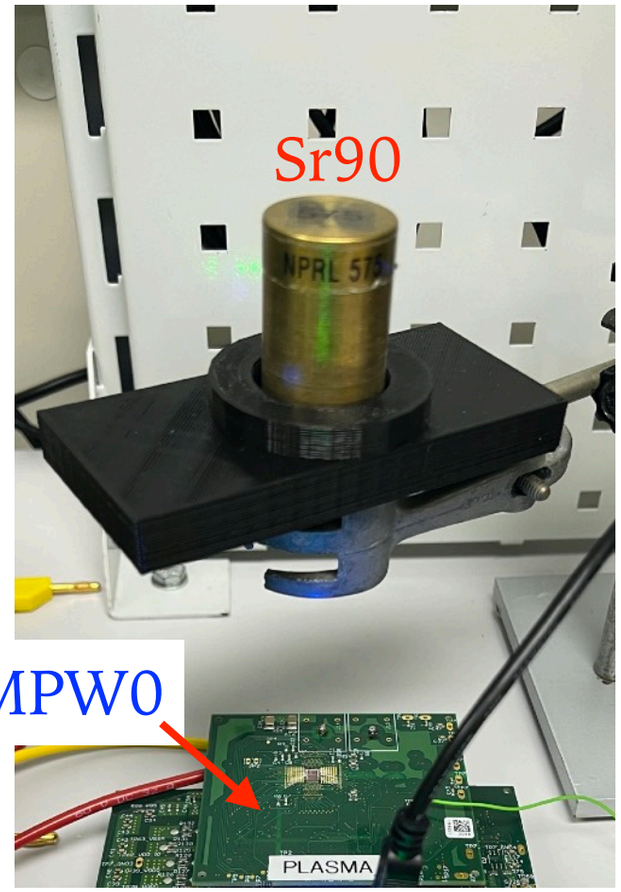
- edge-TCT shows the chip is fully depleted with bias voltage > 300 V and a 50 μm depletion width is maintained after irradiated to a radiation fluence of 1×10^{16} n_{eq}/cm^2.

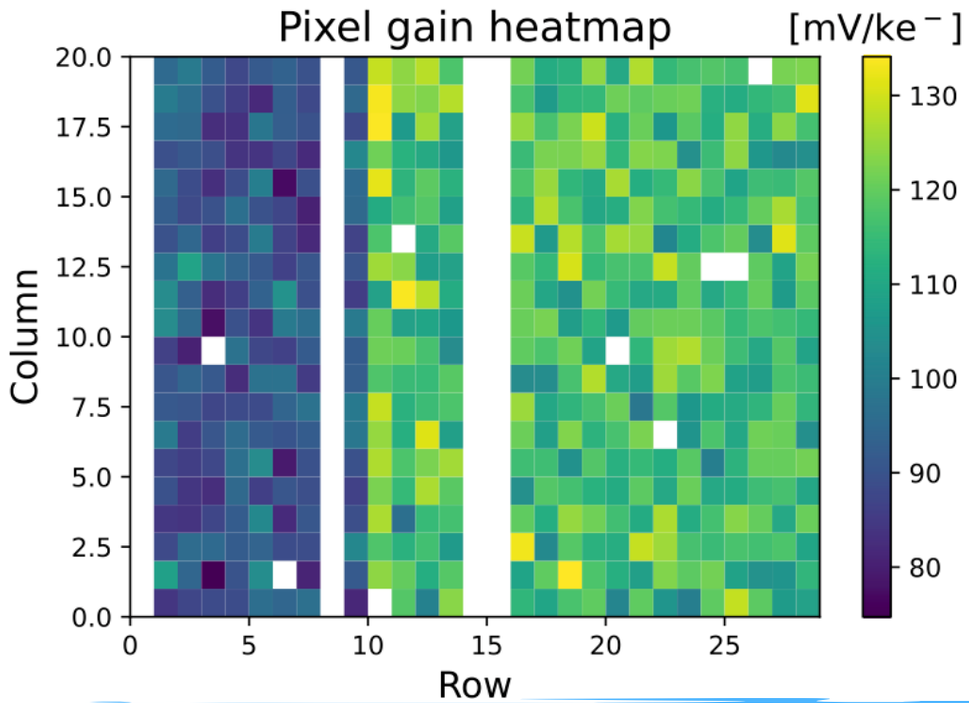


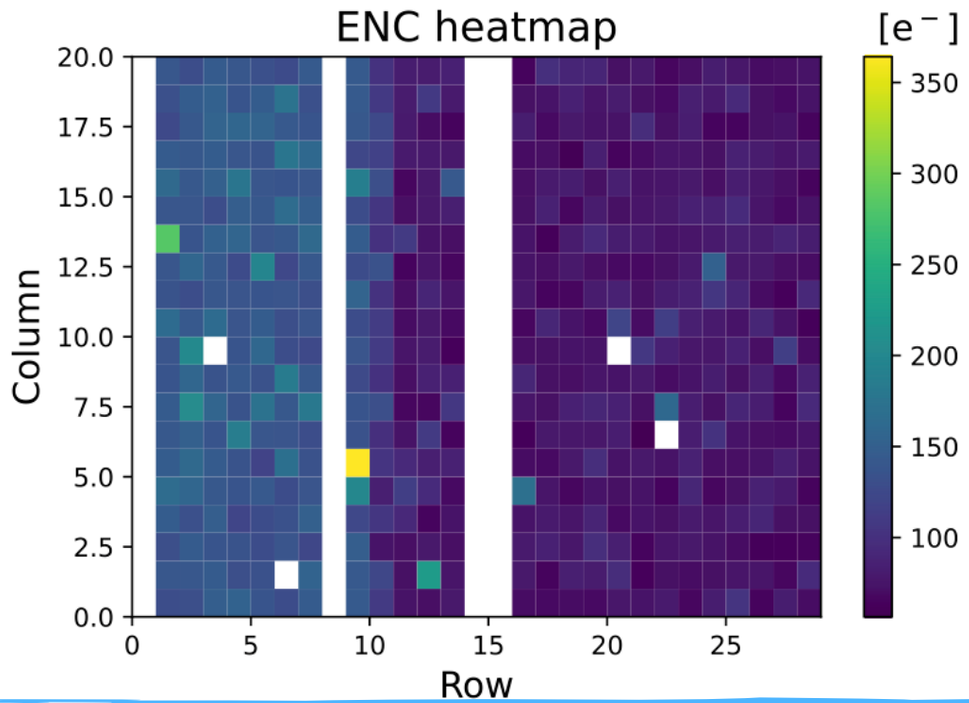
UKRI-MPW0 Pixel Matrix

- Used a Sr90 source to plot the number of hits received by every pixel over a shutter window of 20 s.



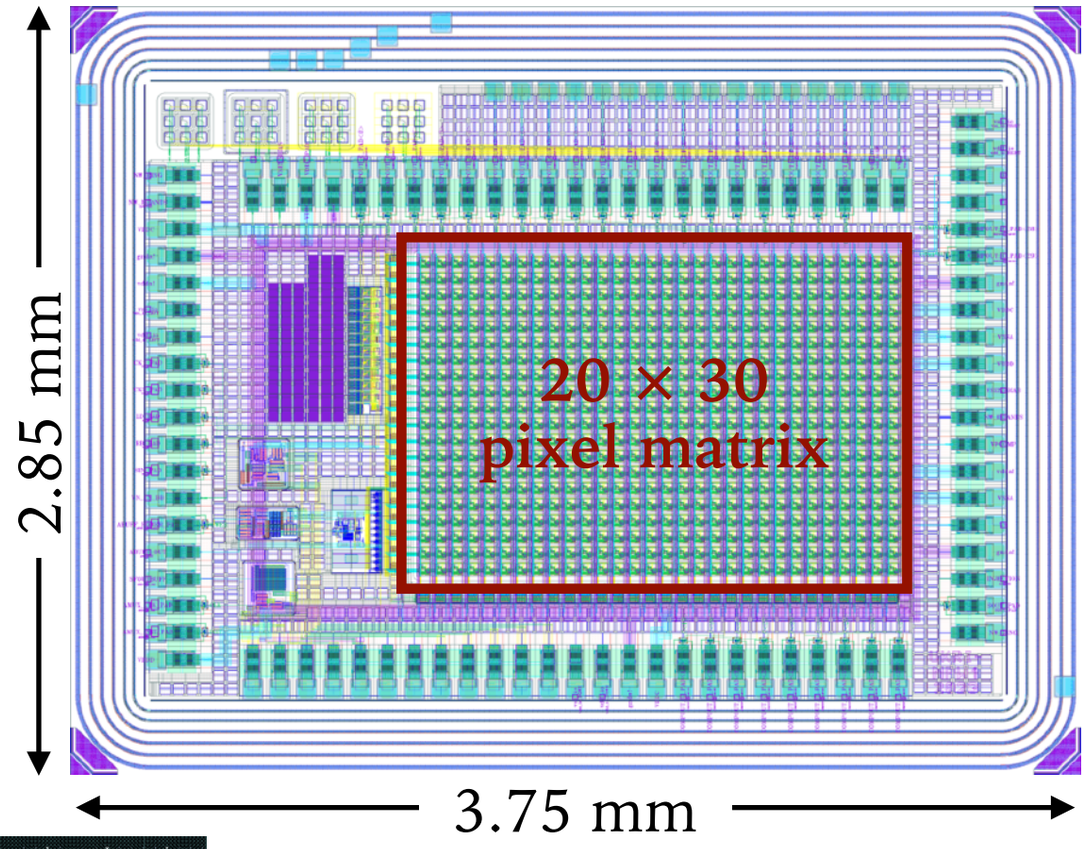




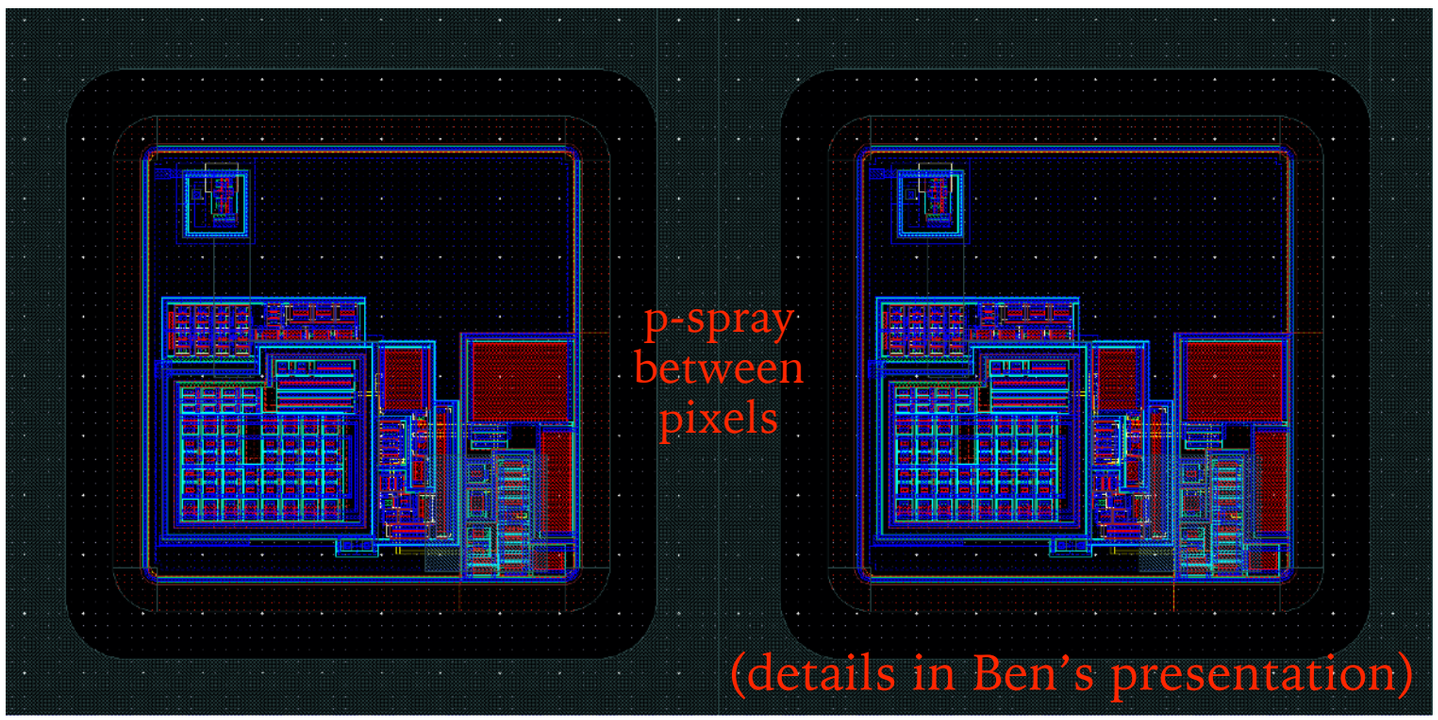


Design of UKRI-MPW1

- **UKRI-MPW1** submitted this week, delivery expected in **Nov. 2023**.
- Will be backside biased.
- Improvements in UKRI-MPW1:
  - ➤ add p-spray layer between pixels to avoid parasitic channel;
  - ➤ use multiple guard chip rings (same as RD50-MPW4) to decrease leakage current.



submitted this week

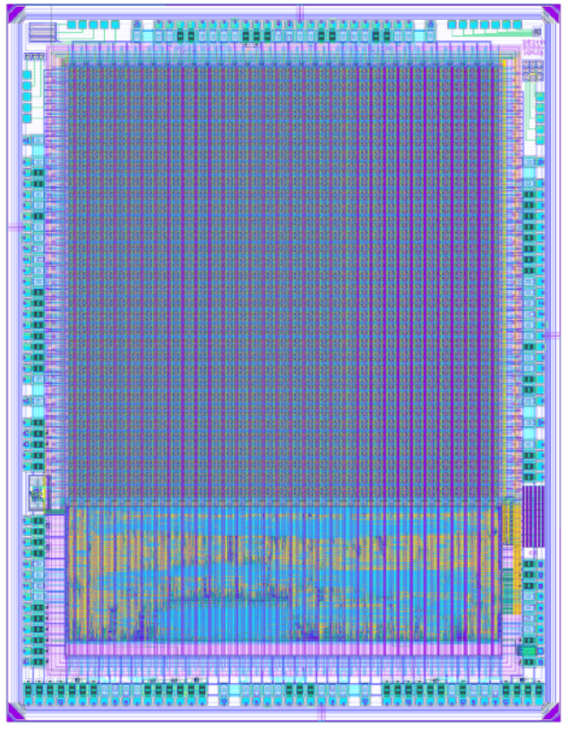


Summary and Next step

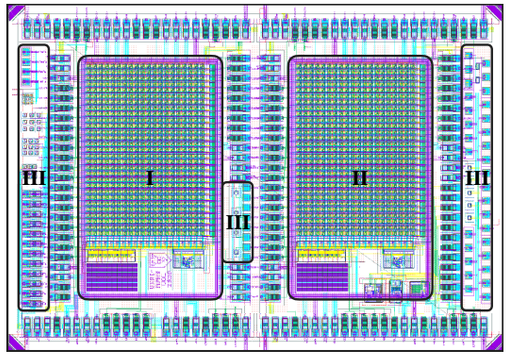
- Found high noise in RD50-MPW3 and high leakage current in UKRI-MPW0.
- Improvements implemented in RD50-MPW4 and UKRI-MPW1.
- Will do a beamtest on irradiated RD50-MPW3 samples in July at DESY. Will potentially test UKRI-MPW0 as well.
- Will design the DAQs for RD50-MPW4 and UKRI-MPW1 before their arrival.

submitted this week

RD50-MPW3
successful beam test



UKRI-MPW0
in-lab measurement



RD50-MPW4 **UKRI-MPW1**
to be received in Nov. 2023