



Darkside-20k



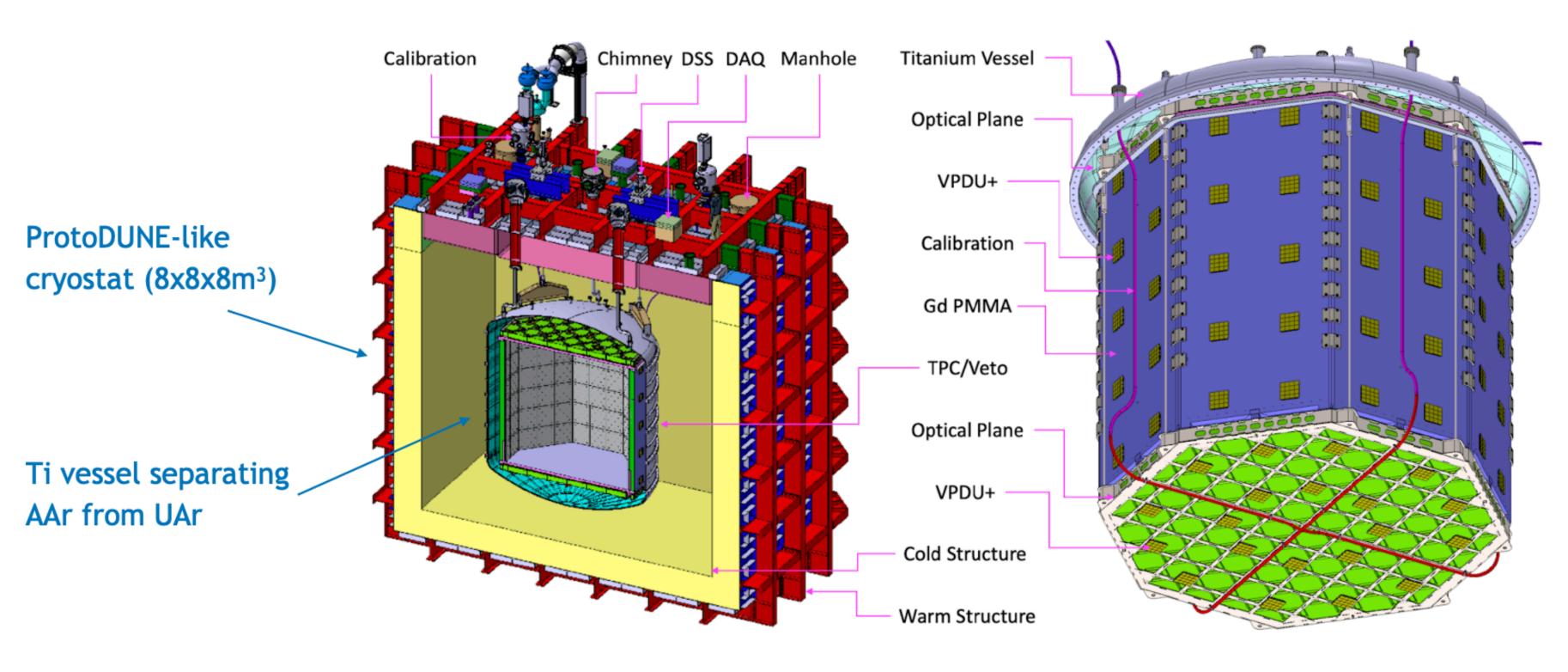


Outline

- Experiment overview
- People
- Production plan and part flow
- vTile assembly
- Cold testing
- Summary and Future



The Darkside-20k experiment



20m² of silicon fabricated by LFoundry in partnership with FBK, Trento.

Experiment at LNGS and cryostat operated at 87K

TPC

- 50 ton of underground LAr
- Gd-loaded acrylic (PMMA) walls to capture neutrons
- Walls coated with TPB as WL shifter
- 2112 channels, each grouping 96 SiPMs

Inner Veto

- 35 ton of underground LAr (single-phase)
- 480 channels, each grouping 96 SiPMs

Outer Veto

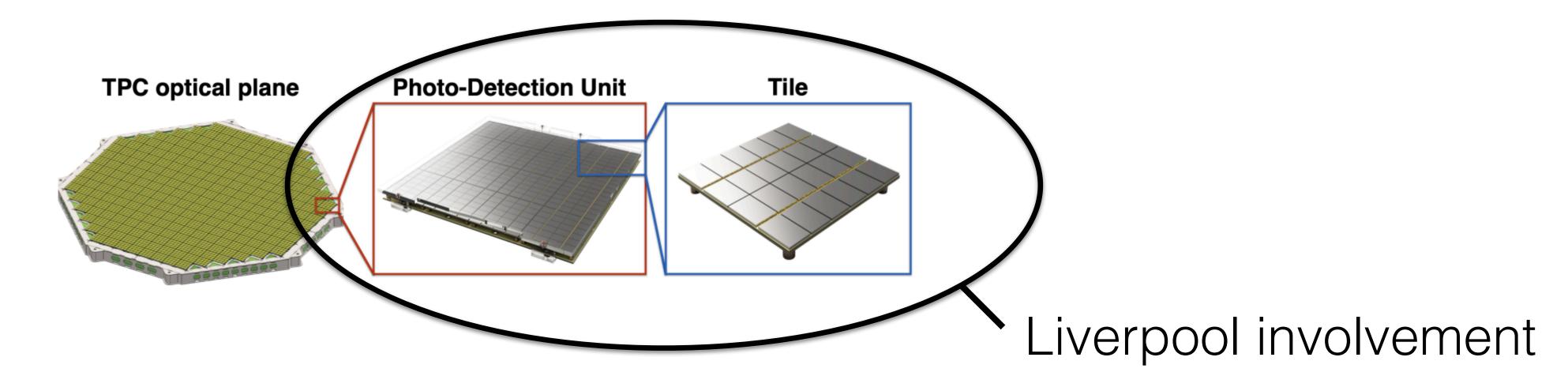
- 700 ton of atmospheric LAr (single-phase)
- 32 channels, each grouping 384 SiPM (PRELIMINARY)



Darkside-20k in Liverpool

- Research staff/academics: Joost Vossebeld, Kostas Mavrokoridis, Tim Jones,
 Gianluigi Casse, Adam Roberts, Alan Taylor, Jon Taylor
- Technical staff: Liam Boynton, Paul Sinclair, Dan Hollywood, T. Lee, P. Timko
- PhD students: Sudikshan Ravinthiran, Alan Taylor

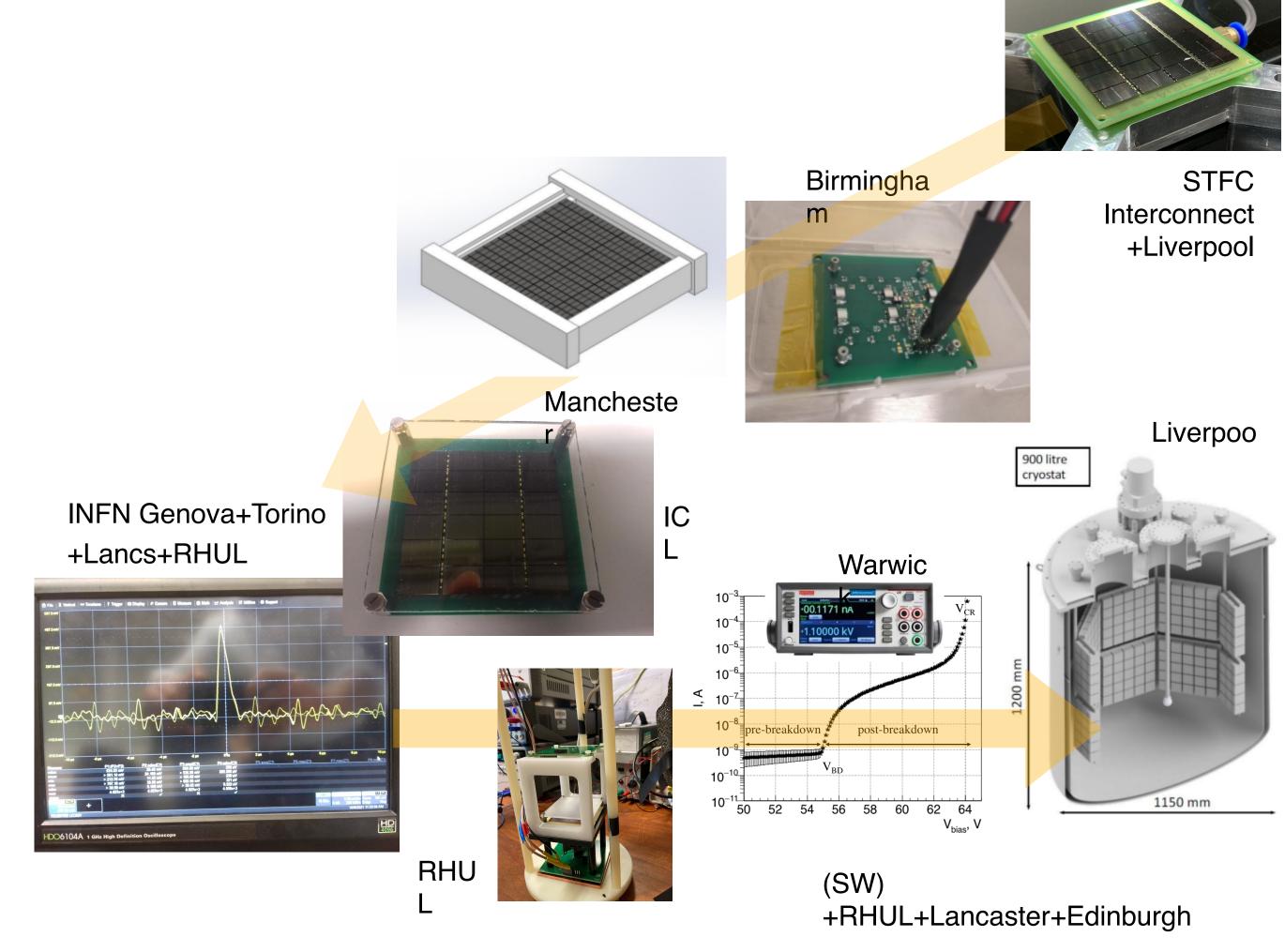
Thanks to Alan and Adam for a lot of the technical work shown in these slides





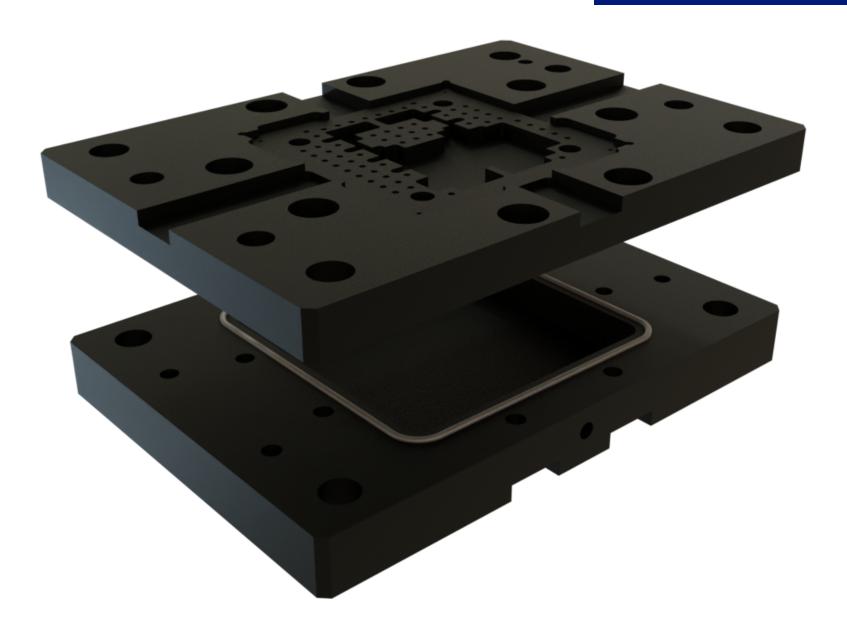
UK veto tile production flow

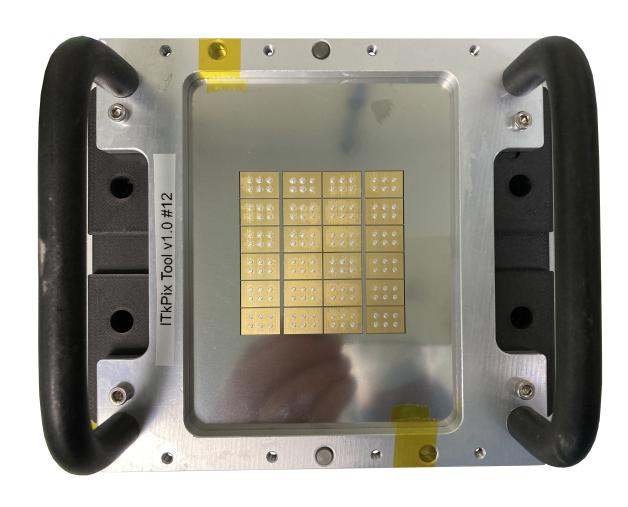
Object	Location	Activity
ASIC	IMEC	production
ASIC	Alter Technologies	packaging
ASIC	Birmingham	Test, prior to assembly
SiPM	NOA	cryoprobe test
vPCB	Stevenage Circuits, Ltd	production
vPCB	Liverpool, possibly Stevanage (under investigation)	QR code engraving
vPCB	Birmingham	assembly and test
vTile	STFC/LSDC	Assembly and test
vTile	RHUL	cold test, single tiles
vMotherboard	INFN	production
vPDU	Manchester	assembly and warm test
vPDU	Liverpool/Naples	cold test, PDU

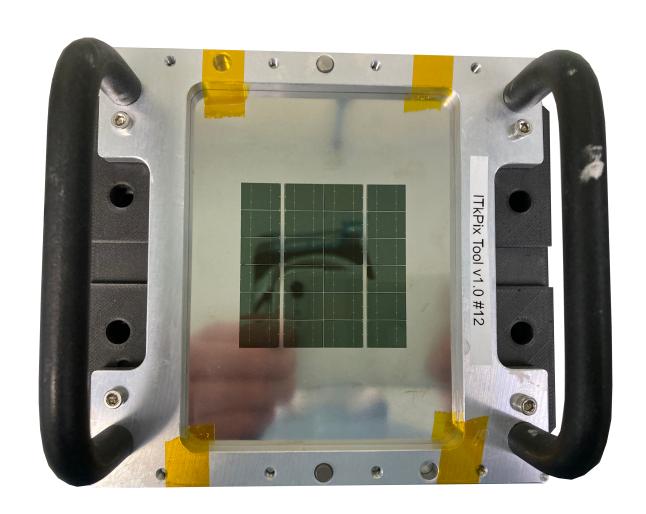




vTile assembly





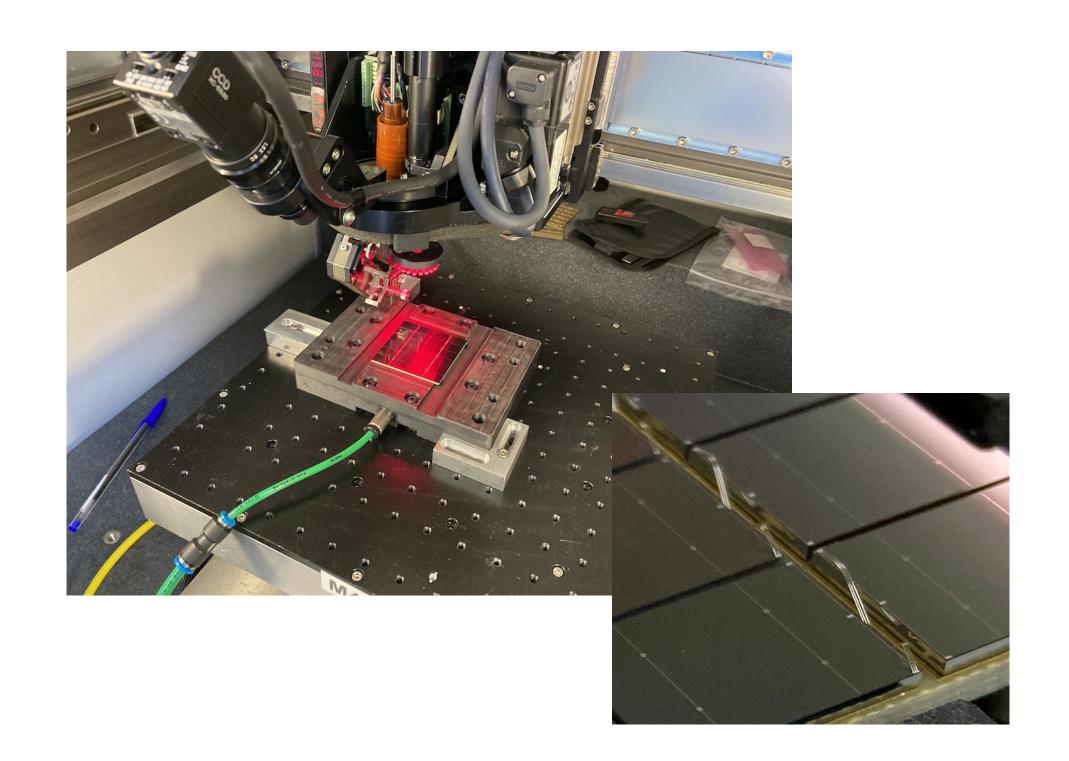


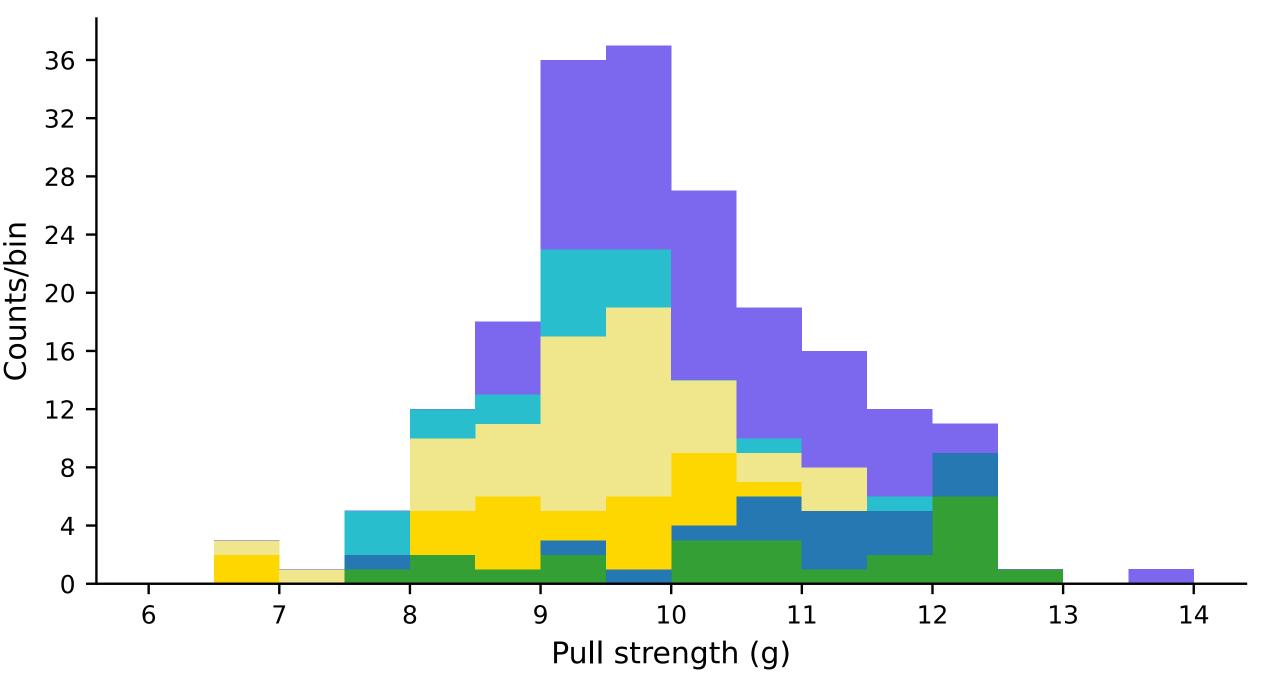
- Custom vacuum tooling 3D printed in AML and machined flat in DFF
- Solder stencils used for deposition of indium solder paste and placement of SiPM dies onto PCB
- After reflow in a dedicated oven, the tile is ready for metrology and wire bonding
- Handling brackets designed and printed for visual inspection and testing



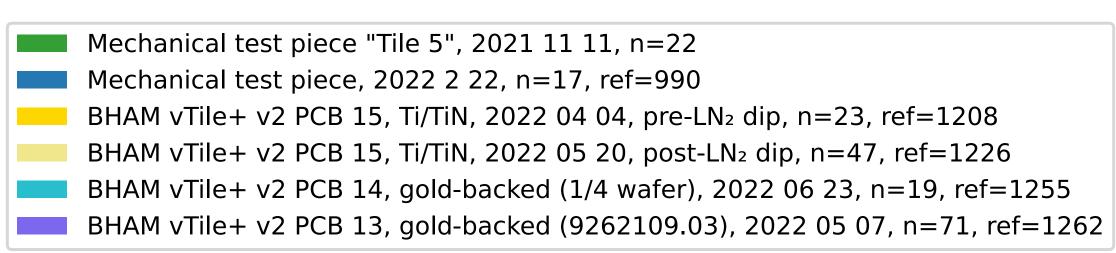


Tile assembly - wire bonding





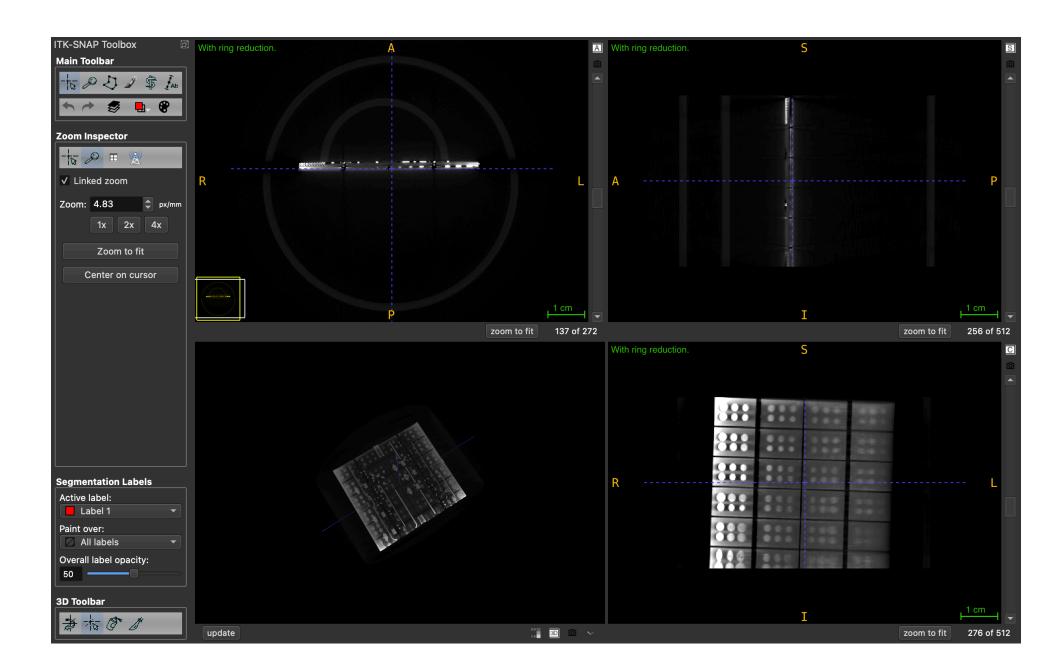
- Wire bonds from SiPM pad to PCB pad
- pull tests show excellent results and pad lifts have not yet been observed

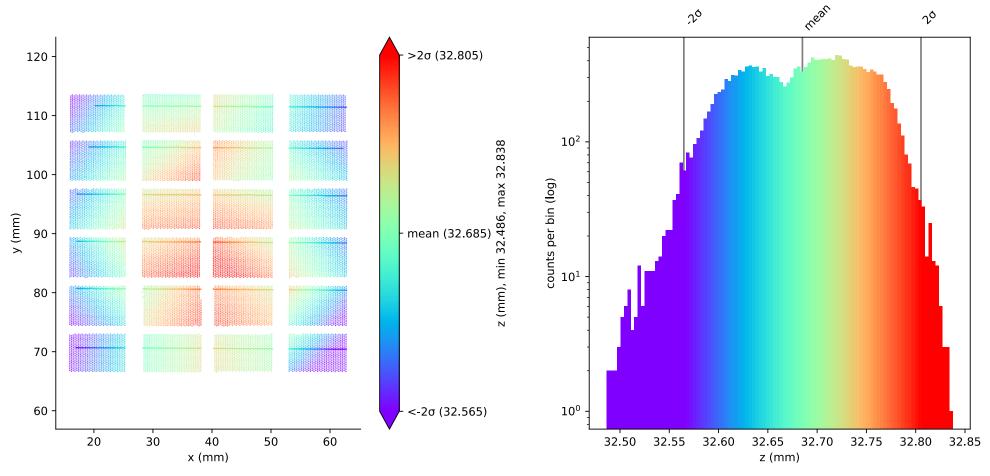




Tile assembly - QC

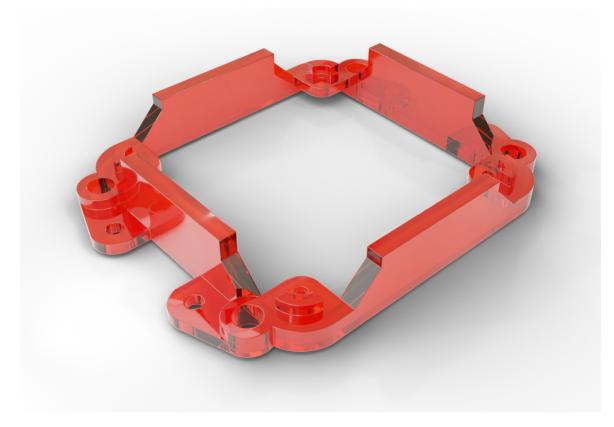
- Visual inspection of assembled vTiles carried out on a high resolution flat bed scanner
- Metrology carried out using the laser measurement attached to the smartscope in the LSDC
- CT scans being investigated for QC of the indium solder distributions between the silicon and the PCB
- Itk-snap software for viewing CT scan data

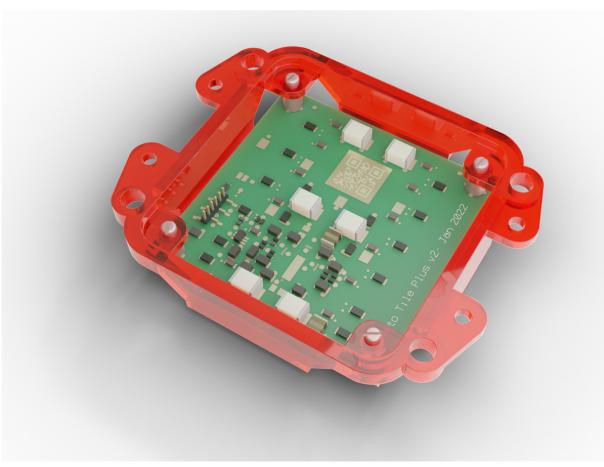


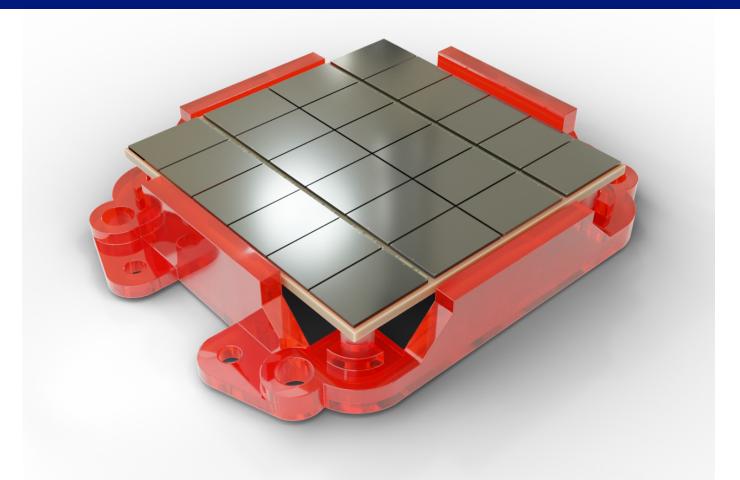




Tile assembly - handling and storage







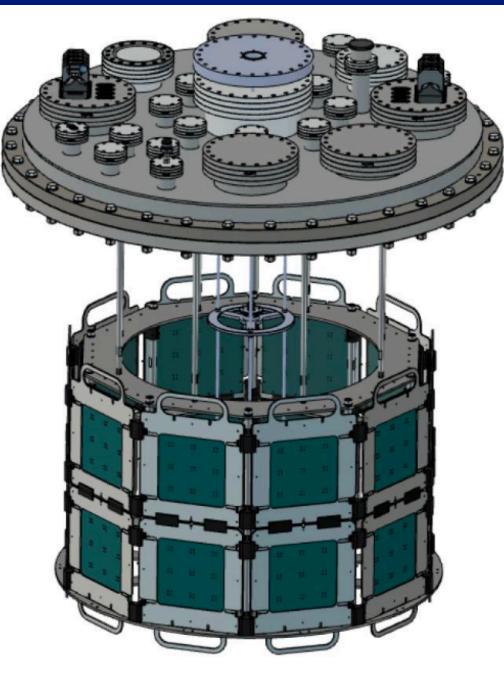
- New ABS resin material investigated for production of the tile handling brackets and the bare SiPM storage trays
- Prevents contamination from CF that were sometimes present after use of Onyx material from FDM printer





Goals of the Liverpool Cold Test site

- Vessel for cold testing of 20 vPDUs per cooldown.
- Central optical calibration system courtesy of Warwick
- VX2745 digitiser, 3x CAEN A2551 LV supplies, 1x CAEN A1541 HV supply.







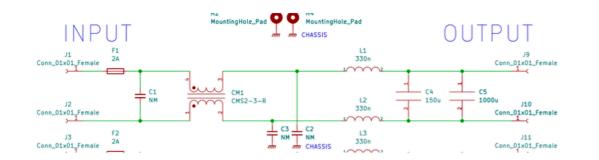
Cryostat current status

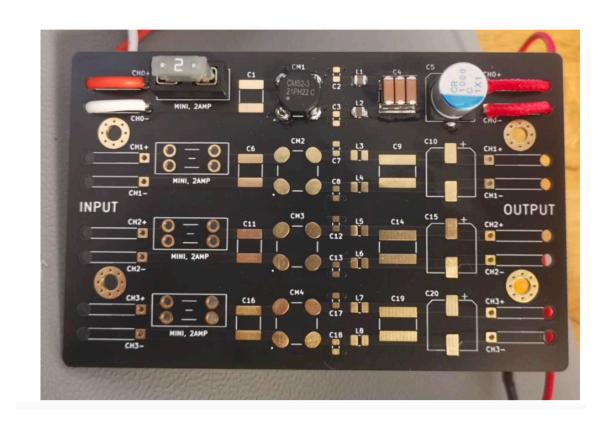
- The main bulk of the mechanics are assembled.
- Need to finish installation of PDU holders, thermocouples, heater etc
- Thermocouples will be installed in four locations, bottom ring, middle ring, top ring and flange underside for feedback during filling/venting.
- MIDAS control of digitisers and LV supplies is essentially ready.
- Testing of full chain using FR4 PDU can happen soon to verify cabling, adapter boards, etc





Electronics for cold testing





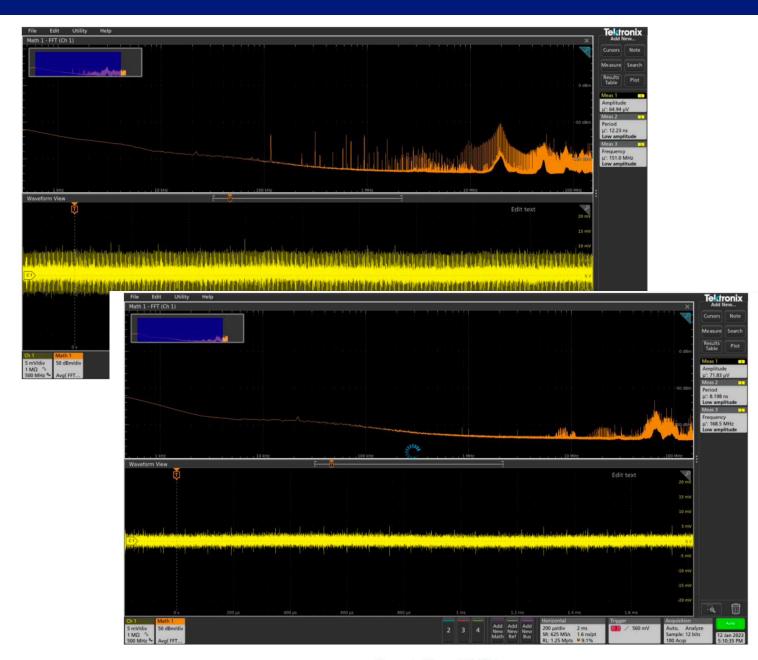


Figure 2: Filtered, 7V/1A

- Due to poor availability of the LTC6820 demo board, a custom steering module board has been developed.
- Enough boards to equip each of the test sites with this same board for a common software/hardware chain.
- Hardware seems to be generally working fine, software, Midas integration etc is being worked on.
- See Martin's talk for more details.

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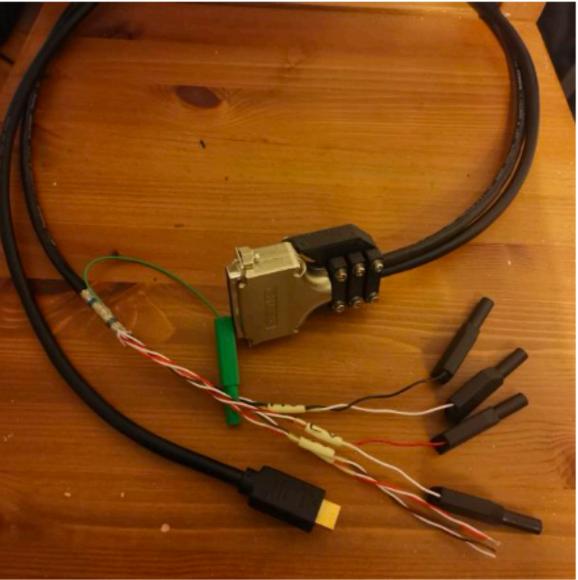
Electronics for cold testing

- We have bought tooling (crimp tools, etc) to assemble high quality dsub style cabling.
- All test stands are using common D50 vacuum feedthroughs for compatibility.
- Liverpool plans to assemble cables for all of the cold test site locations.





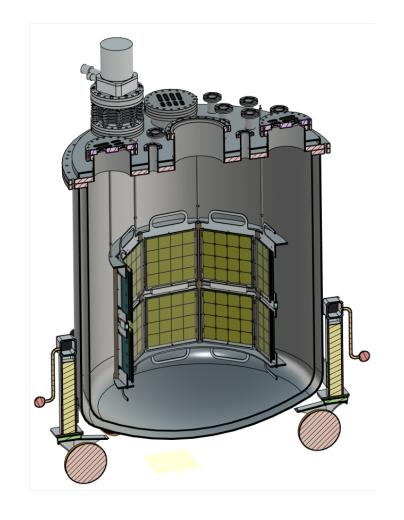




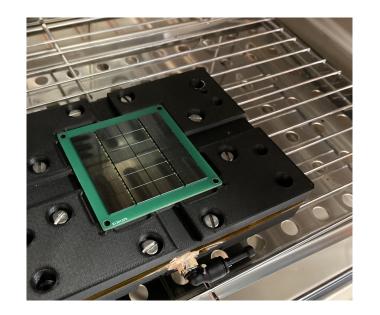


Summary and plans for this year

- vTile design finalised: PCB, mounting pillars and wirebond pattern, radio-assay
- Cryo-probed diced wafers of SiPMs arriving from LNGS and
- vTile pre-production is underway in the LSDC and new staff have been trained in assembly and wire bonding
- Cryostat ready for reception of vPDU3 for first cold tests - some open questions on additional filtering (HV) and feedthroughs will start to be addressed with these tests
- Additional technical effort for production phase to begin soon



How it started...





How it's going

