Using 1S-modules for the MUonE tracker?

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Brief history of 2S-modules

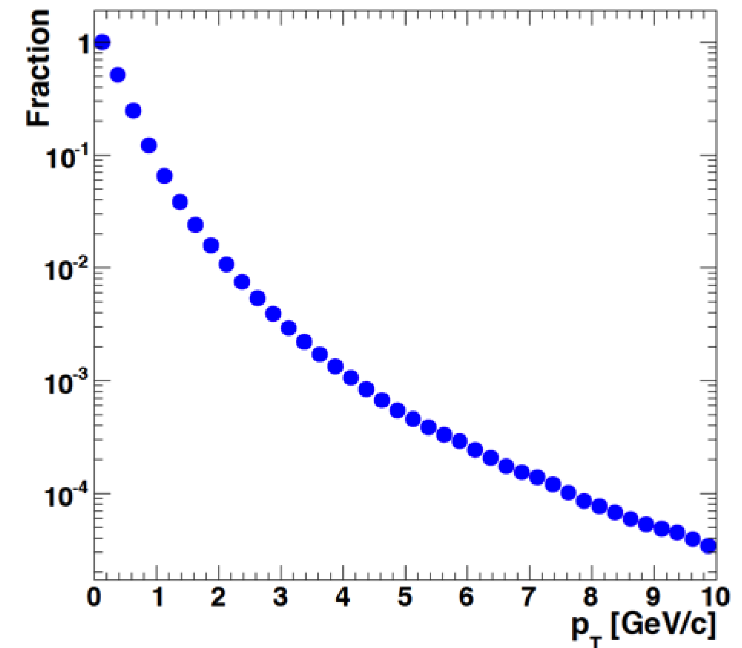
- The 2S-module was devised to provide data to the L1 trigger in CMS
  - Outer tracker : two types of module, each with two sensor layers: 2S (2 x Strips) & PS (Pixel & Strips)
- The present CMS L1-trigger is based on calorimeter and muon data
  - but the rates will increase dramatically for HL-LHC
  - Only limited improvements are possible, with danger of losing physics, e.g. by increasing energy thresholds
- The only extra information potentially available is from the tracker, which has not been used in such a high rate environment because of the volume of data and issues of data transfer
- The CMS tracker 2S-modules were of interest to MUonE because they were available(!)
  - High speed readout but not completely optimal for the purpose
  - However, developing a new module from scratch is a large enterprise

The CMS track-trigger challenge

- It is impossible to transfer all tracker hit data off-detector for trigger decision logic
  - i.e. at 40 MHz, with typical occupancy 1-2%
- so on-detector data reduction (or selective readout) is essential

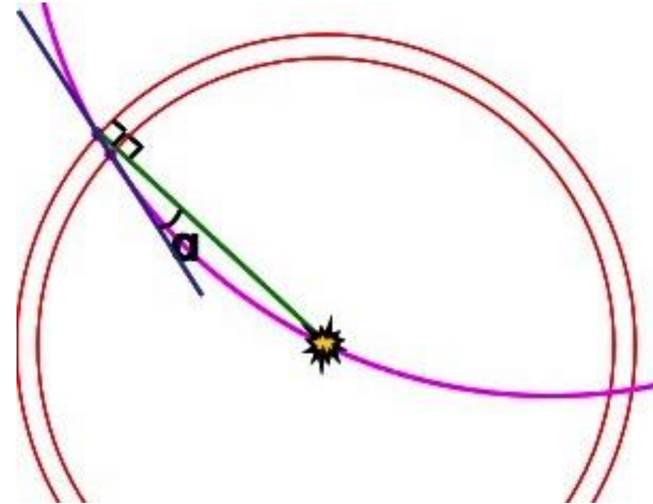
- However 99% of tracks are < 2 GeV/c
  - which are not needed for triggering
- Hence try to suppress hits associated with low p_T tracks

Some very old plots and results, most from Mark Pesaresi's thesis

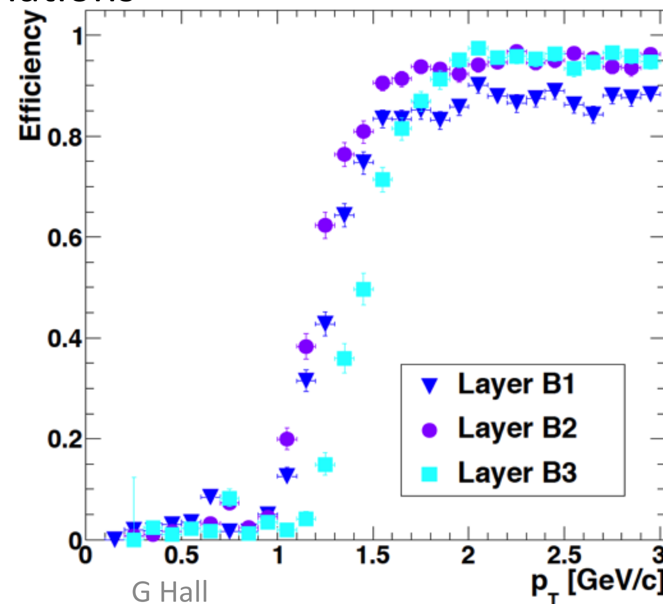


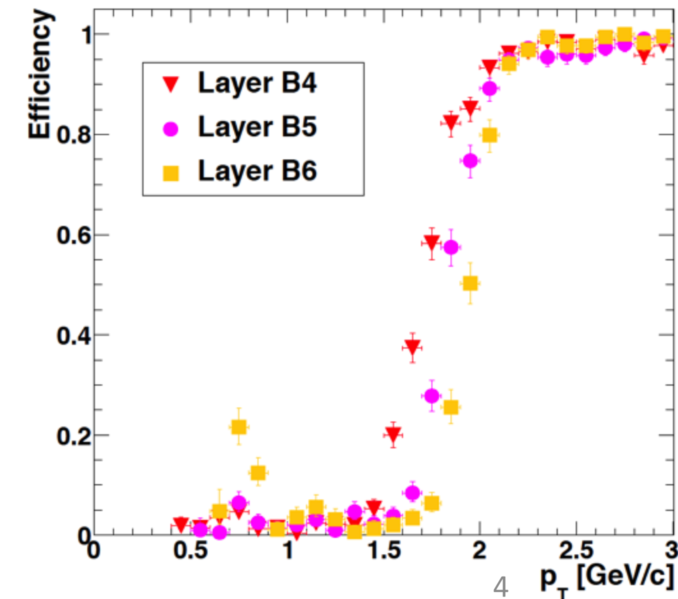
“Stacked-tracker” principle

- Compare pattern of hits in contiguous sensor elements in closely spaced (“stacked”) layers
- pairs of points (“stubs”) make a short vector



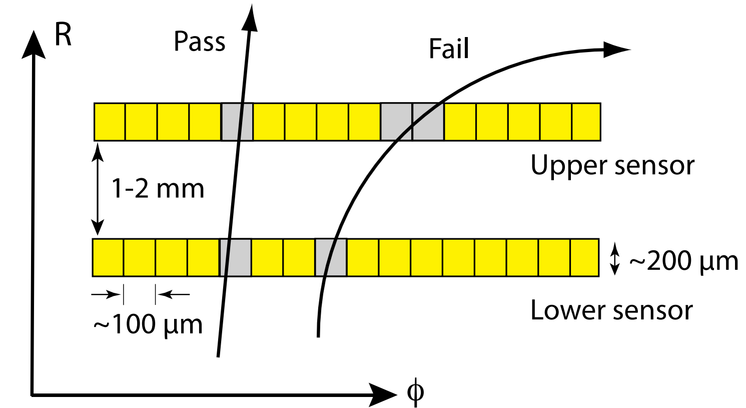
  - p_T cut set by angle of track in layer
  - primarily depends on layer separation
    - but increasing separation worsens fake combinations
  - details depend on
    - pitch
    - thickness
    - charge sharing
    - track impact point
    - …
  - the penalty is extra material

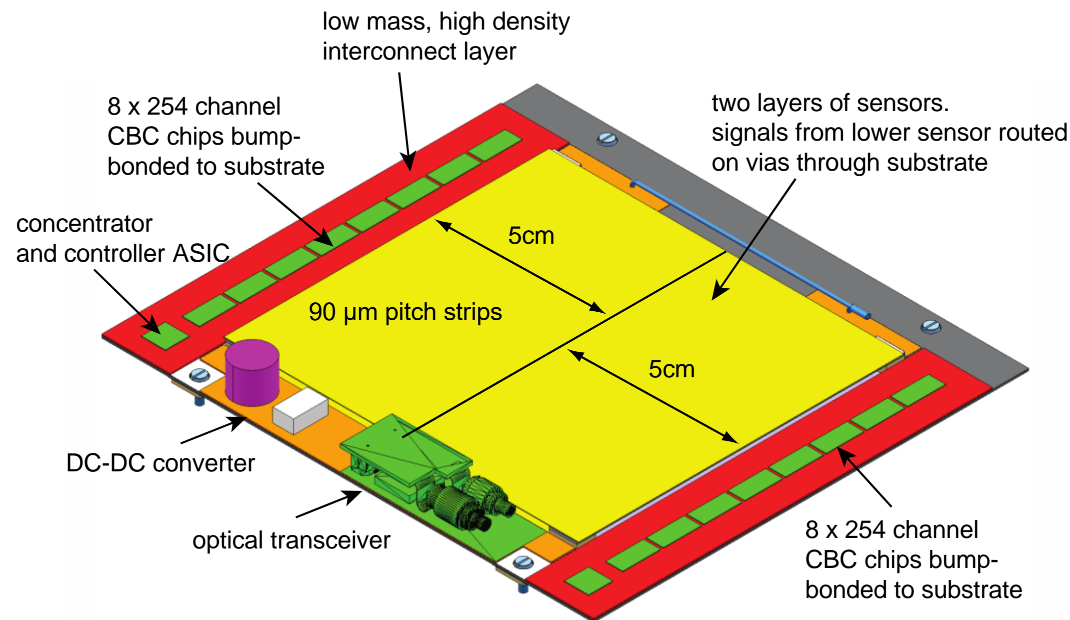




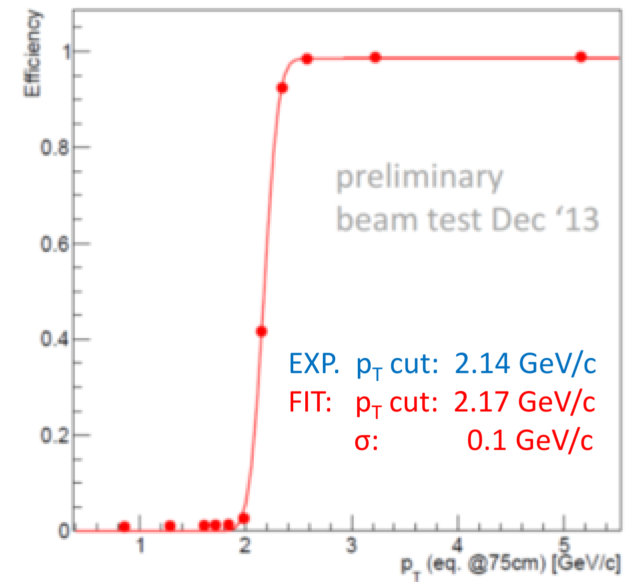
2S-module schematic design

- ~15000 PS & 2S modules transmitting
  - p_T-stubs to L1 trigger @ 40 MHz
  - full hit data to HLT @ 0.5-1 MHz





~8400 2S-modules, inc spares



reconstructed p_T cut of r=75cm layer

MUonE tracker: optimisation

- Possible weak points in the present layout of each station:
  - relatively few measurement points for fully efficient detection and pattern recognition
  - not true 3D-points, so could be vulnerable to beam pileup and combinatorial problems
  - still to understand the optimal operation for asynchronous data (CMS is mostly synchronous)
- Possible improvements – add layers
  - but would risk problems from extra material
- **Can this be addressed by building 1S-modules, instead of 2S-modules?**
  - mechanically, modifying CMS modules seems to be possible (input from Perugia)
  - electronic weak point: stubs are needed for 40 MHz readout.
    - hits are only read out following a trigger, which is not foreseen in MUonE, at rate < 1 MHz
- However, fake stubs can be made by the CBC, without a second sensor
  - they are identical to hits, since the stub is defined by the position in the seed layer
    - bend information is not real, but is not very valuable anyway

Faking stubs

- Must find a cluster in the correlation layer
  - Some noise hits will be present, if threshold is set low enough
  - Rate depends on amplifier characteristics and noise sources
    - O(few MHz), & calculable, see GH NIM A371 (1996) 580
  - Two modes of CBC operation: Fixed Pulse Width (latched) and Sampled
    - latched – a threshold crossing within a clock cycle
    - sampled – a threshold crossing at any time prior to observation, with later descent below threshold
  - Latched mode rate was measured
    - Kirika on bare chip: ≈ 8 MHz (as would be used in 1S-module)
    - Martin Delcourt on module: ≈11 MHz, expected from extra sensor capacitance
    - Neither rate is sufficient to **guarantee** presence of noise hit in correlation layer (next slide)
  - Sample mode can be used (probably with double, not single, bunch timing?)

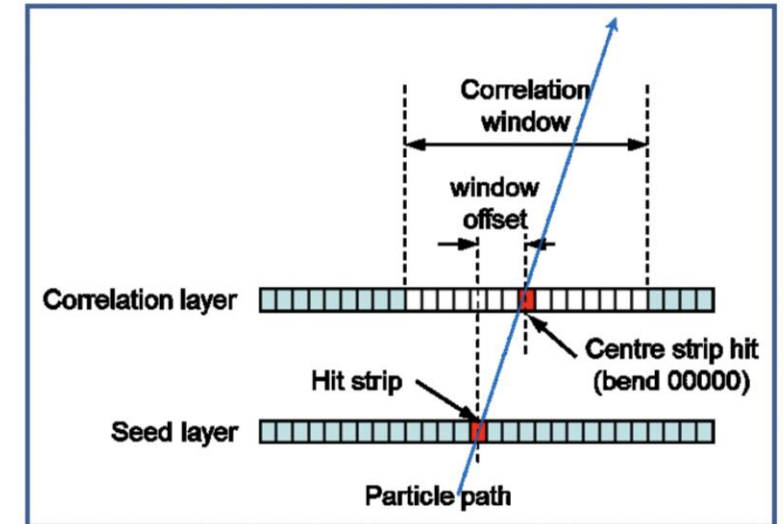


Figure 16 — Example of Correlation Window & Offset Correction

Nuclear Instruments and Methods in Physics Research A 371 (1996) 580–582

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

Level crossing rates in binary counting systems

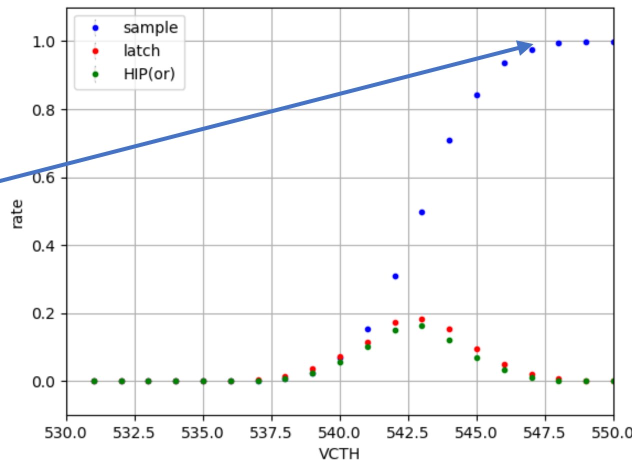
G. Hall

Threshold crossing rates on bare CBC

1S study Kirika

NB sample mode efficiency is 100% for low thresholds

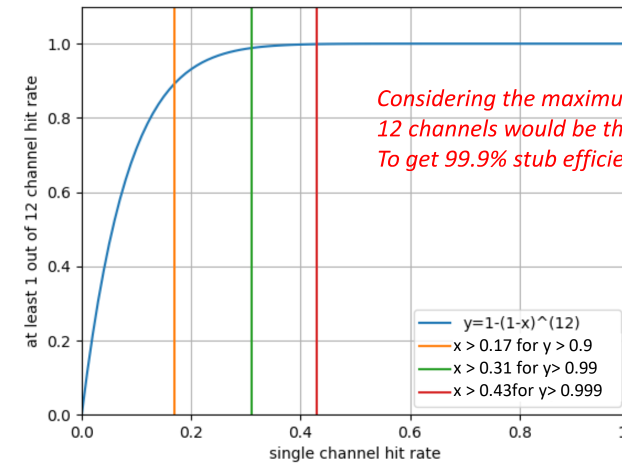
Single channel hit rate for noise vs VCTH



The maximum hit rate is below 0.2 for latch and HIP mode.

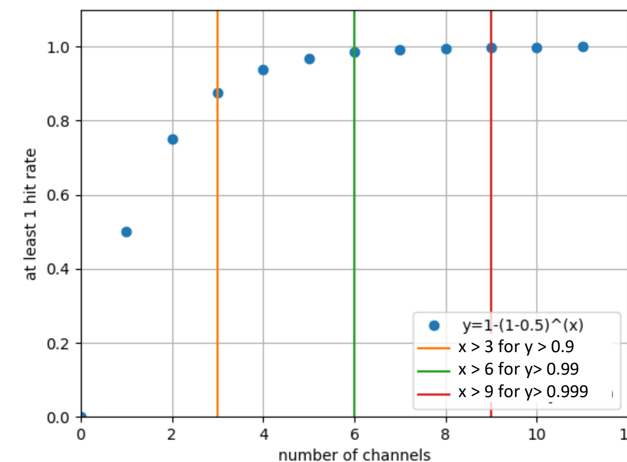
The sample mode could produce stubs,
but the asynchronous signal could create two consecutive stubs
which could overflow at the concentrator chip on the hybrid.
(The analogue signal at the comparator goes back to the baseline in 50 ns.)

Rate of at least 1 hit in 12 channels vs single channel hit rate



Considering the maximum window and cluster width, 12 channels would be the limit per seed. To get 99.9% stub efficiency, 43% hit rate per channel is necessary.

At least 1 hit rate vs number of channels at 50% single hit rate

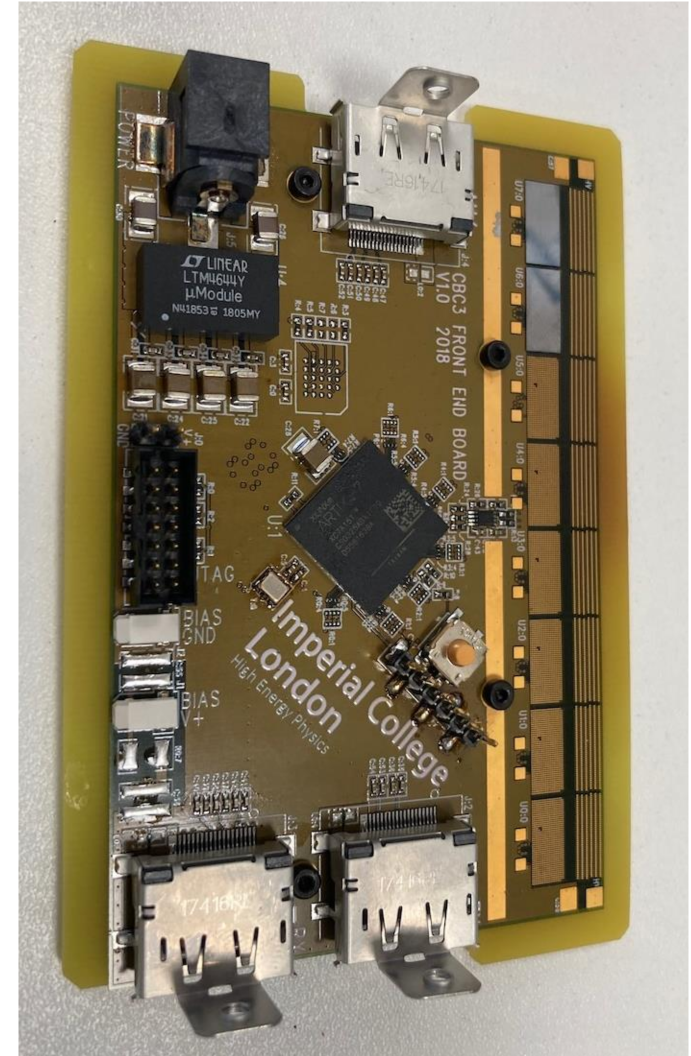


9 channels need to be active per seed for 99.9% stub efficiency

Binomial probability calculations of latched mode efficiency

Constructing 1S-modules

- It’s possible to omit a sensor from 2S-modules, but CMS may not want to do so
  - Radiation hard components not essential for MUonE, and module size less constrained
- Can we build them in MUonE?
  - prototype 8-CBC hybrids designed 2019, but only recently assembled
    - FPGA and communications interfaces
      - No concentrator chip. Free from stub overflow.
    - now under test, so far with 2 CBCs mounted in house
      - Digital interface to FPGA is tested and works as expected.
      - Testing for the connectivity of analogue input side is under development.
  - challenge – also for CMS - to assemble hybrids but C4 technology is not new!
- Probably most efficient to split CBC hybrid from other functions
  - no shortage of CBCs, even if hybrid yield is low
  - sensors being discussed with CMS but should be obtainable from HPK
- More is needed for a complete module
  - mechanical & thermal design, assembly and qualification teams
    - collaborators would be very welcome



Summary

- Several advantages of 1S-modules
  - 1S-modules would be **cheaper** – CMS estimate has 60% of 2S-module cost for sensors
    - some encouraging indications that HPK sensors could be obtained
  - If 1S-modules can be used throughout, the material budget and number of measurements can be optimised
  - Although mechanical design is needed, it should be much simpler than for 2S-modules

- Proof of principle
  - Fake hits in correlation layer can certainly be produced
    - sample mode is needed
  - Data with sample mode readout were acquired in recent beam test
    - but still to be analysed

- Module assembly
  - Modules could be assembled with CMS components, but so far has been delayed a lot
    - radiation hard components are not really needed and add to cost cf. commercial parts
    - Risk of losing some stubs at concentrator chip with sample mode
  - Could MUonE build all its own modules? It seems feasible, but effort is needed (anyway?)

Backup

2S module design

SEH
- DCDC converter for powering
- lpGBT & VTRx+ for data transmission

Ground Balancer
- connects left and right FEH

FEH
- 8 CBC
- 1 CIC
- Folded around AlN spacers to connect to both sensors

Al-CF Bridges
- C-Fiber reenforced Al
- Positioning and cooling
- 2 main bridges
- 1 or 2 stump bridges
- Define sensor spacing

2 x Strip Sensor
- 2 x 1016 strips each
- 290 μm (320 μm) active (physical) thickness
- ~10 cm x 10 cm

2S module assembly

1. Glue Kapton isolators and HV tails to sensor backsides

Check dicing precision (metrology)

Optical inspection

2. Wire-bond and encapsulate HV tails

HV test backside isolation

Sensor I(V)

3. Glue sensors on Al-CF bridges

Module metrology

4. Glue FEHs, SEH and ground balancer to bare module

Optical inspection

(HV/LV test)

5. Place wire-bonds

Module test

6. Encapsulate wire-bonds

Module test

adapted from Stefan Maier

A. Mussgiller | 2S and PS Module Design, Assembly, QC and Part Procurement | 26/10/2023

7

C4 bump bonding

- Ancient technology, developed by IBM in 1960s
  - so readily available, industry-standard??
  - standard BGA pitch = 500 µm
  - C4 allows pitch >200 µm. CBC pads on 250 µm
- We have mounted individual chips in-house
  - lead-free solder melts at low enough temperature
  - high enough yield with 8 CBCs??
  - large-scale commercial hybrid assembly still proving challenging

Motorola IEEE paper 1994

C4 flip-chip technology utilizes 97/3 Pb/Sn solder bumps deposited on wettable metal terminals populating the active surface of a semiconductor chip (**Figure 1**). C4 bumps are aligned to the substrate's corresponding metal pads and reflowed at high temperature (365°C peak) to simultaneously form electrical and mechanical connections (**Figure 2**). Surface tensions of the molten solder self-align the chip to the substrate making C4 assembly extremely robust. A liquid underfill can be dispensed and cured to enhance C4 reliability.

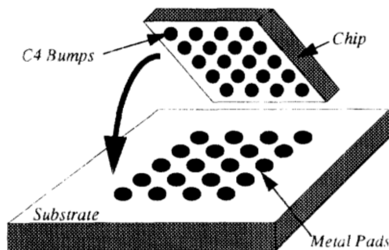


Figure 1 - C4 Flip-Chip Technology

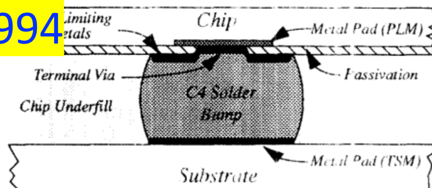


Figure 2 - Controlled Collapse Chip Connection (C4)

DCA, illustrated in **Figure 3**, utilizes low melting eutectic lead/tin solder selectively deposited on an organic substrate.

The low melt solder wets to the C4 solder bumps on the chip with minimal diffusion. This allows rework of the DCA assembly if necessary. Because the C4 bump does not reflow, a finite standoff is defined between the chip and substrate. In the purest sense, the DCA process does not form a C4 as the C4 solder bump on the chip does not collapse.

The flip chip technology was introduced by IBM in the early 1960s for their solid logic technology, which became the logical foundation of the IBM System/360 computer line [1]. Figure 1(a) shows the first IBM flip chip with three terminal transistors, which are Ni/Au plated Cu balls embedded in a Sn–Pb solder bump on the three I/O pads of transistor. A Cr–Cu–Au adhesion/seed layer is deposited between the Al–Si contact pads on the Si chip and the solder bump. Figure 1(b) shows the first IBM flip chip assembly (three chips) on a ceramic substrate.

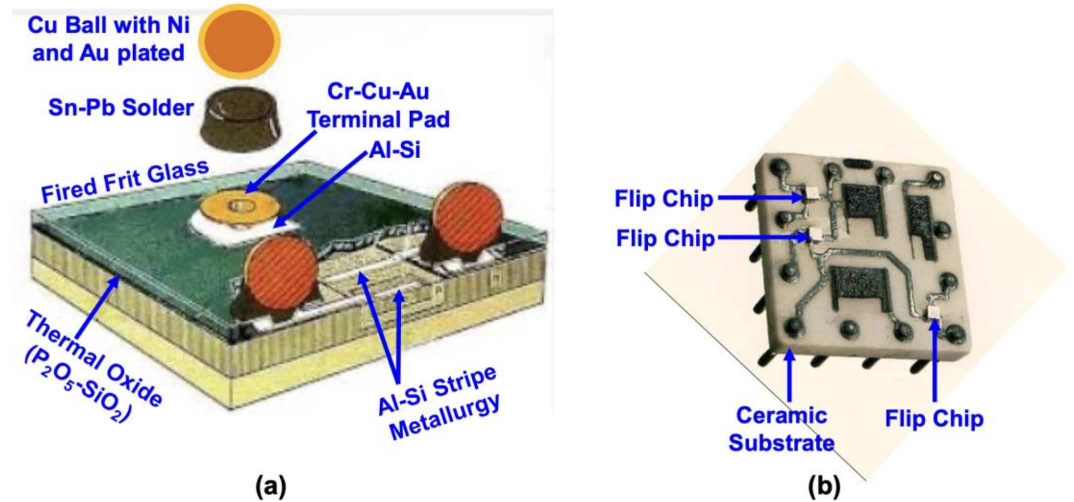


Figure 1 - (a) IBM's first flip chip component with 3 terminal transistors. (b) IBM's first flip chip assembly (3 chips) on a ceramic substrate

As the I/Os increase, the Cu ball is replaced by solder bump. The so-called C4 (controlled-collapse chip connection) technology [2] utilizes high-lead solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate. The solder-bumped flip chip is aligned to the substrate, and all solder joints are made simultaneously by reflowing the solder.