AGH University of Science and Technology

Design and performance of the SALT ASIC

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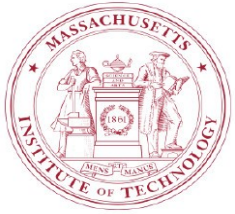
MPP2023 – II Workshop on Muon Precision Physics
7–10 November 2023, Liverpool, UK

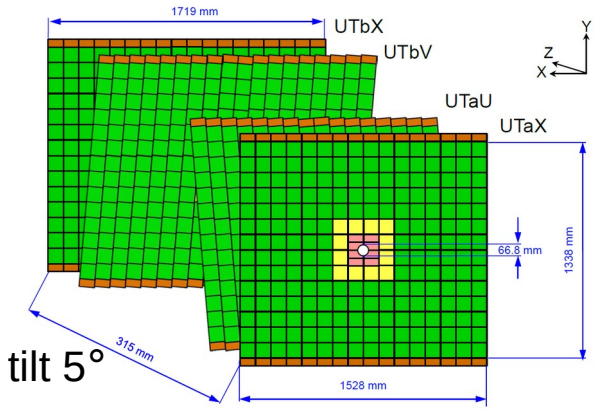
Outline

- Introduction
- SALT design
  - Main blocks (FE, ADC, DSP)
  - Layout and power delivery
- SALT measurements
  - SALT on hybrid with 12pF sensor – full tests with transmission of digitized data
- Summary

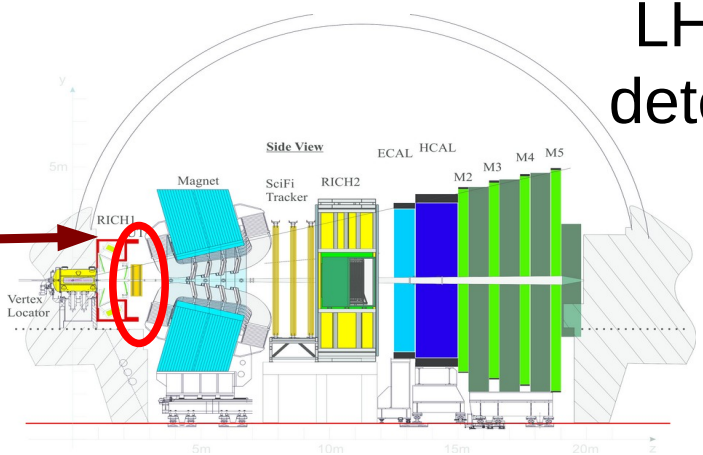
UT working group in SALT design



Introduction
Upstream Tracker (UT) in LHCb detector



LHCb detector



- UT is part of LHCb Inner Tracker
  - silicon strip sensor (4 types)
    - p^+-in-n, 10 cm
    - n^+-in-p, 10/5 cm
  - ~1000 hybrids with 4 or 8 ASICs

- SALT (~4000 ASICs)
  - 128 channels (500k in total)
  - 40 MHz – machine clock
  - Variable data rate and number of active e-links (3-5)

Introduction
SALT specification (version 3)

- CMOS 130 nm technology
- 128 channels (80um pitch), Front-end & ADC in each channel
- Sensor: capacitance 1.6–12 pF, AC coupled
- Input charge range ~30ke– with both polarities (p^+-in-n and n^+-in-p)
- Noise: ENC ~1000e– @10pF + 50e–/pF
- Pulse shape: T_{peak}~25 ns, very short tail: ~5% after 2*T_{peak}
- Crosstalk < 5%
- ADC: 6-bit resolution (5-bit&polarity), 40MS/s
- DSP functions: pedestal and common mode subtraction, zero-suppression
- Memory: 5kb (648 bytes or 430 12-bit words)
- Serialization & Data transmission: 320 Mbps e-links to GBT, SLVS I/O
- Slow control: I^2C (~350 cfg. regs.)
- Power < 6 mW/channel
- Radiation hardness ~30 MRad

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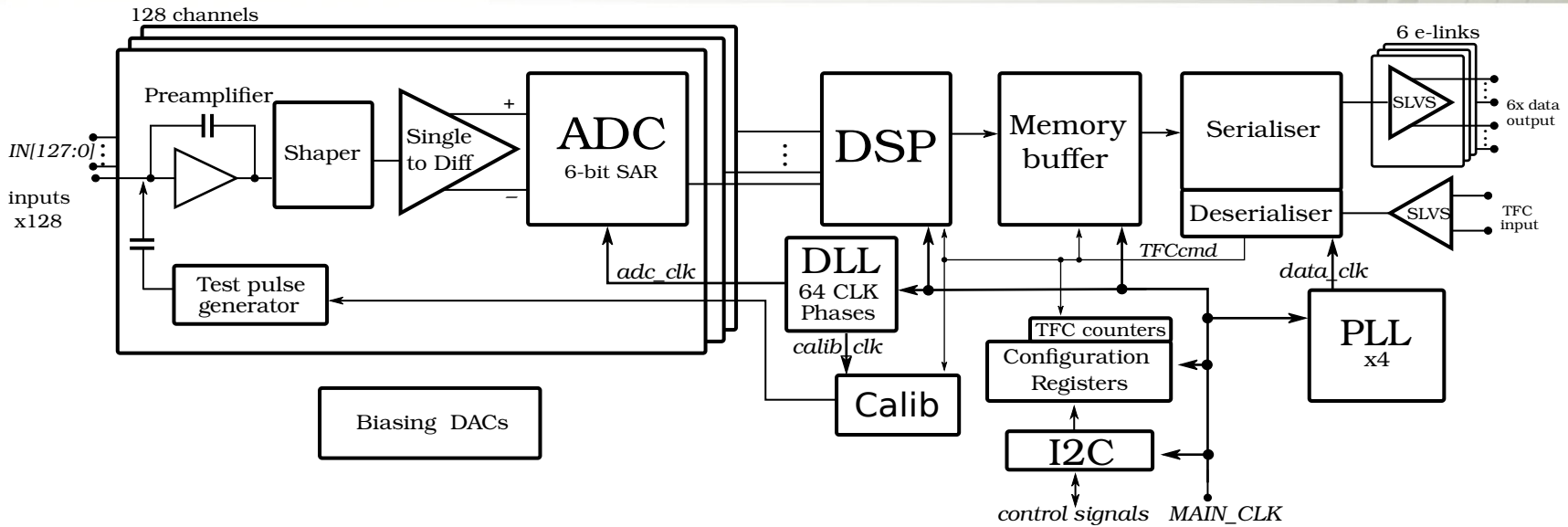
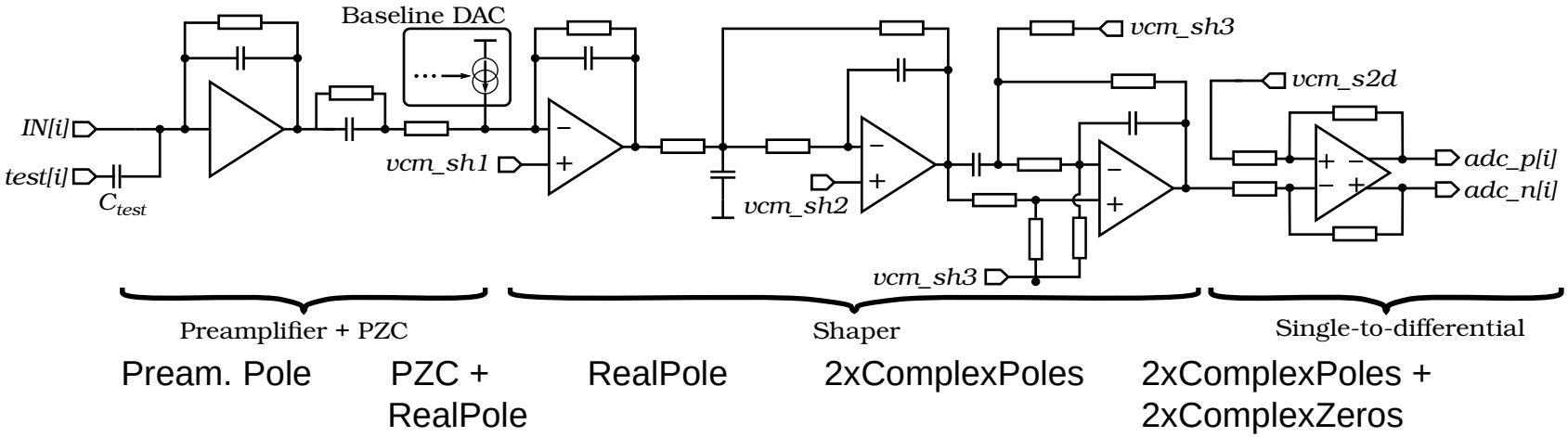
SALT – Silicon ASIC for LHCb Tracking Architecture



- Front-end & ADC in each channel – 128 standard channels plus 2 test channels (nr -1,128 not shown) with analogue outputs
- Digital Signal Processing (DSP) of the ADC data
- And many other features/blocks: PLL, DLL, TFC, I2C, serialiser, SLVS I/O, biasing DACs, monitoring ADCs, …. (not all shown)

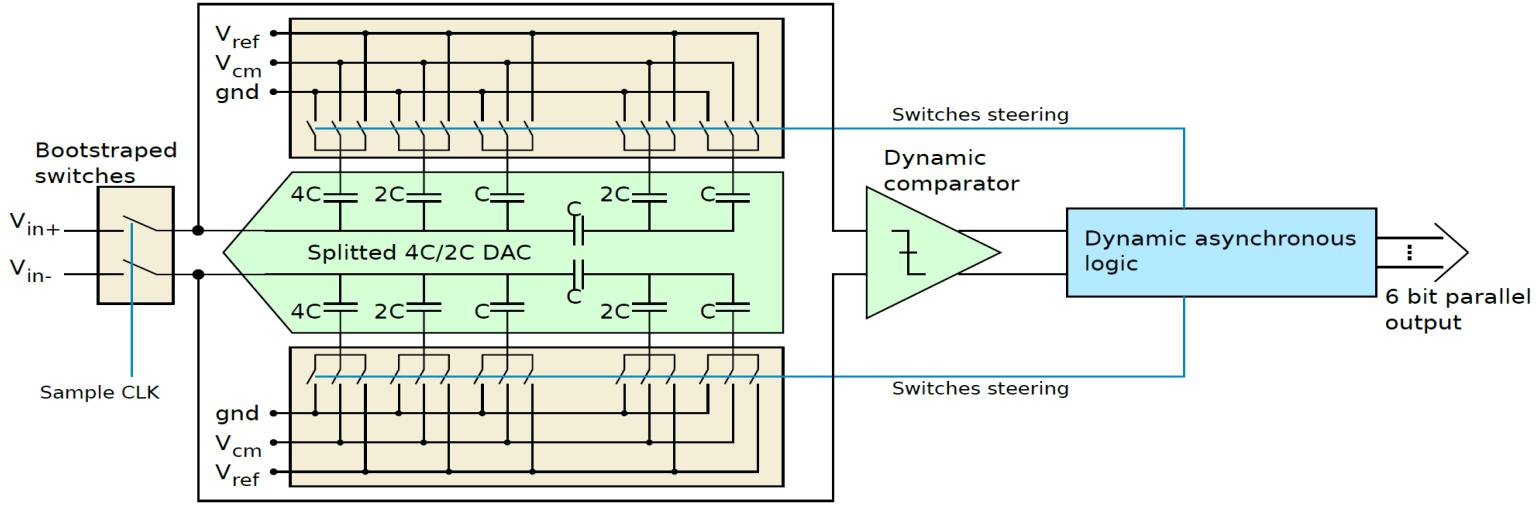
SALT design
Preamplifier&Shaper and Conv. Single-to-Diff.

Simplified circuit diagram



- 3-stage shaper (complex poles and zeros) gives the pulse with short tail
- Common mode (vcm_sh) at half power supply for both pulse polarities
- Single-to-Differential converter to generate differential signal for ADC
- Power consumption: ~1.5 mW

SALT design
6-bit ADC



SALTv3:

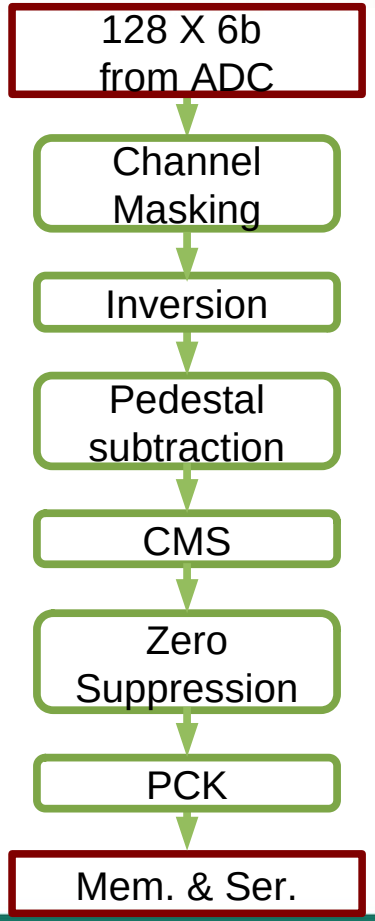
optional dummy current added (constant current after conversion) to keep current consumption more stable

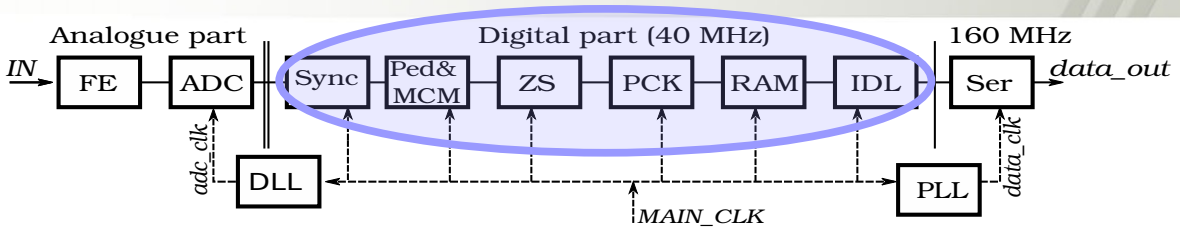
Main features:

- SAR architecture, 6-bit resolution
- 40 MSps nominal sampling rate
- Merge Capacitor Switching (MCS)
- Bootstrapped input switches

- Dynamic comparator
- Dynamic asynchronous logic
- Pulsed power consumption
- Power consumption ~350µW+400µW

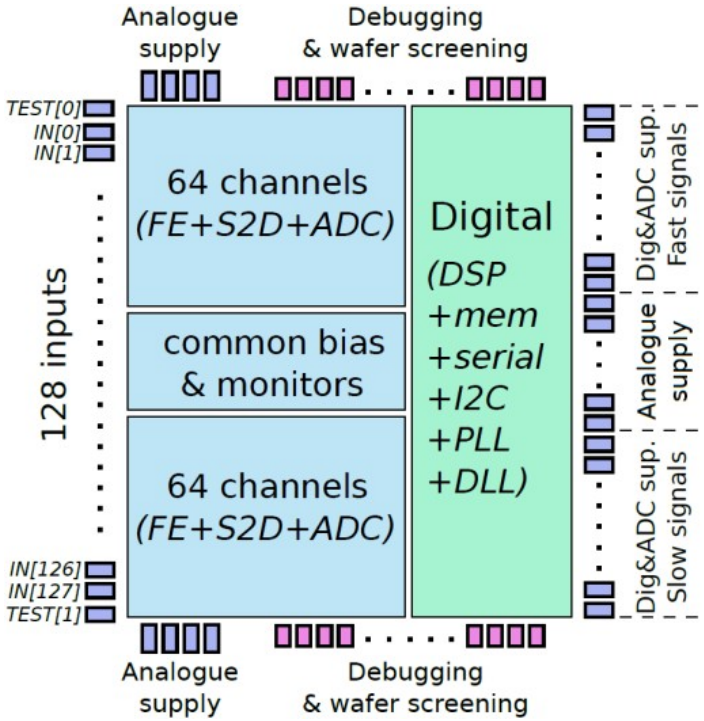
SALT design
DSP operations



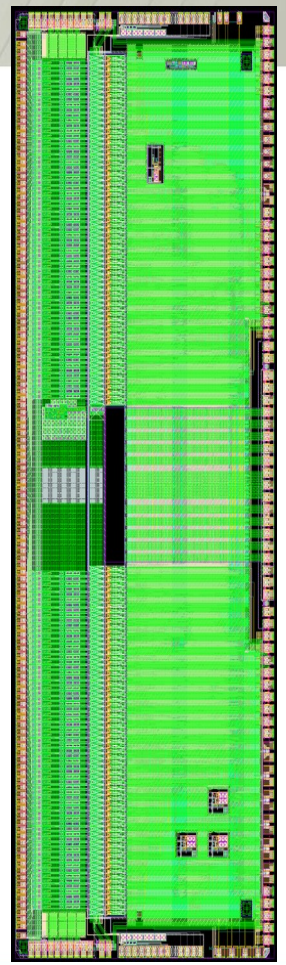


- Input data: 6 bits (5 bits plus sign – 2's complement)
- Noisy or dead channels can be masked
- All channel values can be inverted (1 config bit)
- Pedestal subtraction in each channel (saturation arithmetic)
- CMS – (Mean) Common Mode Subtraction
  - average of all channels below CM threshold
  - subtraction in each channel
- ZS – Zero suppression
  - only channels above ZS threshold are sent out
- PCK – Packet building (TFC & mem. occupancy depended)

SALT Design
Floorplan and layout – SALTv3.9



- Power can be delivered top&bottom (recommended) or from back side
- Analogue power distribution redesign to minimize inductances – important because of ADC power consumption
- Additional test channels (top and bottom) available from scope



- Left & right sides bonded to the hybrid.
- **Top&bottom pads best for analogue supply**

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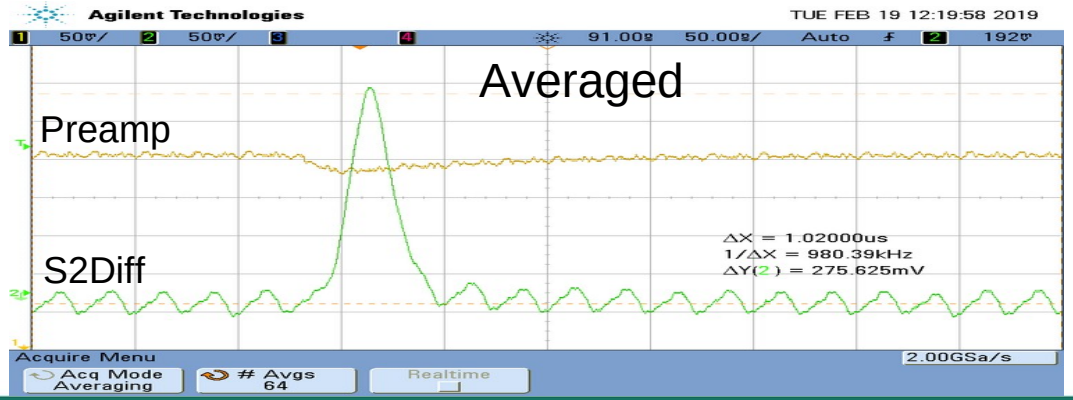
Analogue test channel output (@scope)

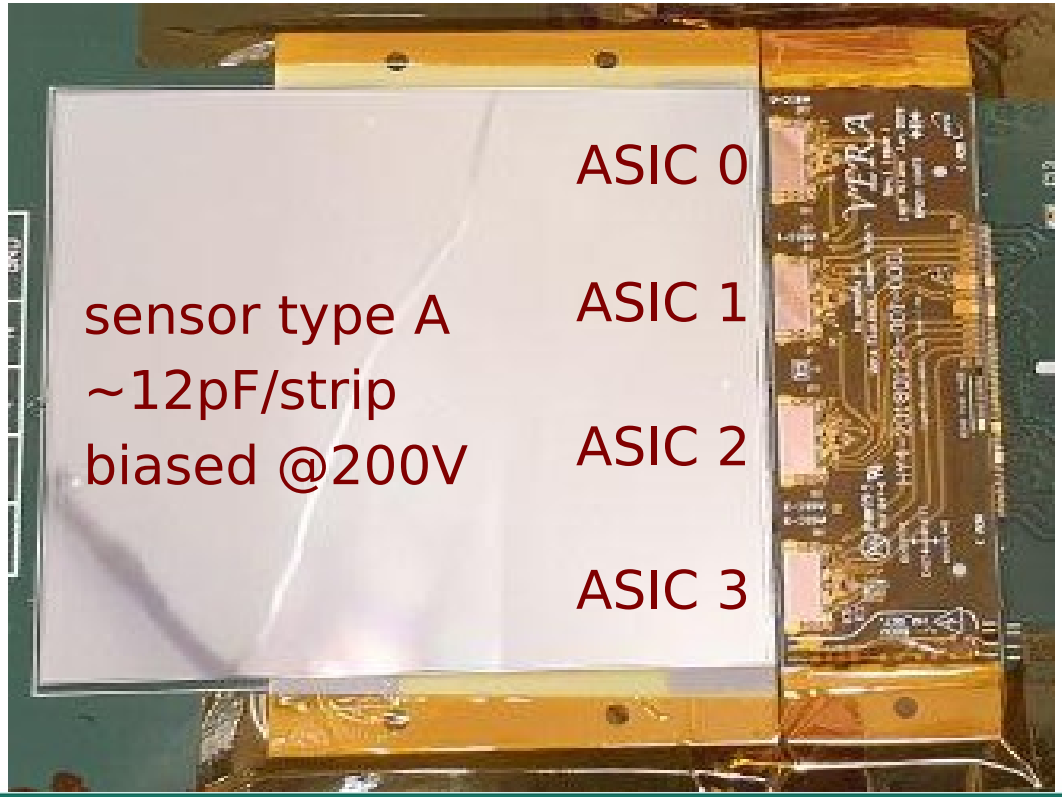


Transient response to MIP (~4fC) with 12pF external input capacitance

- For SALTv3 good pulse response is seen with large input capacitance
- With large input capacitance small 40MHz disturbance is still present (also in simulations)

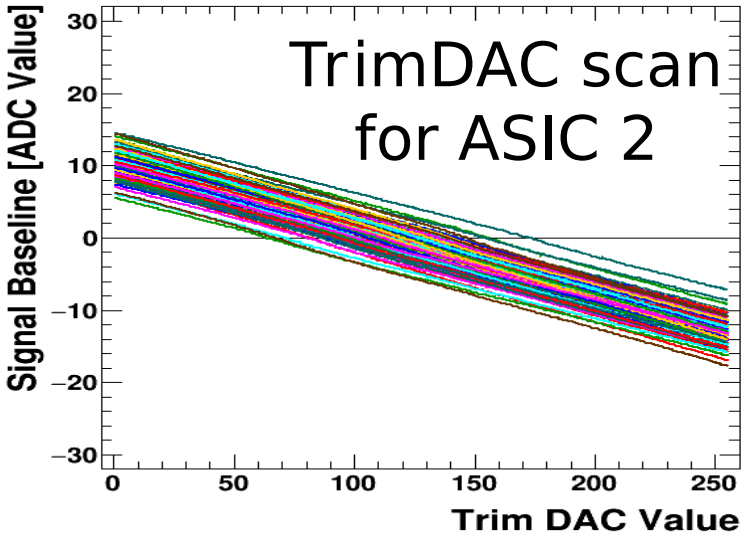
SALT on hybrid
(full tests with digitized data)

Hybrid with the largest sensor and 4 SALT ASICs

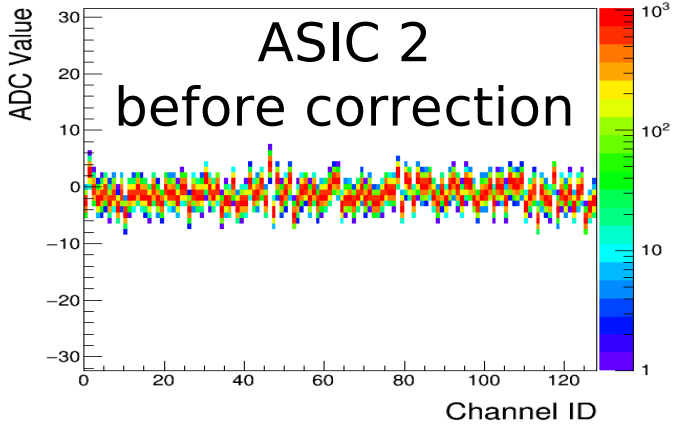


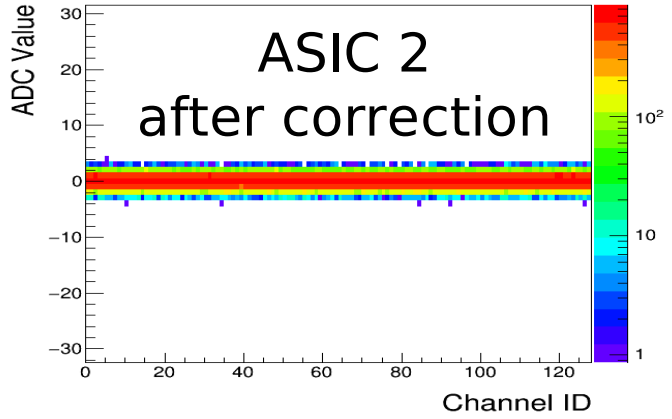
- Power consumption of ASIC @ Vsup=1.2 V:
  - ~580 mW (total)
  - ~4.5 mW/channel (within spec.)
- Hybrid design crucial for analogue performance – minimisation of 40MHz disturbances

Baseline correction



Each channel is corrected by setting its own TrimDAC

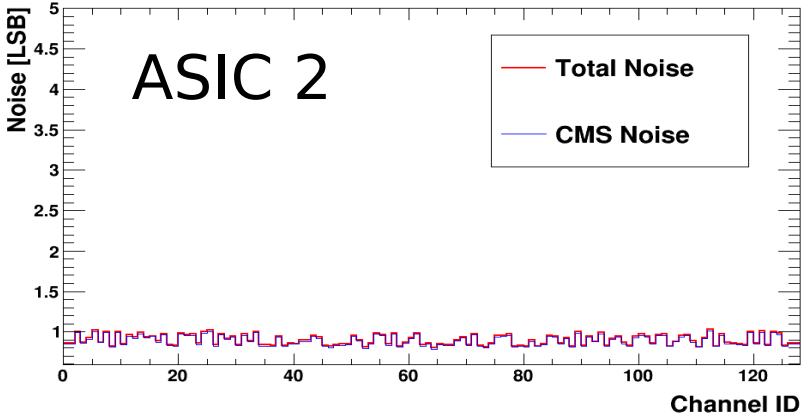




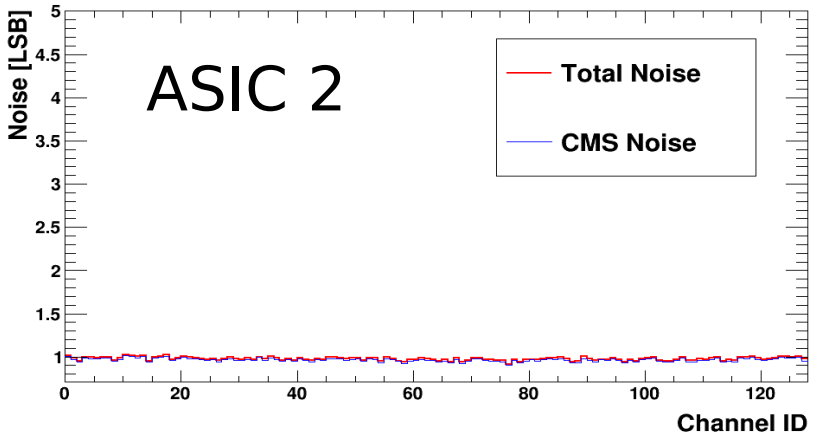
- Analogue baseline correction works well
- Important for DSP processing – pedestal subtraction may be a second step if needed

Noise with 12pF sensor (on hybrid)

Before TrimDAC correction



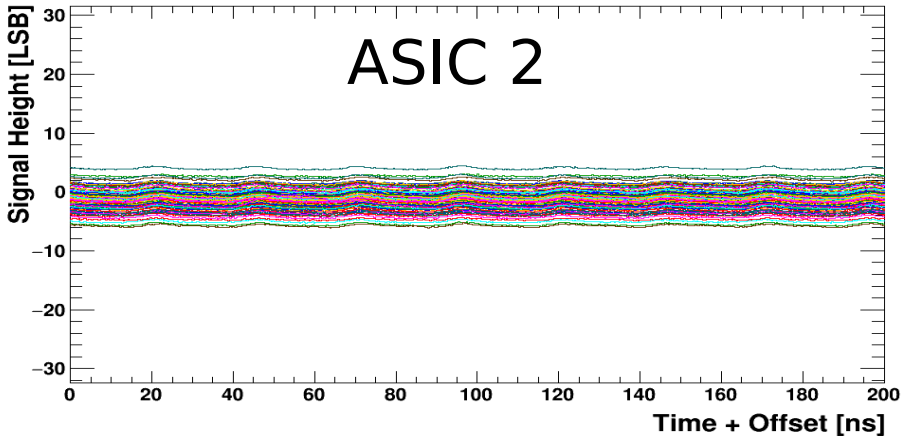
After TrimDAC correction



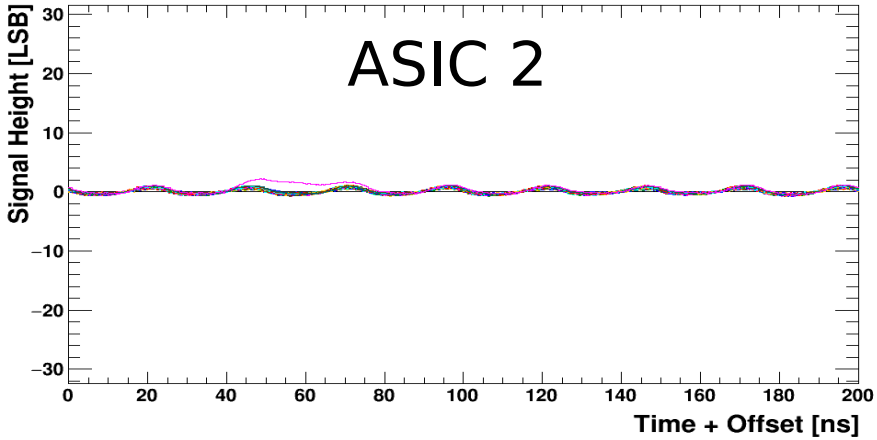
- Measurements show that noise RMS is slightly below 1 LSB
- For MIP (4 fC) one can estimate SNR above 10

Baseline versus time

Before TrimDAC correction



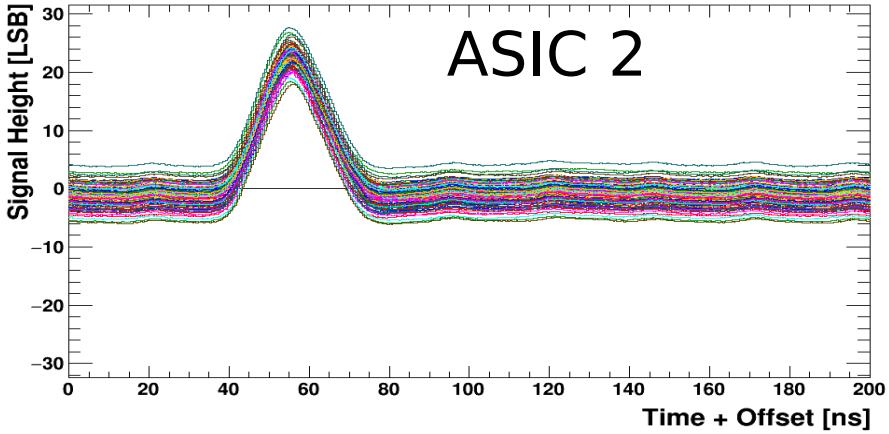
After TrimDAC correction



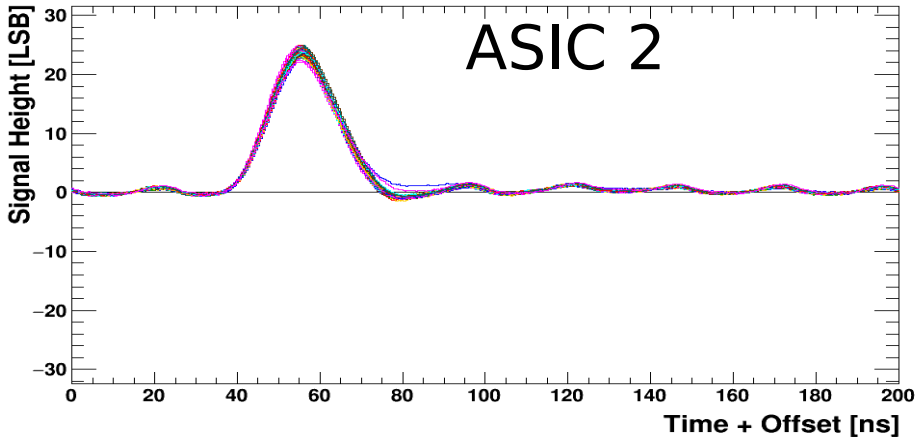
- In standard operation samples are taken every 25ns
- To obtain above plots internal DLL was scanned over all 64 phases ($\Delta t = 25ns/64$) and data was averaged for each phase
- In standard operation small 40MHz component is seen as constant offset but can be subtracted in DSP

SALT on hybrid with 12pF sensor
Pulse shape

Before TrimDAC correction



After TrimDAC correction



- Pulse shape is obtained via DLL scan
- Observed pulse shape is consistent with simulations

- Disturbances are small and similar to scope measurements of analogue test channels

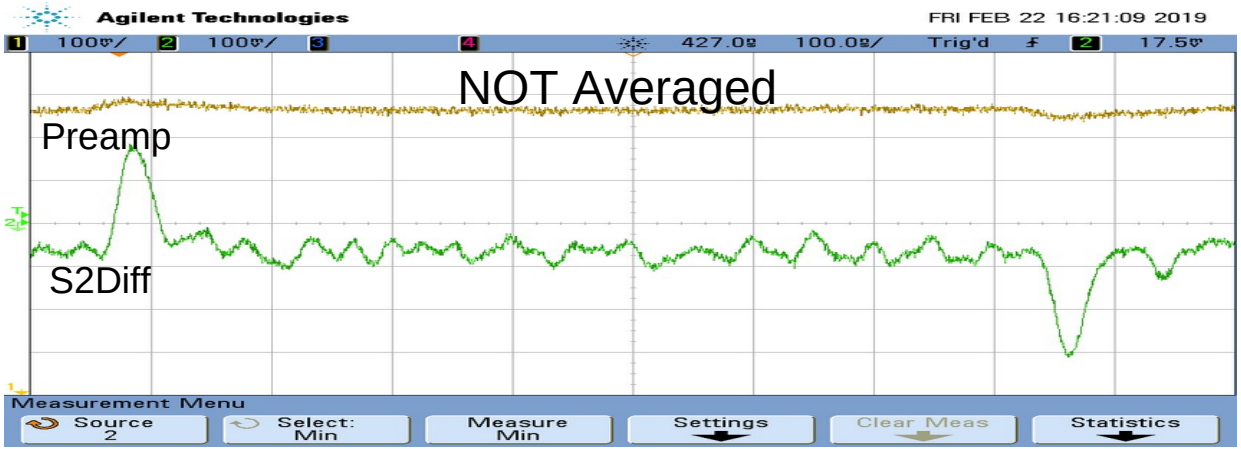
Summary

- SALT is the world first high speed readout ASIC for HEP detector with fast ADC (40MSps) implemented in each channel
- About 5000 chips are already working in the LHCb detector
- Recommendation for usage:
  - version 3.9 (more SEU robust)
  - supply from top&bottom
  - existing 4-chip SALT hybrid as a starting point
- Existing calibration and monitoring procedures may be adapted

Thank you for your attention

Backup

Analogue test channel output for large input capacitance (@scope)

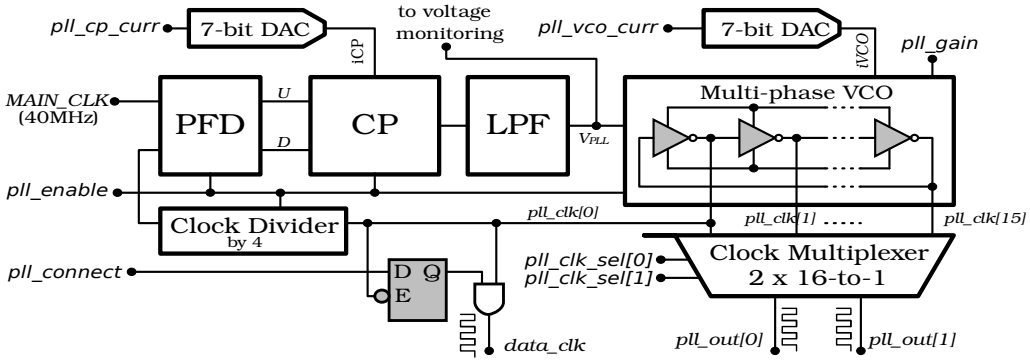


Transient response to MIP (~4fC) with 24pF external input capacitance

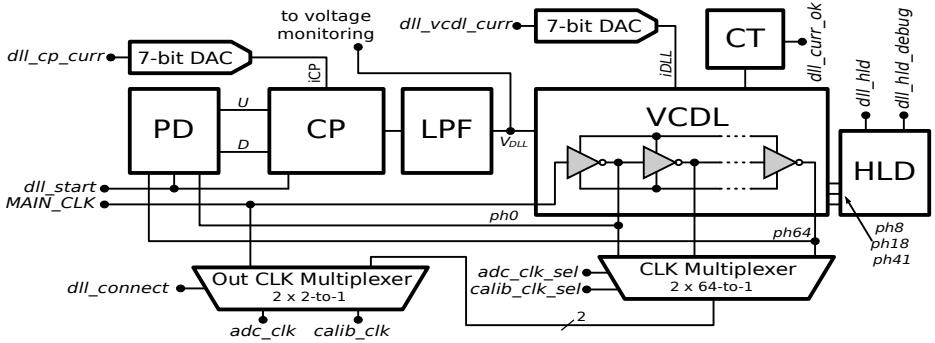
- Good pulse response is seen even with 24pF input capacitance
- With this capacitance small 40MHz disturbance are also present

SALT design
PLL, DLL

PLL



DLL



PLL features:

- High frequency (160 MHz) clock for DDR serializer
- Input frequency 40 MHz
- Power consumption ~0.5 mW @ 160 MHz
- 2 output phases (multiplexing) selected from 16 uniform phases (receiver synchronization)

DLL features:

- ADC sampling phase setting
- Test pulse phase setting
- Input frequency 40 MHz
- Power consumption ~0.7 mW
- 2 output phases (multiplexing) selected from 64 uniform phases

SALT Design
Data packets

Packet name	Header (12-bit)				Data	Comment
	BXID	Parity	Flag	Length		
	4 bits	1 bit	1 bit	6 bit	n·12 bits	
Idle	0000	1	1	'b11_0000	—	no enough data
BxVeto	*bxid_cnt[3:0]*	*	1	'b01_0001	—	BxVeto in TFCcmd
HeaderOnly	*bxid_cnt[3:0]*	*	1	'b01_0010	—	HeaderOnly in TFCcmd
BusyEvent	*bxid_cnt[3:0]*	*	1	'b01_0011	—	*nHits*> 63
BufferFull	*bxid_cnt[3:0]*	*	1	'b01_0100	—	no space in memory
BufferFullN	*bxid_cnt[3:0]*	*	1	'b01_0101	—	no space in memory
NZS	*bxid_cnt[3:0]*	*	1	'b00_0110	Values	NZS in TFCcmd
Normal	*bxid_cnt[3:0]*	*	0	*nHits*	Hits	Normal event
Sync	*bxid_cnt[11:0]*				*sync_pattern*	Synch in TFCcmd

- All packet consist of 12-bit words
- Packet type depends on
  - TFC command (Sync, HeaderOnly, BXVeto, NZS)
  - Memory space (BufferFull, BufferFullN, Idle)
  - Number of hits (BusyEvent)
- NZS packet contain debug information: common mode and non active channels (MCM)