Nuclear Inst. and Methods in Physics Research, A 1034 (2022) 166826

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

Development of high voltage-CMOS sensors within the CERN-RD50 collaboration

E. Vilella, on behalf of the CERN-RD50 collaboration[1]

The University of Liverpool, Department of Physics, Liverpool L69 7ZE, UK

ARTICLE INFO

Keywords:
CERN-RD50
Depleted monolithic active pixel sensor
Future hadron colliders
High voltage-CMOS technology
High voltage pixel detector
Monolithic CMOS detector

ABSTRACT

This paper presents work done by the CERN-RD50 collaboration to develop and study monolithic CMOS sensors for future hadron colliders, especially in terms of radiation tolerance, time resolution and granularity. Currently CERN-RD50 is completing the performance evaluation of RD50-MPW2 and has recently submitted RD50-MPW3, the second and third prototype sensor chips designed by the collaboration. The paper gives an overview of the main design aspects and performance evaluation results of the first two prototype chips RD50-MPW1 and RD50-MPW2, and details the design of the latest prototype RD50-MPW3. RD50-MPW2 is a small prototype with an 8 x 8 matrix of active pixels which implement analogue readout electronics only and solutions for low leakage currents. This prototype has been evaluated in the laboratory and also at proton and ion beam facilities, before and after irradiation with neutrons up to $2{\cdot}10^{15}$ n_{eq}/cm^2. RD50-MPW3 is a more advanced prototype with a matrix of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes. To alleviate routing congestion and minimise crosstalk noise, the pixels are serially configured and organised in a double column scheme. This prototype has optimised peripheral readout electronics for effective chip configuration, based on the I2C protocol, and fast data transmission.

1. Introduction

This paper presents results from the RD50-MPW series of monolithic CMOS sensors, developed by the CERN-RD50 collaboration to study this technology in view of the harsh requirements imposed by future hadron colliders on tracking systems [1]. The RD50-MPW sensors developed so far are in the 150 nm High Voltage-CMOS (HV-CMOS) process from LFoundry S.r.l. Parameters especially considered in this programme are radiation tolerance, time resolution and granularity.

2. Design and characterisation of RD50-MPW1 and RD50-MPW2

This section reviews the main design aspects and performance evaluation results of RD50-MPW1 and RD50-MPW2 to illustrate the background on which the current prototype, RD50-MPW3, lies. Fig. 1 shows the layout views of these three sensor chips. RD50-MPW1 has a matrix of 40 rows x 78 columns of high-granularity pixels where these integrate the analogue and digital readout electronics inside their area of 50 μm x 50 μm. The analogue readout, based on conventional electronics for charge-collecting detectors, includes a Charge Sensitive Amplifier (CSA) with continuous reset, low-pass and high-pass filters, and a CMOS comparator with a 4-bit Digital-to-Analogue Converter (DAC) to tune locally small threshold voltage variations. The digital readout is based on the well-known column drain architecture (i.e. FE-I3 style) [2]. It provides two 8-bit time-stamps, one for the leading edge and another one for the trailing edge, and an 8-bit address. When a pixel registers an event, it sends the leading and trailing edge time-stamps, and its address, to the corresponding End-Of-Column (EOC) circuit at the periphery through a 24-bit bus. This bus is shared by all the pixels within a column. The 78 EOC circuits of the matrix, which function as two 16-bit parallel-in parallel-out shift-registers, are connected to two readout serialisers designed to run at a maximum frequency of 640 MHz. RD50-MPW1 was fabricated in two high resistivity substrates with nominal values of 500 Ω cm – 1.1 kΩ cm and 1.9 kΩ cm.

The Data Acquisition System (DAQ) for the RD50-MPW sensor chips builds on the general-purpose Control and Readout (CaR) board [3]. It comprises a dedicated chip carrier board, the CaR board, an FPGA Mezzanine Card (FMC) and a Xilinx ZC706 or ZC702 evaluation board. The evaluation of fabricated RD50-MPW1 samples has revealed this chip essentially works, but also that it suffers from high leakage current in the sensing diodes, voltage drops across the pixel matrix and crosstalk noise between the lines that carry digital signals [4]. Several RD50-MPW1 samples have been irradiated with neutrons up to $2{\cdot}10^{15}$ n_{eq}/cm^2 at the TRIGA reactor in Ljubljana, Slovenia. The test structures of this chip, which consist of a small matrix of passive pixels, have been

E-mail address: vilella@hep.ph.liv.ac.uk.
[1] See https://rd50.web.cern.ch/ for full authors list.

https://doi.org/10.1016/j.nima.2022.166826
Received 21 November 2021; Received in revised form 13 April 2022; Accepted 22 April 2022
Available online 7 May 2022

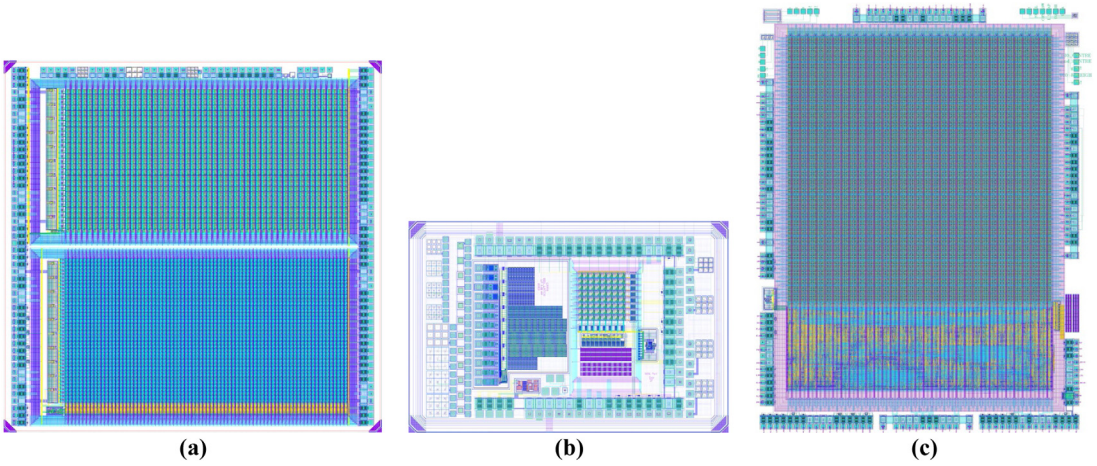

Fig. 1. Layout views of RD50-MPW1 (a), RD50-MPW2 (b) and RD50-MPW3 (c). The dimensions of these prototype sensor chips are 5 mm x 5 mm, 3.2 mm x 2.1 mm and 5.1 mm x 6.6 mm respectively.

evaluated with the edge Transient Current Technique (eTCT) using the Particulars measurement system [5,6]. The measurement results show the irradiation effects are compatible with those found in the literature [7].

RD50-MPW2, the successor chip, implements solutions to minimise the high leakage current observed in RD50-MPW1 and has a simple pixel matrix to test these. The solutions consist of a guard ring frame at the edge of the chip and the prevention of certain post-processing filling layers that involve conductive material. The guard ring frame has one n-type ring that acts as a current collecting ring and six p-type rings that control the termination of the lateral depletion of the sensing diodes, in addition to one p-type seal ring that protects the design from damage caused by the sawing process [8]. RD50-MPW1 has the p-type seal ring only. The matrix in RD50-MPW2 has 8 rows x 8 columns of 60 μm x 60 μm pixels with analogue readout only. The larger pixel size is due to the increase of the spacing between the p–n electrodes of the diode for a higher breakdown voltage (8 μm spacing in RD50-MPW2 as opposed to 3 μm spacing in RD50-MPW1). The matrix integrates two different flavours of readout electronics, with continuous and switched reset CSAs, optimised for short response times to resolve particles at high rates [9]. RD50-MPW2 was fabricated in the standard resistivity of 10 Ω cm and in three high resistivity substrates with nominal values of 500 Ω cm – 1.1 kΩ, 1.9 kΩ cm and > 2 kΩ cm.

RD50-MPW2 has been evaluated in the laboratory and also at proton and ion beam facilities. The prototype exhibited a leakage current of 100 pA/pixel (1 μA/pixel in RD50-MPW1), a breakdown voltage of 120 V (56 V in RD50-MPW1) and an Equivalent Noise Charge (ENC) better than 2 mV [10]. Given the capacitance of 2.8 fF of the calibration circuit for injecting a test charge into the amplifier, the ENC is therefore better than 50 e^-. The eTCT setup has been used to study the depletion depth of the test structures, integrated in RD50-MPW2 as a small matrix of passive pixels, after irradiation with neutrons to several fluence up to $2{\cdot}10^{15}$ n_{eq}/cm^2 [7]. The setup was also used, for the first time, to investigate the time-walk of the 8 x 8 active pixel matrix [11]. The eTCT measurements showed the depletion depth is 110 μm, while the time-walk is better than 10 ns at 200 e^- threshold voltage and from 2 ke^- collected charge and above. Both parameters were measured at 100 V substrate biasing and before irradiation. After irradiation to $5{\cdot}10^{14}$ n_{eq}/cm^2 the depletion depth is 90 μm and the time-walk is kept at approximately the same value as before irradiation. After irradiation to $2{\cdot}10^{15}$ n_{eq}/cm^2, the depletion depth is 60 μm. The uncertainty in the measurement of the depletion depth is of the order of 10% and not better than 5 μm. The proton test beams have been conducted at the Rutherford Cancer Centre in Northumberland, United Kingdom, and MedAustron in Vienna, Austria [12], and the ion test beam at the Ruđer Bošković Institute in Zagreb, Croatia. The main goal of the proton test beams was to evaluate the experimental setups, newly developed to enable synchronisation with other detectors and accept triggers, together with the sensor chip and a particle beam as well as to obtain initial measurement results. Both setups consist of a telescope made of one RD50-MPW2 sample and the CaR DAQ placed between two scintillators. At the Rutherford setup the trigger is taken from the comparator output of the sensor chip, the two scintillators are used to discard noise events and the data generated by the amplified and discriminated outputs are recorded using a DRS4 switched capacitor array digitiser [13]. At the MedAustron setup the telescope is triggered by the coincidence of the two scintillators and the data is recorded using a test beam firmware based on a First-In, First-Out (FIFO) memory that captures the Time-over-Threshold (ToT). Beam energies of 120 MeV (Rutherford) and 252.7 MeV (MedAustron) were used. The ToT was characterised at both test beams with the switched reset pixel flavour, for which a value around 30 ns is expected regardless of the charge collected by the pixel according to design simulations. While the switched reset pixel does not provide information about the signal amplitude, it was chosen for these measurements to validate the test beam setups. The measured ToT distribution peaks at 30 ns (Rutherford) and 35 ns (MedAustron). Fig. 2 shows the simulation of the analogue pixel output, from which the simulated ToT was calculated, and the ToT distribution measured at Rutherford. The analysis of the ion test beam at the Zagreb Ruđer Bošković Institute is ongoing. Table 1 summarises the main performance parameters of RD50-MPW2.

In spite of its success RD50-MPW2 has several design limitations, such as the small number of rows and columns of the pixel matrix, the lack of digital readout electronics to identify events and a very simple peripheral readout that makes certain types of measurements too slow or not possible. To give a specific example of the consequences of these limitations, in RD50-MPW2 only one pixel at a time can be read out and this has restricted its evaluation programme. The collaboration is currently developing a new prototype, RD50-MPW3, which integrates a larger and more advanced pixel matrix with new and optimised peripheral readout electronics to further study monolithic CMOS sensors.

3. Design of RD50-MPW3

RD50-MPW3 overcomes the limitations of RD50-MPW2 by extending the number of pixels in the matrix (64 columns x 64 rows), incorporating in the pixel area digital readout electronics based on the column drain architecture and adding optimised peripheral readout electronics for effective pixel configuration and fast data transmission. RD50-MPW3 includes as well a few dedicated test structures, mostly to characterise the diode current-to-voltage characteristics, depletion

Table 1
Main performance parameters of RD50-MPW2. All the values are measured at 100 V substrate biasing with 1.9 kΩ cm substrate resistivity samples (except where specified). CR stands for Continuous Reset pixel and SR for Switched Reset pixel. NC stands for Not Characterised.

Parameter	Value (before irradiation)	Value ($5{\cdot}10^{14}$ n_{eq}/cm^2, neutrons)	Value ($2{\cdot}10^{15}$ n_{eq}/cm^2, neutrons)
Breakdown voltage [V]	120	126[d]	136[e]
Leakage current [nA/pixel]	0.1	50[d]	60[e]
Depletion depth [μm][a]	110	90	60
ENC [e^-]	50	NC	NC
Time-walk (CR) [ns][b]	9	9	NC
ToT (CR) [ns][b]	110	120	NC
ToT (SR) [ns][c]	30	NC	NC

[a]Measured with a > 2 kΩ cm sample. A depletion depth of 118 μm was measured with a 1.9 kΩ cm RD50-MPW1 sample at a 100 V substrate biasing (estimated depletion depth from measurements, as breakdown voltage is around 56 V in this prototype).
[b]Measured at 200 e^- threshold voltage and 8 ke^- collected charge using an eTCT setup. Continuous reset pixels were chosen for this study as the comparator output signal scales with the signal size and can be used to measure the amount of input charge.
[c]Measured at proton test beams. Switched reset pixels were chosen as these have higher gain than continuous reset pixels.
[d]Measured after irradiation to $1{\cdot}10^{14}$ n_{eq}/cm^2. The values after $5{\cdot}10^{14}$ n_{eq}/cm^2 are expected to be very similar.
[e]Measured after irradiation to $1{\cdot}10^{15}$ n_{eq}/cm^2. The values after $2{\cdot}10^{15}$ n_{eq}/cm^2 are expected to be very similar.

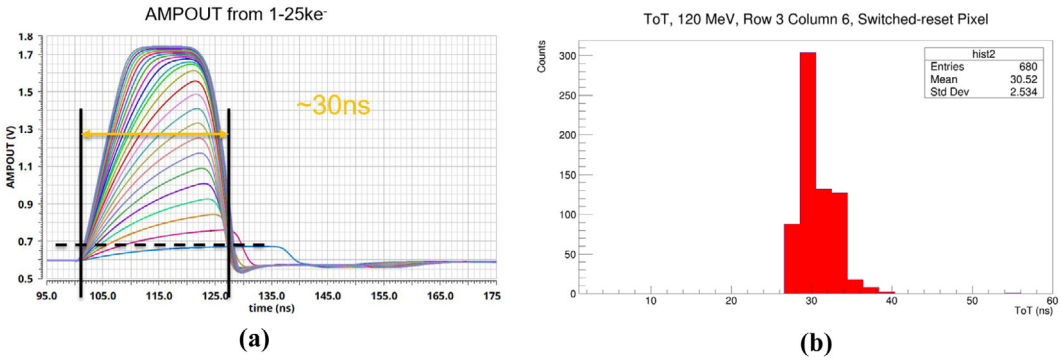

Fig. 2. The simulation of the analogue output gives a ToT of about 30 ns (a) and ToT measurement results show a distribution peaking at 30 ns (b).

depth and parasitic capacitance. RD50-MPW3 is being fabricated in three different substrate resistivities, which are the standard resistivity (10 Ω cm) and two high resistivities of 1.9 kΩ cm and 3 kΩ cm.

3.1. Pixel electronics

The RD50-MPW3 in-pixel digital readout is a highly improved version of that developed for RD50-MPW1. It incorporates logic to mask noisy pixels, replaces the priority circuit that determines the order in which hits are read out for a more compact alternative based on an OR chain, and allows pausing the digitisation of new hits until the readout of a column is complete. Each pixel contains as well a new 8-bit SRAM shift register, which enables serial configuration and stores a per pixel-trimming to compensate threshold voltage variations (four bits), a flag to mask noisy pixels (one bit), and data to enable or disable the calibration circuit (one bit), the amplifier output monitor (one bit) and the comparator output monitor (one bit). The configuration shift registers are programmed during the chip initialisation and hold the values indefinitely until the chip is reprogrammed or powered down. The analogue readout electronics reuse those developed for the continuous reset pixel of RD50-MPW2, as the laboratory and test beam evaluations showed their performance matches design specifications. Details about the diode implementation are available in [4]. Fig. 3 shows a simplified version of the pixel schematic. Fig. 4 shows a mixed-mode simulation using the post-layout view of a pixel that receives a test pulse from the calibration circuit.

3.2. Double column scheme

RD50-MPW3 implements a double column scheme for the first time in the RD50-MPW prototypes, which together with the also new 8-bit SRAM shift register for serial configuration, alleviates the routing congestion and facilitates means to minimise the crosstalk noise. Most of the routing area is occupied by a 24-bit bus with 8-bit Gray encoded time-stamps of the leading and trailing edges of the discriminator output as well the 8-bit address of the pixel. The double column scheme almost halves the number of necessary metal routing lines, as the pixels within a double column share most of the many metal routing lines they require. To enable that, the layout of the pixels is horizontally mirrored in every double column (i.e. analogue readout on one side and digital readout on the other side for one of the two columns, and vice versa for the other). To further prevent the generation of crosstalk noise, there is one metal routing line connected to ground between every two long metal routing lines that carry fast digital signals. The width of these metal lines, which are in metal 4, and the spacing between them is the minimum allowed by the design rules. The connections between the two pixels in a double pixel are in metal 3. To avoid noise coupling between the analogue and digital domains, the analogue and digital grounds are separated with a trench made of shallow n-well and deep n-isolation (called NISO in this process). The pixel size in RD50-MPW3 is 62 μm x 62 μm. This represents a small increase of the pixel size in RD50-MPW2 (60 μm x 60 μm), however it is necessary to accommodate all the new features here described while maintaining the breakdown voltage achieved in the previous prototype (8 μm spacing between the

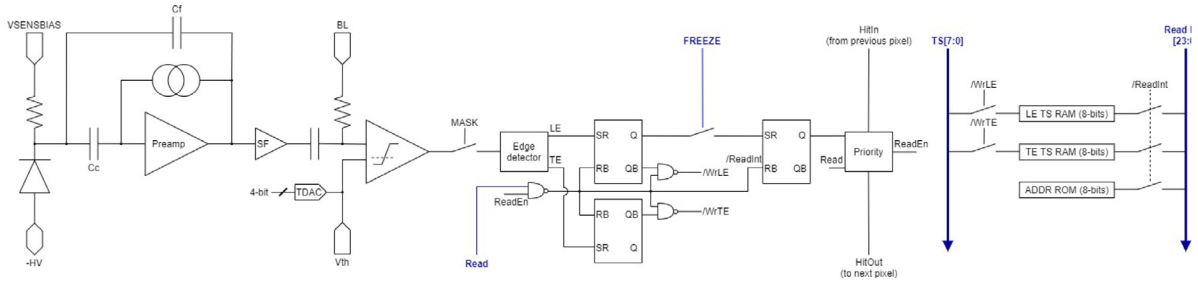

Fig. 3. Simplified schematic view of the RD50-MPW3 pixel including both the analogue and digital readout electronics.

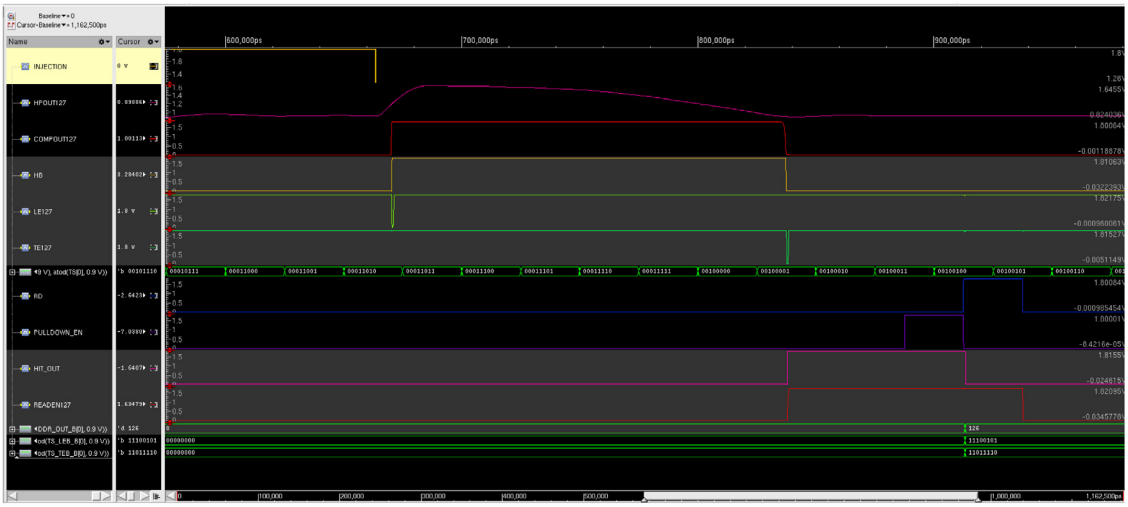

Fig. 4. Mixed-mode simulation using the post-layout view of a pixel: INJECTION is the test pulse from the calibration circuit; HPOUT the shaped signal at the comparator input; COMPOUT the comparator output; LE and TE the leading and trailing edges sensed by the digital readout electronics; TS the time-stamp; RD and PULLDOWN_EN digital signals sent to the pixel to store the pixel address and time-stamps in the corresponding EOC; HIT_OUT the output of the priority circuit connected to the following pixel in the double column; and READEN the output of the priority circuit connected to the digital readout of the pixel. The last three waveforms (figure bottom) correspond to the pixel address, and leading and trailing edge time-stamps.

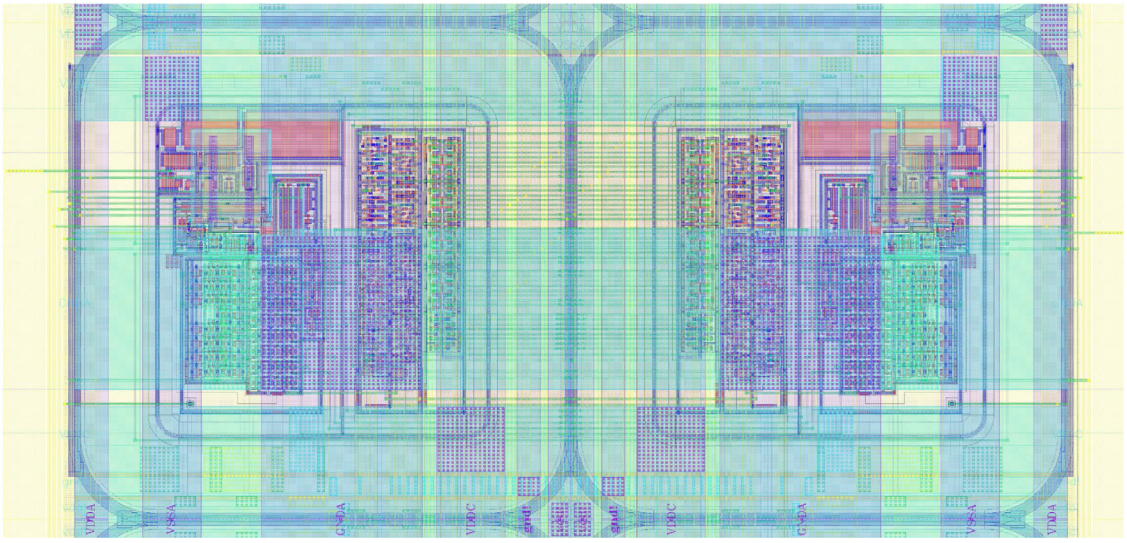

Fig. 5. Layout view of a double pixel. Explanations are given in the text.

p–n electrodes of the diode for a 120 V breakdown voltage). Fig. 5 shows the layout view of a double pixel. To avoid voltage drops in the power distribution, the pixel matrix incorporates a grid of wide metal lines in the highest possible metal layers (horizontal lines in

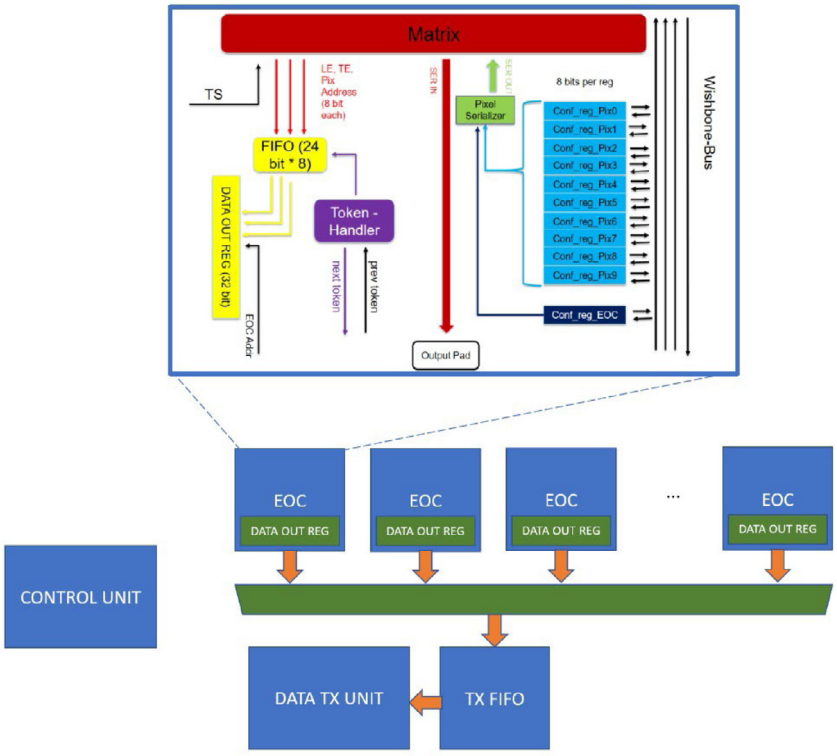

Fig. 6. Simplified block diagram of the peripheral readout electronics of RD50-MPW3.

metal 5, and vertical lines in metal 6). The metal grid is visible in the layout view of the double pixel. The pixels have four independent power domains, as the various sub-circuits in each pixel are powered separately, in addition to two ground domains.

3.3. Peripheral electronics

The peripheral electronics, which configure the pixels and control the data readout, consist of new and optimised EOC circuits, a Control Unit (CU) and a slow control system based on the I2C protocol for external communication using an internal Wishbone bus. There is one EOC circuit for every double column of pixels. The EOCs are handled by the CU. They use a FIFO memory to store, temporarily, the data generated by the pixels within a double column (i.e. leading and trailing edge time-stamps, and pixel address). This reduces the dead time, as pixels with hits are read out immediately as long as the FIFO is not full. The generated data is packed into frames, zero-suppressed and serialised at a maximum rate of 640 Mb/s, by a data transmission unit over Low Voltage Differential Signal (LVDS) lines. The readout of the pixel matrix is triggerless. All the peripheral blocks are configured through Control Status Registers (CSRs), which are connected to a Wishbone bus and read/written using an I2C interface. Fig. 6 shows a block diagram of the peripheral readout electronics.

4. Conclusion

This paper describes work done by the CERN-RD50 collaboration to study and develop the RD50-MPW series of monolithic CMOS sensors in the 150 nm HV-CMOS process from LFoundry S.r.l. RD50-MPW2 has been designed and evaluated both in the laboratory and also at proton and ion beam facilities. The prototype exhibited a leakage current of 100 pA/pixel, a breakdown voltage of 120 V and an Equivalent Noise Charge (ENC) better than 50 e^-. The eTCT measurements showed the depletion depth is 110 μm, and the time-walk is better than 10 ns at 200 e^- threshold voltage and from 2 ke^- collected charge and above. After irradiation to $5{\cdot}10^{14}$ n_{eq}/cm^2 the depletion depth is 90 μm and the time-walk is kept at approximately the same value as before irradiation. After irradiation to $2{\cdot}10^{15}$ n_{eq}/cm^2, the depletion depth is 60 μm. The test beam measurement results show a ToT distribution peaking around 30 ns and are in good agreement with simulated results. RD50-MPW3 is a more advanced prototype, with a matrix of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes, and optimised peripheral readout electronics for effective chip configuration and fast data transmission. This chip is currently being fabricated.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

This work has been partly performed in the framework of the CERN-RD50 collaboration. It has received funding from UK Research and Innovation (UKRI) under the grant reference MR/S016449/1, and from the European Union's Horizon 2020 Research and Innovation programme under grant agreement 101004761 (AIDAinnova).

References

[1] M. Benedikt, et al., Future Circular Collider, Vol. 3: The Hadron Collider (FCC-hh), CERN-ACC-2018-0058, 2018.
[2] I. Peric, et al., The FEI3 readout chip for the ATLAS pixel detector, Nucl. Instrum. Methods Phys. Res. Sect. A 565 (2006) 178.
[3] H. Liu, et al., Development of a modular test system for the silicon sensor R & D of the ATLAS Upgrade, arXiv:1603.07950v4 [physics.ins-det].
[4] E. Vilella, Recent depleted CMOS developments within the CERN-RD50 framework, PoS (Vertex2019) 019.

[5] G. Kramberger, et al., Investigation of irradiated silicon detectors by Edge-TCT, IEEE Trans. Nucl. Sci. 57 (2010) 2294.
[6] Particulars, Advanced measurement systems, Ltd. www.particulars.si.
[7] I. Mandić, et al., Study of neutron irradiation effects in Depleted CMOS structures, arXiv:2112.10738v1 [physics.ins-det].
[8] J. Liu, Study of a Monolithic Pixel Detector for the ATLAS Tracker at the High Luminosity LHC (PhD thesis), Aix-Marseille University, Marseille, 2016.
[9] C. Zhang, et al., Development of RD50-MPW2: A High-Speed Monolithic HV-CMOS Prototype Chip Within the CERN-RD50 Collaboration, PoS (TWEPP 2019) 045.
[10] R. Marco, Latest depleted CMOS sensor developments in the CERN-RD50 collaboration, in: JPS Conf. Proc. Vol. 34, 2021, p. 010008.
[11] B. Hiti, et al., Characterisation of analogue front end and time walk in CMOS active pixel sensor, J. Instrum. 16 (2021) P12020.
[12] P. Sieberer, et al., Readout system and testbeam results of the RD50-MPW2 HV-CMOS pixel chip, arXiv:2201.08585v1 [physics.ins-det].
[13] S. Ritt, Design and performance of the 6 GHz waveform digitizing chip DRS4, in: 2008 IEEE Nuclear Science Symposium Conference Record, 2008, pp. 1512–1515, http://dx.doi.org/10.1109/NSSMIC.2008.4774700.