
LHCb Upgrade II

Karol Hennessy

on behalf of Eva, Sigrid, Ashley, Jan, Ayushi, Tara, Kurt, Kieran

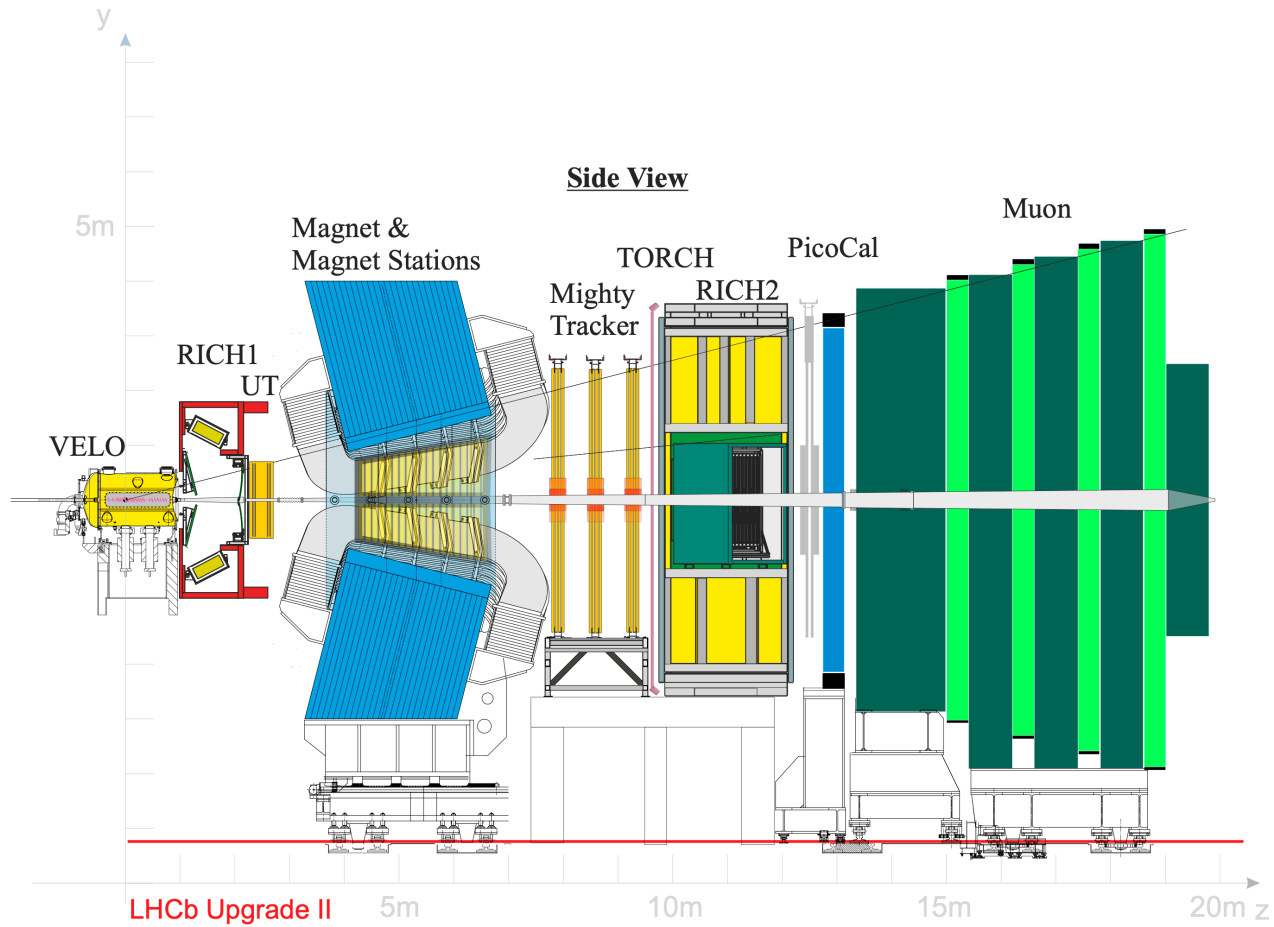
2024-05-24



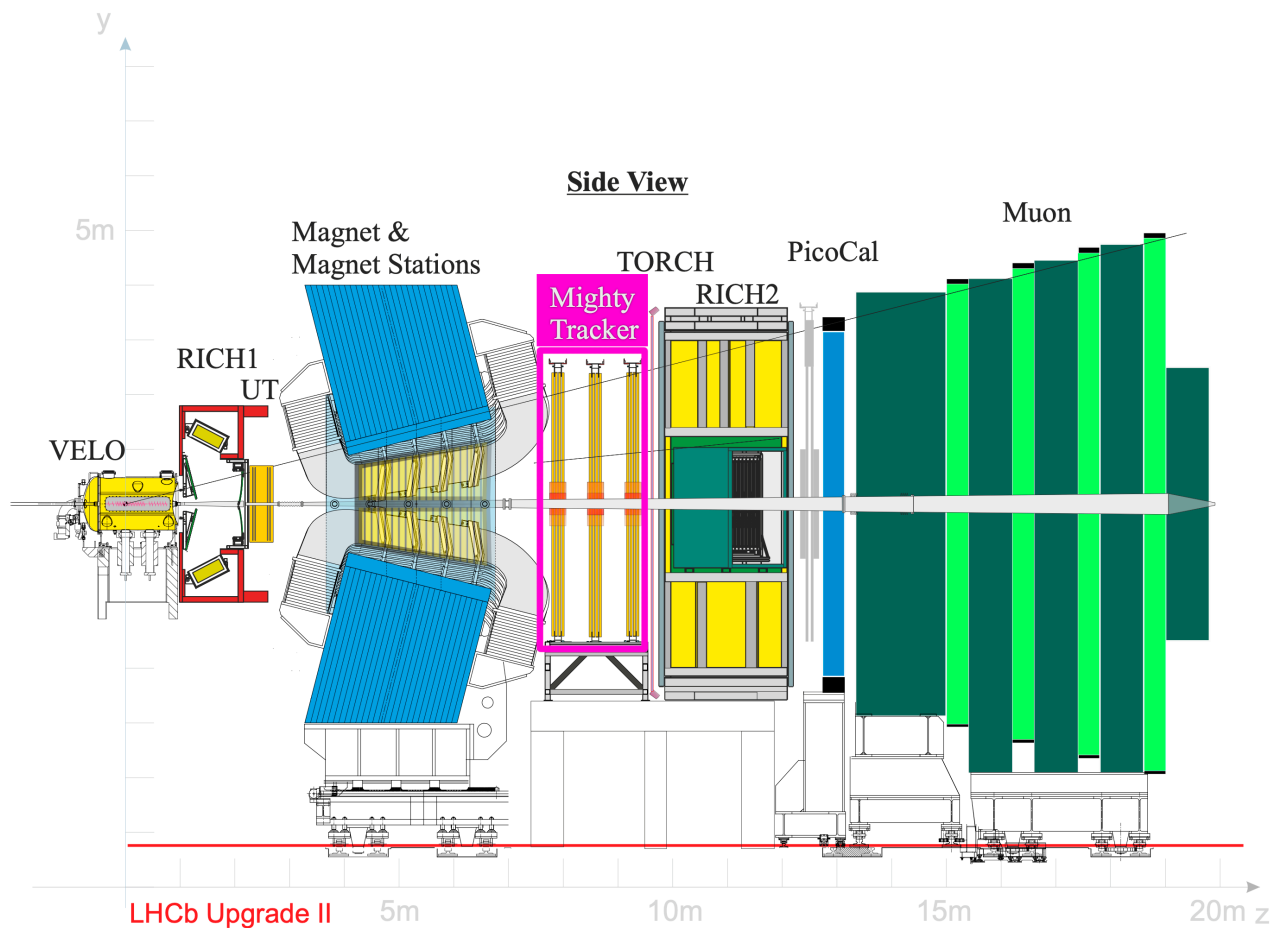
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LIVERPOOL

LHCb
ГНСП

LHCb Upgrade II



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LHCb Upgrade II

- Physics programme limited by detector, NOT by LHC
- Therefore, we should **upgrade to get the maximum physics LHC can deliver**

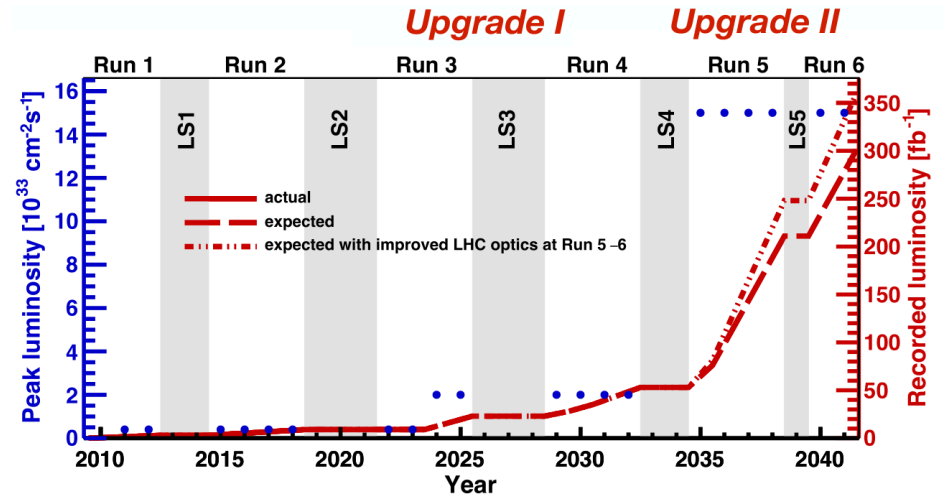
Upgrade I

- $L_{peak} = 2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$

Upgrade II

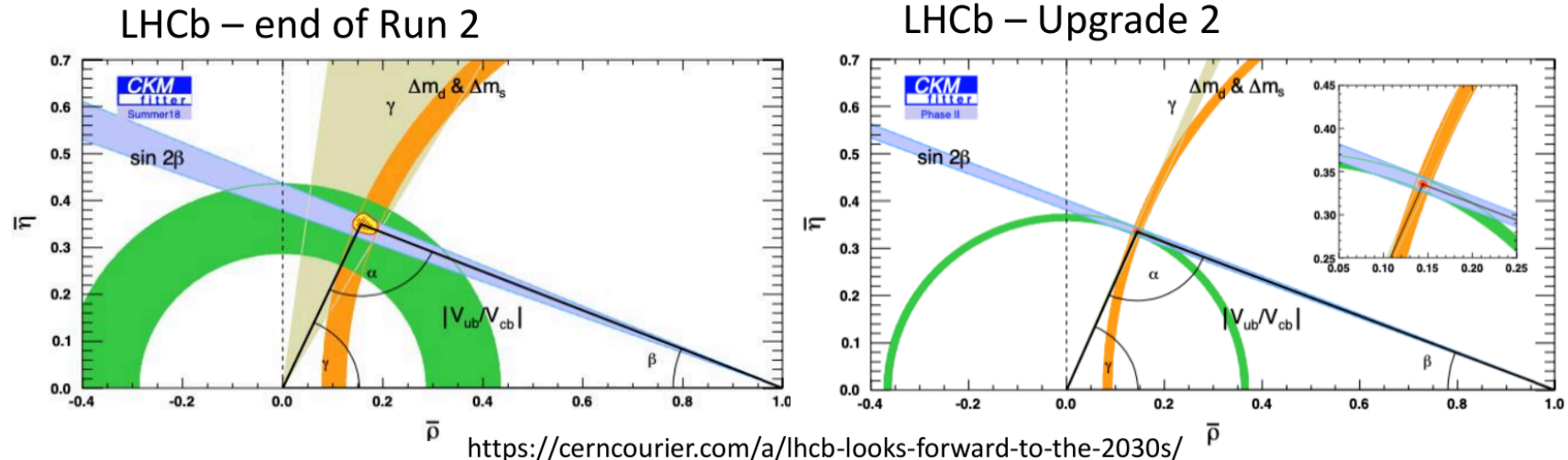
- $L_{peak} = 1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
- $L_{int} = 300 \text{ fb}^{-1}$ during Runs 5 & 6.

Installation in LS4



Upgrade II motivation

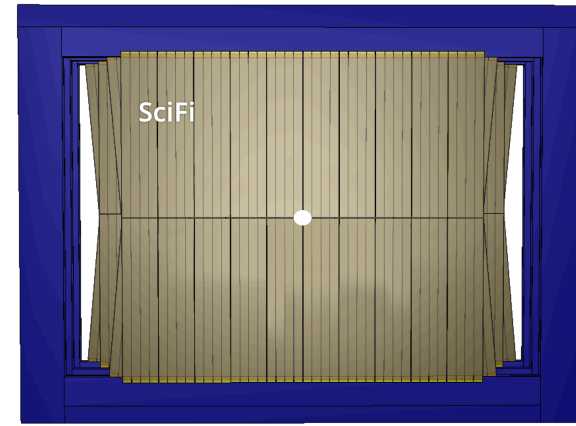
- Sensitivity to mass scales several orders of magnitude above those within reach of direct production measurements at the energy frontier
- Numerous **key observables** have negligible theoretical uncertainty
- Test of **CKM matrix to unprecedented accuracy**
- Flavour sector has arguably a *great likelihood* for discovery at HL-LHC



Mighty Tracker

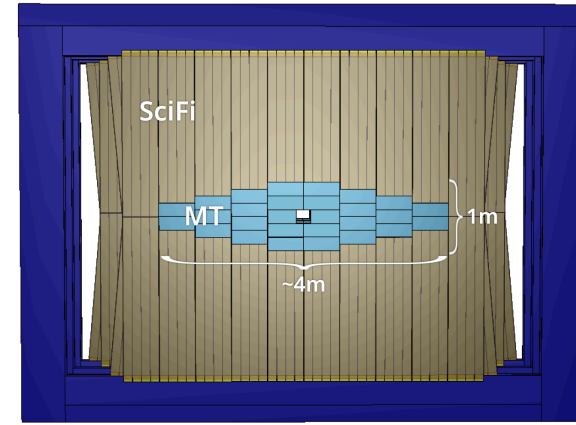
Mighty Tracker

- Scintillating Fibre (**Sci-Fi**) outer tracker
- To cope with the **increased pile-up** replace the inner section with a silicon pixel detector
- 6 layers
- Mighty Tracker is required to be
 - low-mass
 - cooled below 0°C
 - have modest spatial resolution



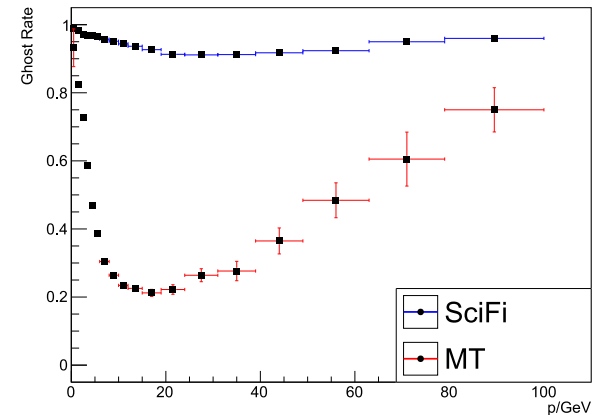
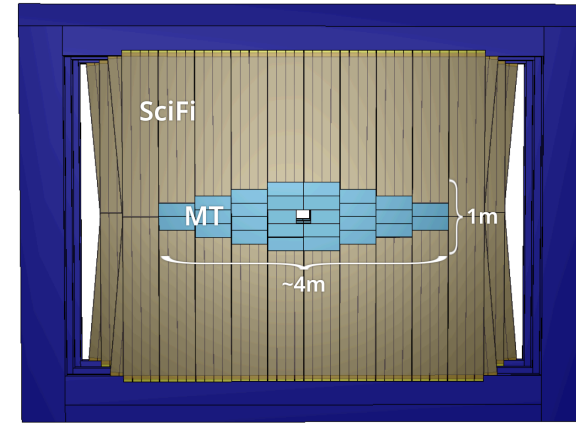
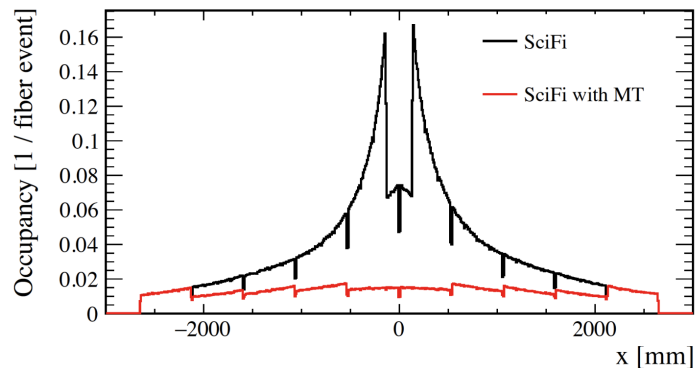
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Mighty Tracker

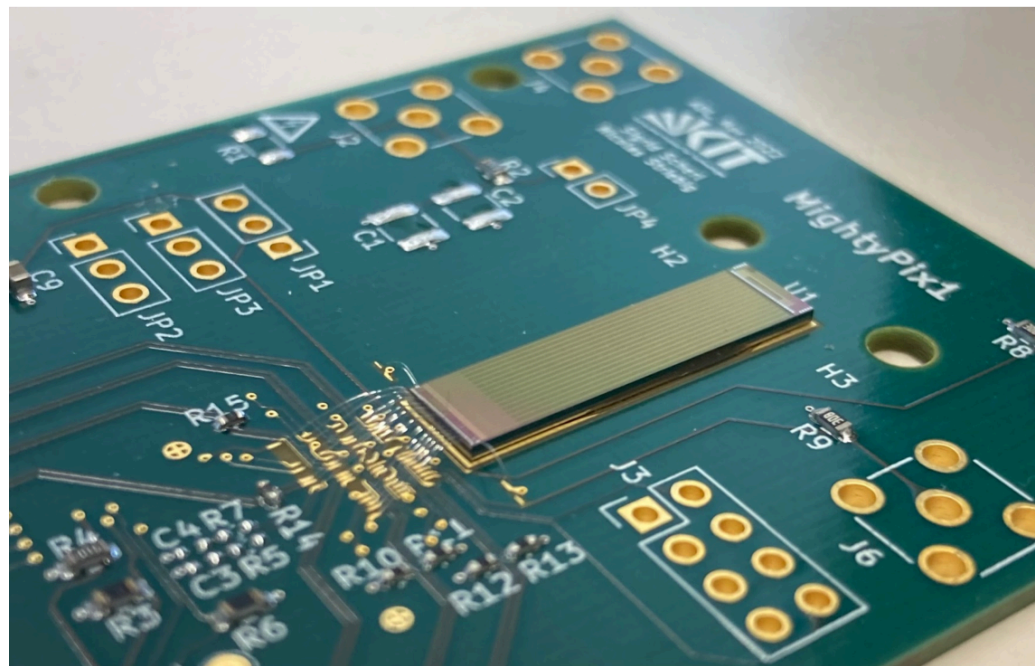
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MightyPix

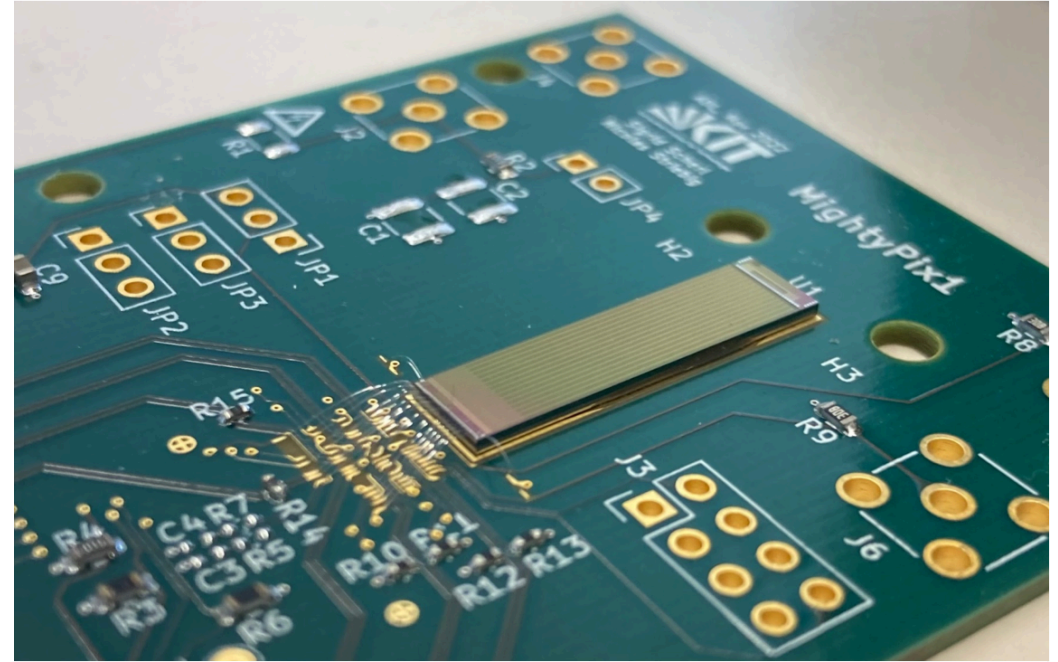
MightyPix

- This time last year we had defective MightyPix v1
 - Tried to repair with **Focused Ion Beam** surgery - failed
 - Tried again with a different company - success !
- Found some other issues
 - synchronisation, wrong timestamping, missing shielding
 - Compiled a series of “lessons learned”
- But **we can still test!** :)



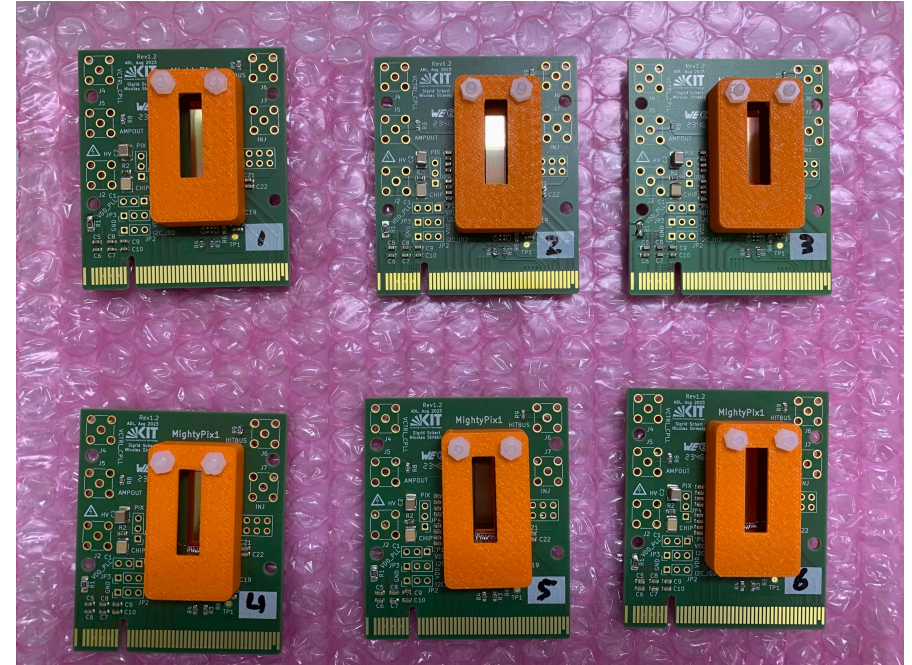
MightyPix

- Suspension of TSI 180 nm CMOS process
 - Search for a new foundry
 - Primary candidates **AMS** and **LFoundry**
 - Submitted to LFoundry in April (with guard rings developed by RD50)
 - We have experience with both
- Will also submit to AMS
- Need to **submit MightyPix 2 in 2025**



MightyPix v1 Testing

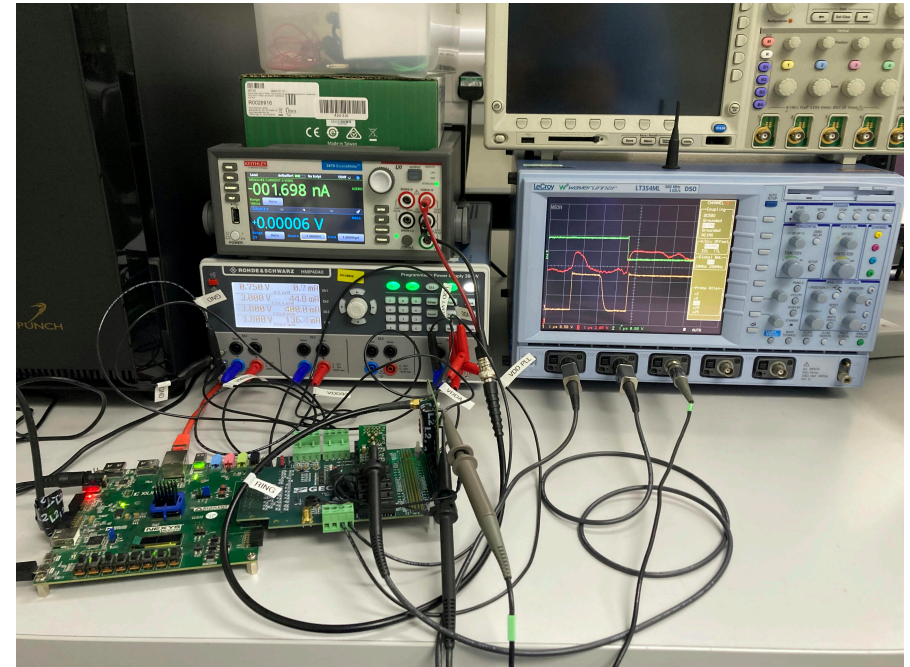
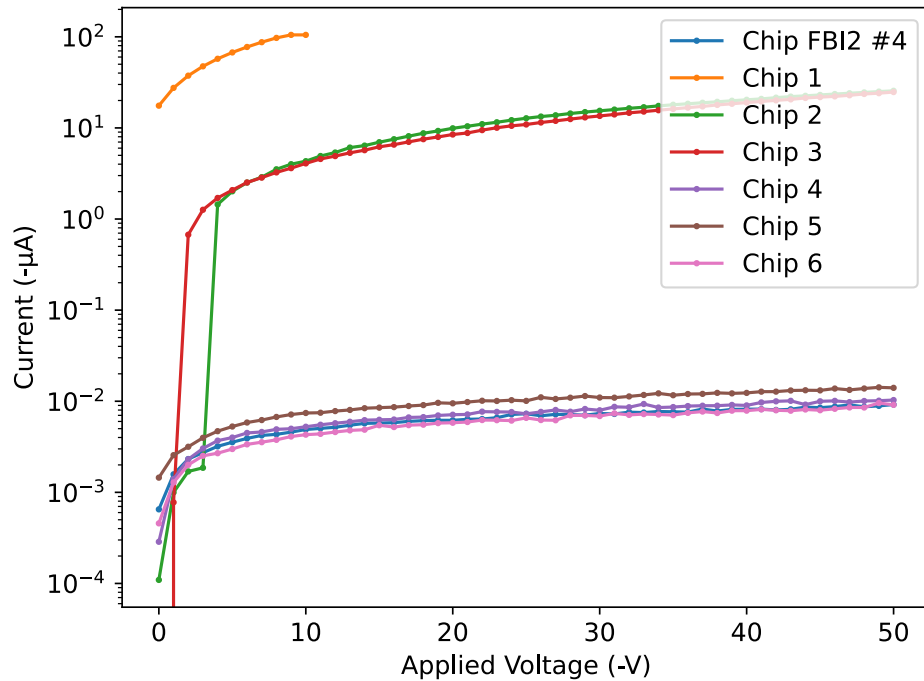
- 6 FIB'd MightyPix v1's tested at Liverpool
- checked configuration and leakage current



MightyPix v1

MightyPix v1 Testing

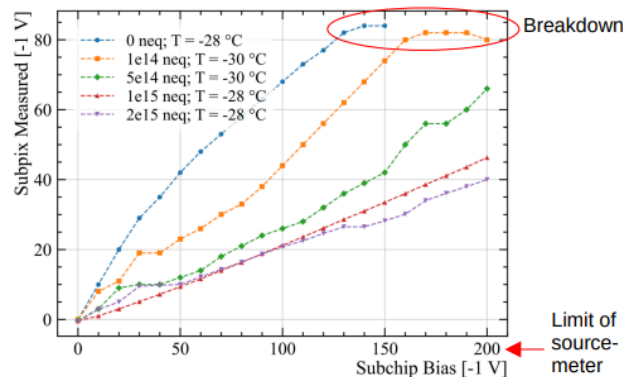
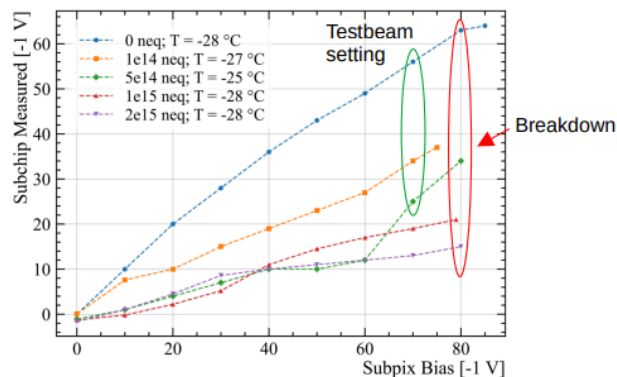
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MightyPix v1 test stand in LSDC

- distributed to UK sites

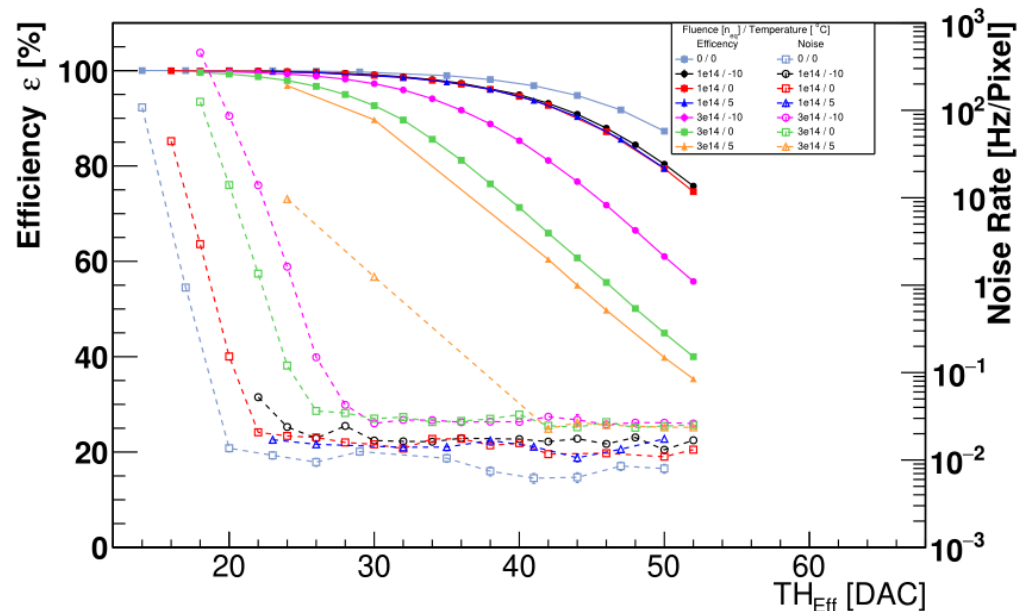
- DESY: 11th-24th March 2024
- Under test:
 - Telepix (MightyPix' cousin)
 - irradiated ($1 \times 10^{15} n_{eq}$) and unirradiated
 - MightyPix v1 unirradiated



– wrong bias scheme, being revised

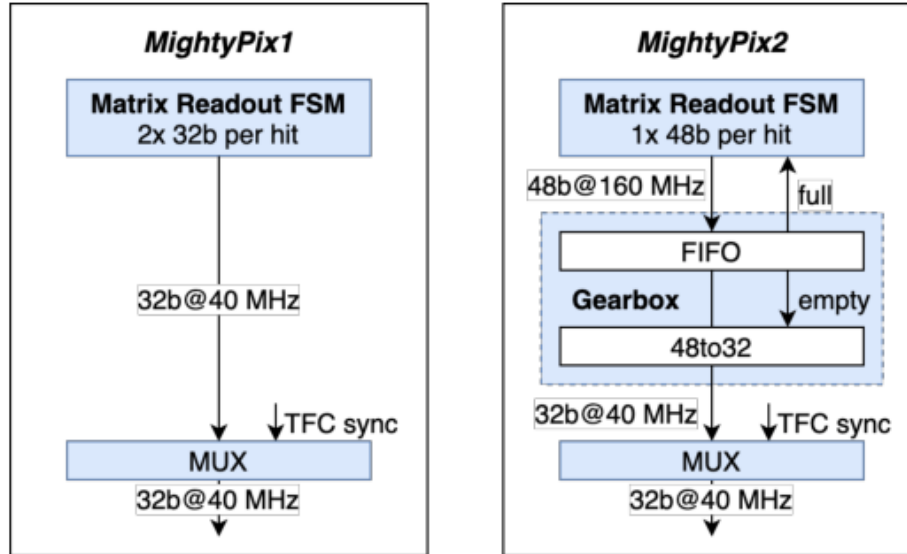


- Studies of ATLASPix 3.0 and 3.1
 - more MightyPix cousins
 - several irradiations
 - significant degradation beyond $3 \times 10^{14} n_{eq}$
- Improved understanding of previous testbeam data
- **Congratulations to Jan on passing his viva :)**

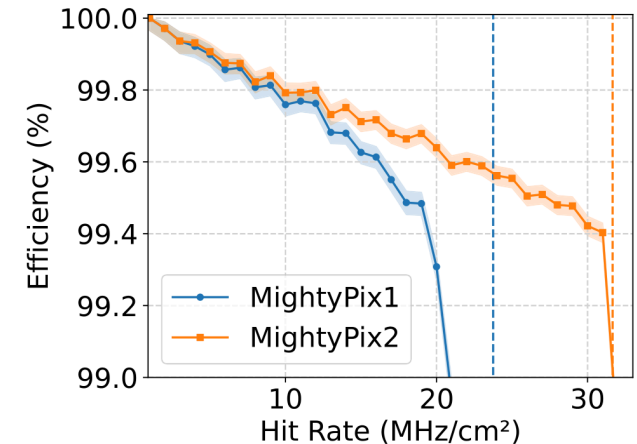
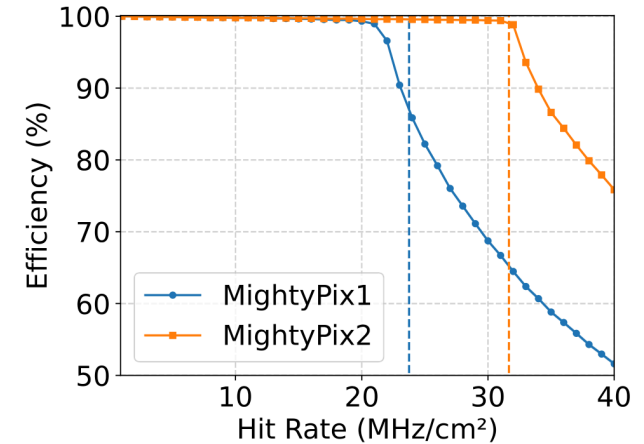


Design optimisation and prototyping

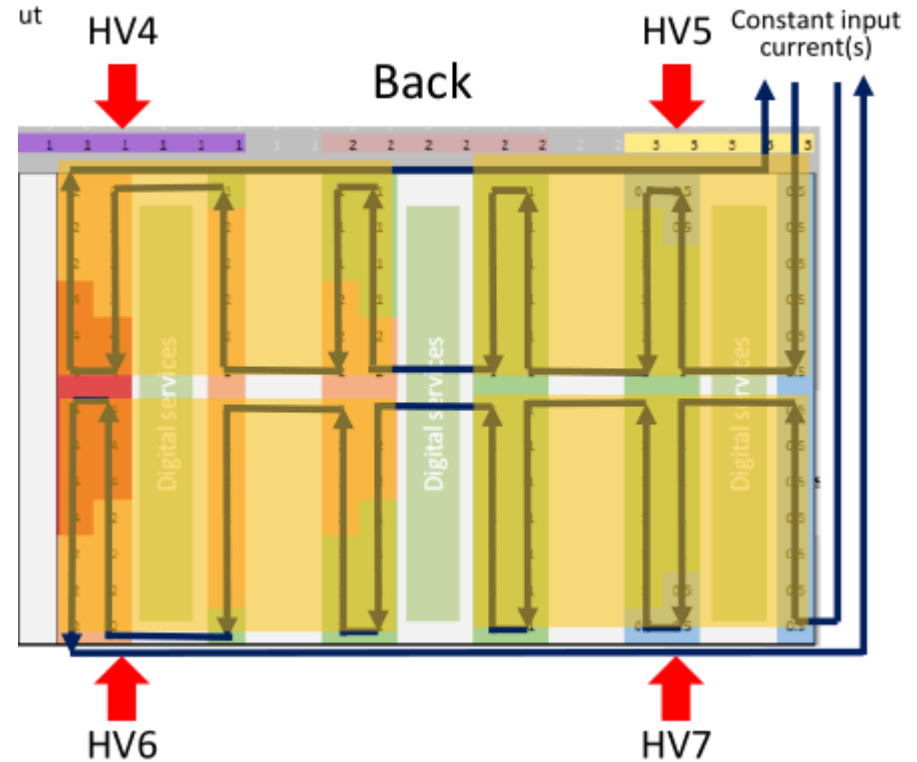
MightyPix Efficiency Improvements



- Improvements to readout FSM
- MightyPix 2 hit rate efficiency above 99.5% @ 30 MHz/cm² (former limit 20 MHz/cm²)
- Trying to replicate tests with MightyPix 1 in the lab

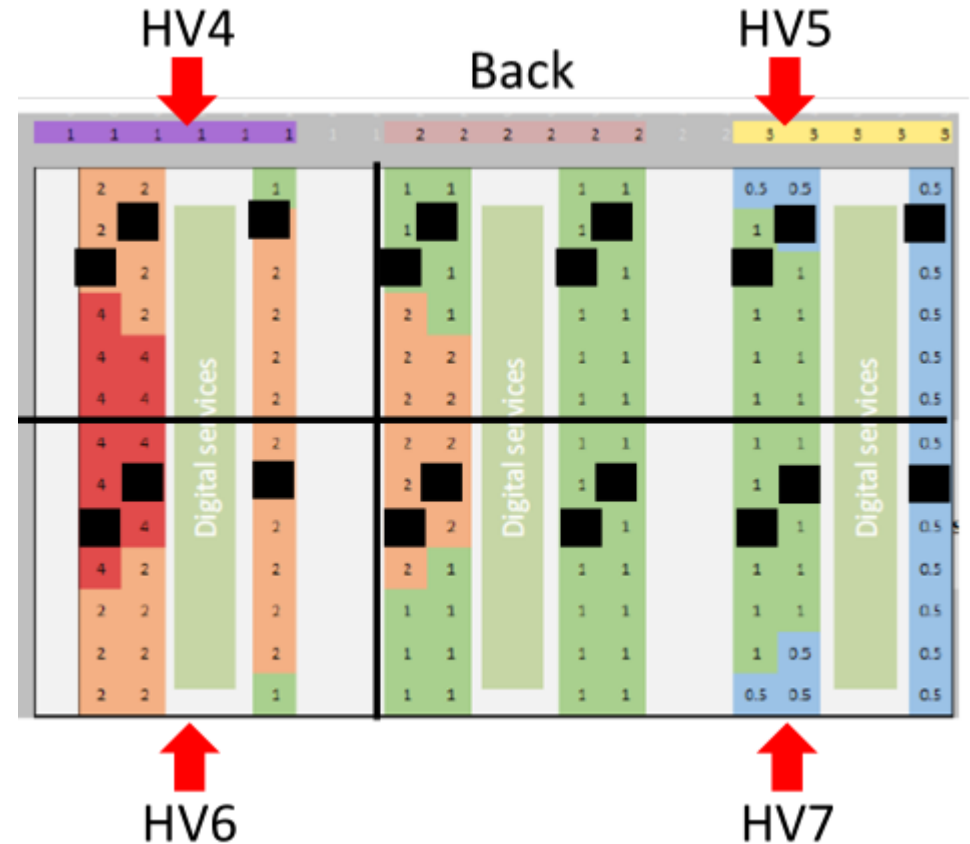


- HV to be distributed across many sensors
- Examining different routing schemes
- **How to improve redundancy?**
 - add HV switch per submodule flex
 - reduce loss of sensors from 42 to 7(6)
 - Closely following ATLAS ITk work



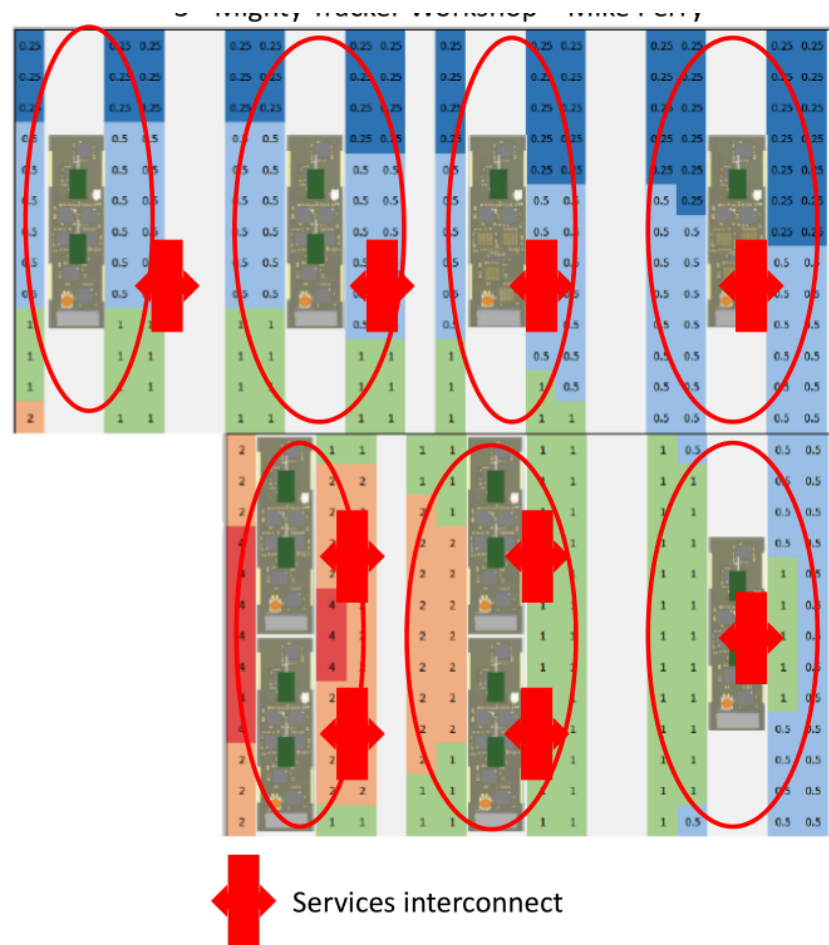
Example HV routing

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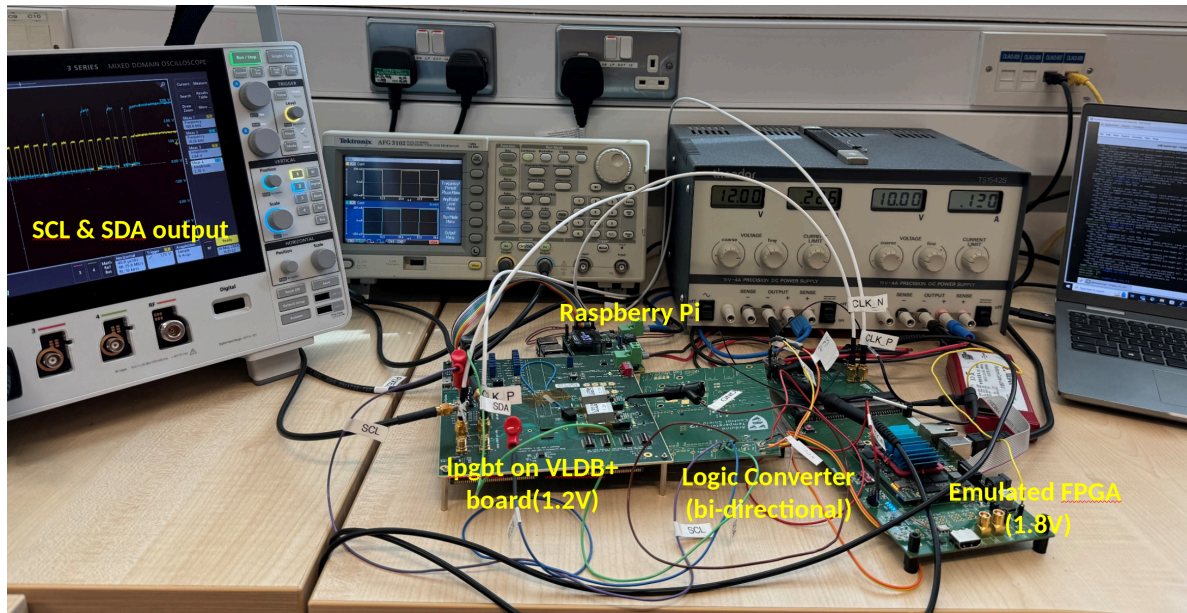


HV Switches in black

- Serial Powering now considered default
 - Saves space on service boards
 - Reduces material
- Locked to service boards
- To be included in MightyPix 2
- Several design iterations on hybrids/modules for optimal layout - nothing final yet
- Have 3 ATLASPix samples
 - use to gain experience with Serial Powering

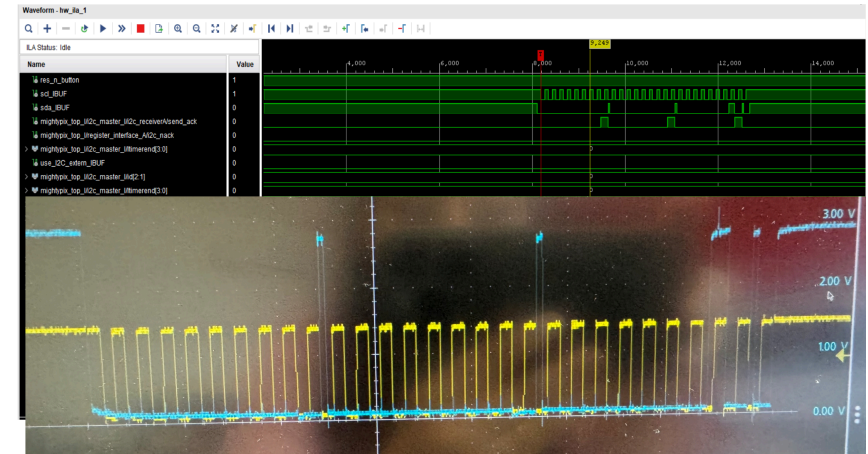


- Idea: use an FPGA to emulate MightyPix
 - Test digital functionality
- Connect to VLDB+ and talk to MightyFPGA over I²C



VLDB+ & MightyFPGA setup

- Successfully managed to talk to MightyFPGA over I²C and configure and read back internal registers



Communication from IpGBT to MightyFPGA

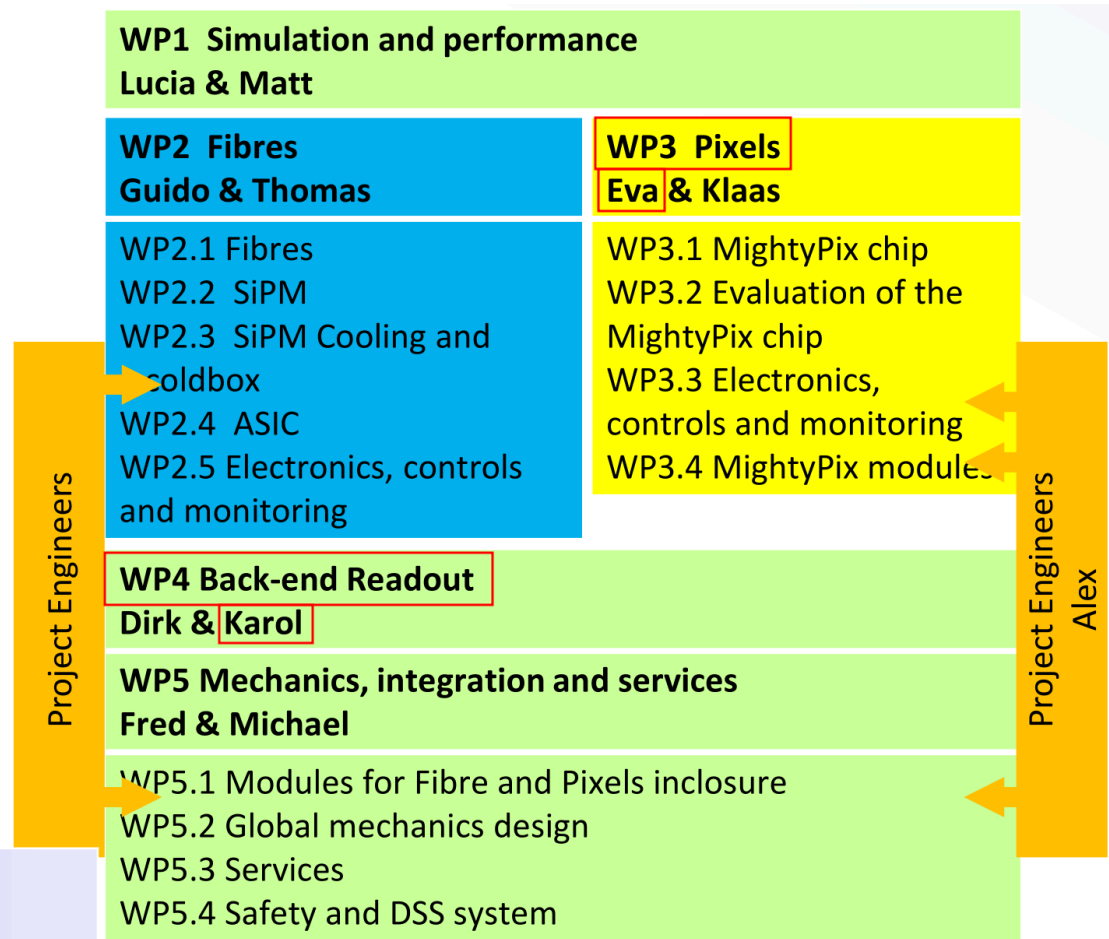
Coordination

Weekly meeting of Extended Coordination team:

- ✓ WP0: Blake, Fred, Matt & PP
- ✓ WP1: Lucia (& Matt)
- ✓ WP2: Guido & Thomas
- ✓ WP3: Eva & Klaas
- ✓ WP4: Dirk & Karol
- ✓ WP5: Michael (& Fred)
- ✓ Project engineers: Alex & ?

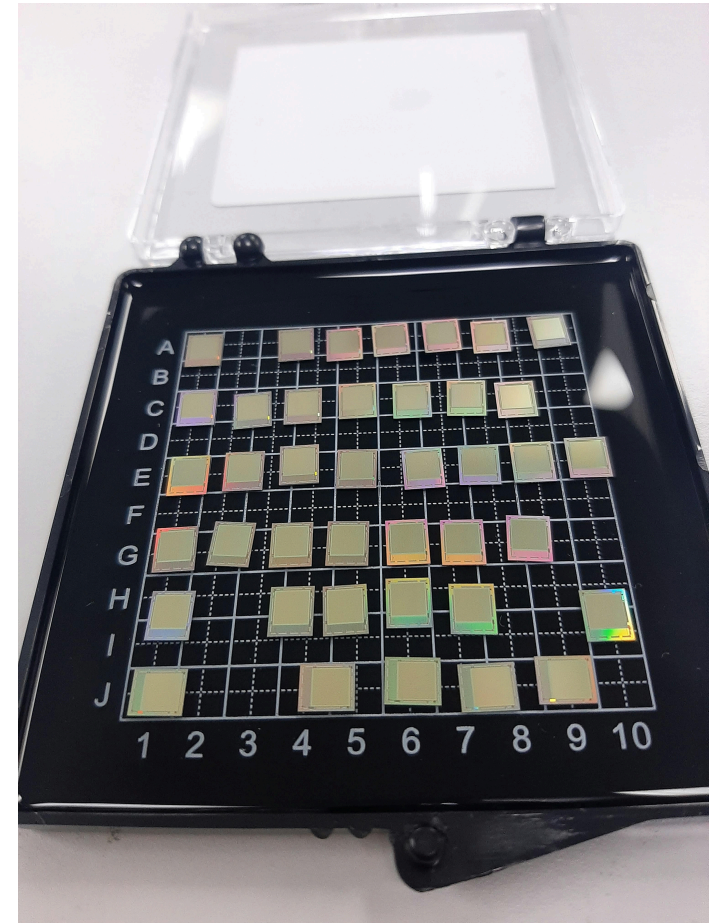
WP0 Coordination

Pascal, Blake & U2 Coordinators Fred & Matt

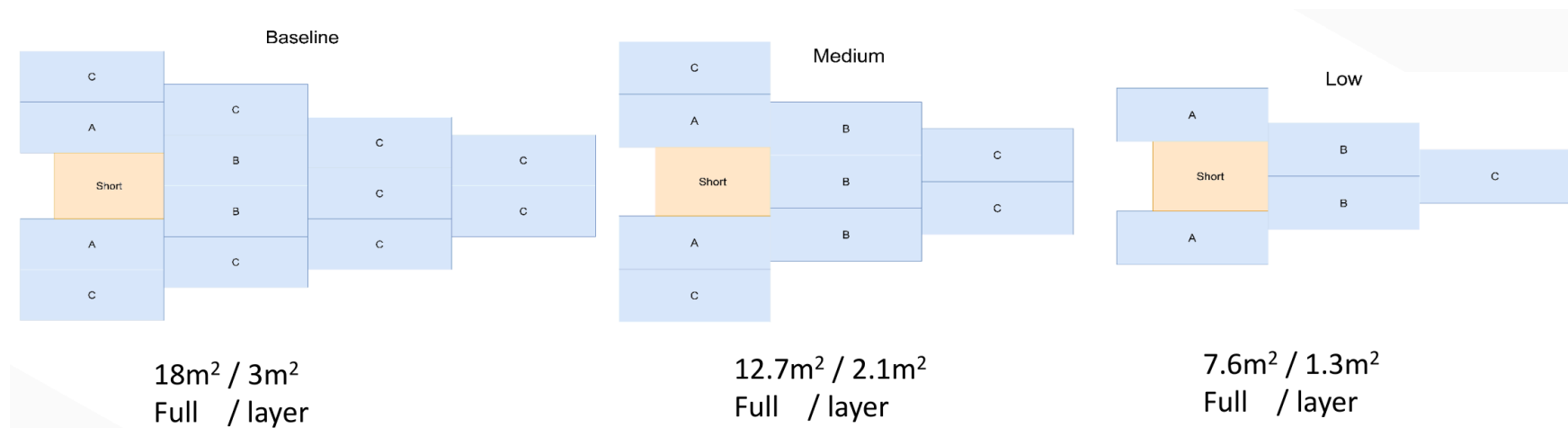


Recent developments...

- Forming a working group to **develop a high radiation tolerant MightyPix type chip** in LFoundry
- Capitalise on recent advancements achieved through CERN-RD50
 - **RD50-MPW4 chip - Liverpool design**
 - small pixel
 - high radiation tolerance
 - for more details see Jan's talk
- We will make the chip for the Mighty Tracker but **also for the UT.**
- **Kick-off meeting in June** with essentially Liverpool, RAL and the UT.



Scoping



- Feb. had to submit a scoping document for Upgrade 2 with scenarios for 100%, 85%, 70% cost.
- Likely result: reduction in silicon area; reduce DAQ margins

Writing the scoping document was great fun, and not boring!"
— No-one Ever

4th Mighty Tracker Workshop at Liverpool

2–4 Jul 2024
126 Mount Pleasant, Lecture Theatre 113
Europe/Zurich timezone



Overview

Timetable

Registration

Participant List

Contact

- ✉ vilella@hep.ph.liv.ac.uk
- ✉ A.J.Reid@liverpool.ac.uk
- ✉ hannah.melia@liverpool...

The workshop will be held at Liverpool

It will start on **Tuesday 2nd July** in the morning and will end on **Thursday 4th July** in the afternoon.

The workshop will be held **in-person on the University campus in the Liverpool city centre**. The room is [Lecture Theatre 113 at 126 Mount Pleasant \(map\)](#). Remote attendance (via zoom) will be arranged for those who cannot travel, but attendance in person is highly encouraged.

Registration is now open with deadline of 23rd June. You are kindly asked to register quickly and indicate whether you will be attending in person.

A workshop dinner will be held on Wednesday 3rd. Participants are expected to pay directly for their dinner. Further information will be provided at a later date.

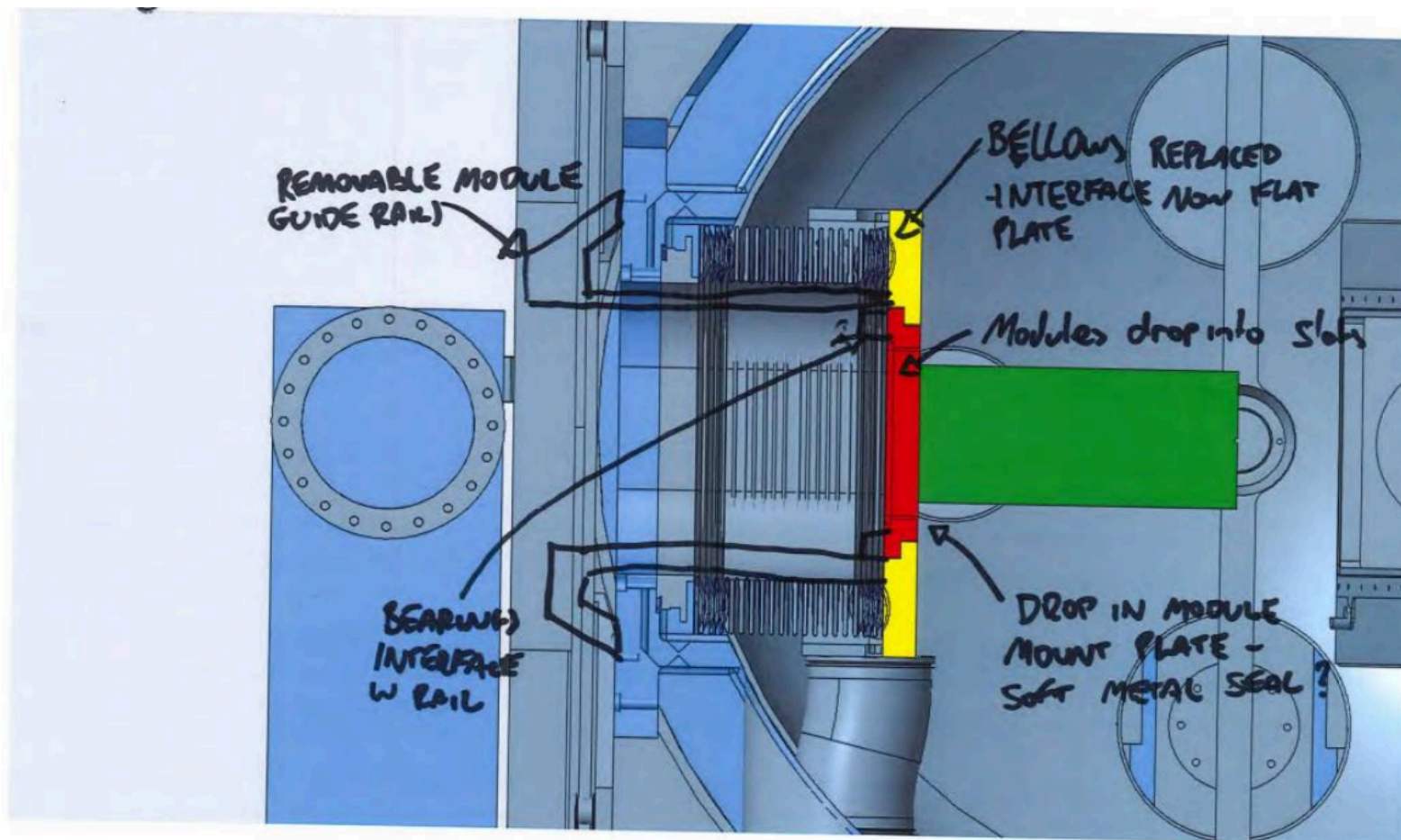
There is no registration fee, but registration is required for everyone attending to determine the number of participants (size of the room) and participation to the workshop dinner.

Travel to Liverpool



VELO U2


- Current radiation damage estimates mean upgrade 2 VELO modules unlikely not survive the lifetime of the experiment
- Kieran developing the **mechanics for a replacable module system**
 - Top level design requirement
 - Possibility to upgrade modules
- Challenges:
 - contamination; radiation exposure; cooling, power, electronic connections...

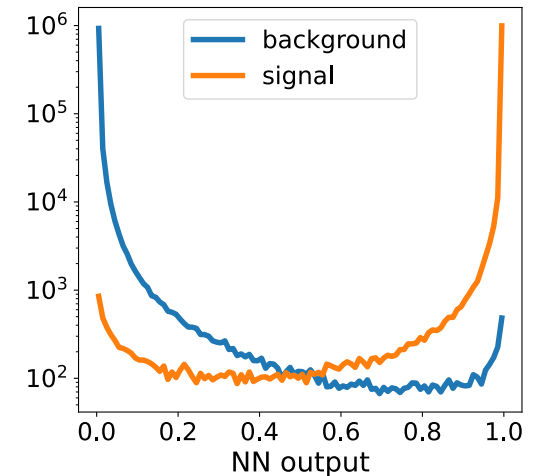
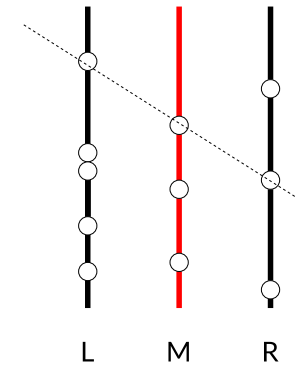


Data Processing for U2

ML Tracking on FPGAs

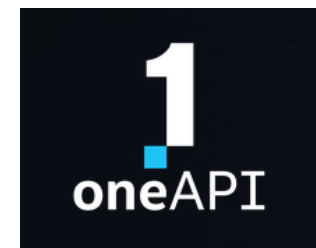
Kurt Rinnert, Karol Hennessy

- Use LHCb VELO as a test-bed.
- Connect the dots
 - Take 3 detector planes (Left, Middle, Right)
 - **make all combinations of triplets from hit clusters**
 - **choose the “best” triplet**
 - Train the machine on LHCb MC data
- NN developed using  PyTorch
- **Port the resulting models to FPGA**
- Performance: high efficiency ~ 92%, purity ~ 97%, low ghost rates



oneAPI framework

- Write code in **C++** and **SYCL** (Data Parallel C++)
- Verify and Deploy to accelerator (GPU, FPGA)
- *Open Standard*
- **In four months, we managed to put the triplet finding algorithm on the FPGA, and verify the results**
- Next:
 - optimising for throughput
 - Integrate with existing DAQ workflow
 - compare to GPU
- Overall impression: Despite a few small annoyances, the framework is very powerful. **Potential to open FPGA programming to software developers**



BittWare IA-840f FPGA card

Thanks for listening!

PS... a vote for reinstating the Christmas meeting



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Pro	Con
People aren't on holidays, they already have one at the end of the month	Bah humbug!
Fewer conferences	
Students/LTAs get to travel home for winter break (cost saving)	
It's at a known time of year (not announced with 2 weeks notice)	
Christmas jumpers	

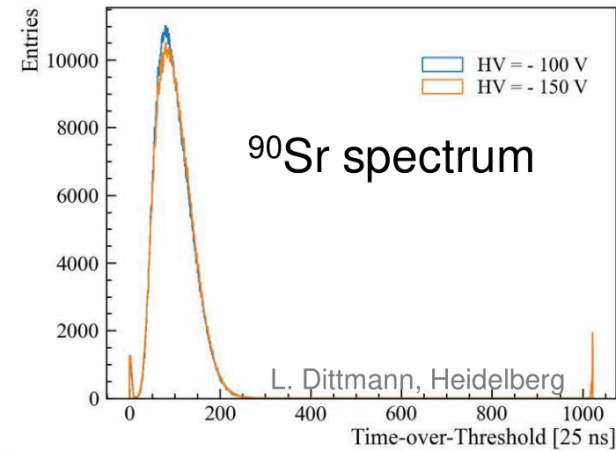
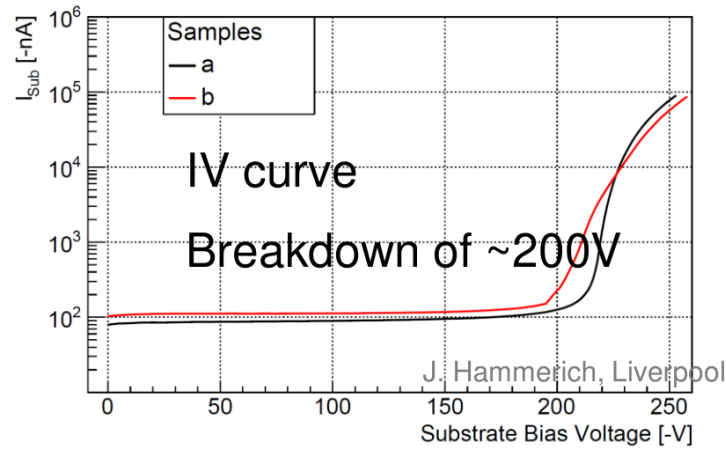
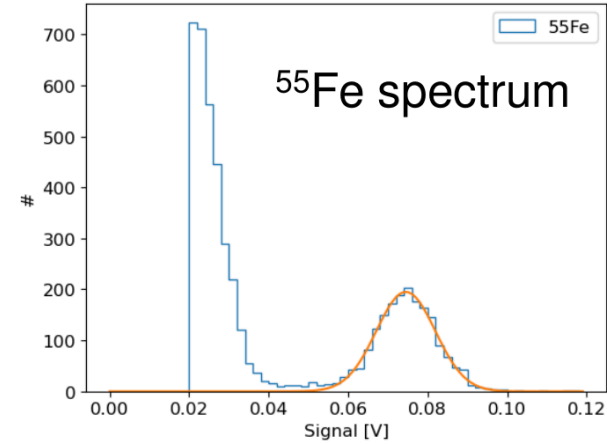
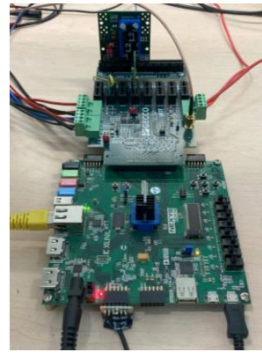
Backup

MightyPix

- The Mighty Tracker design centres around a new chip - **MightyPix**
- Based on knowledge from **ATLASPix** and MuPix
- **TSI 180 nm** process
- **HV-CMOS**: Sensing element and readout circuit on same chip

Requirements

Pixel size	$< 100\mu m \times 300\mu m$
In-time efficiency	$> 99\%$
Radiation tolerance	$6 \times 10^{14} \cdot 1MeVn_{eq} / cm^2$



MightyPix v1 lessons learned

- configuration problem
 - missing load signal ; analog config not possible
 - workaround : FIB surgery
 - lesson : check coverage, improve testing
- synchronisation problem
 - no proper communication possible between modules
 - modified model files
 - workaround : power cycle chip
 - lesson: use design defaults

MightyPix v1 lessons learned

- Timestamp wrong
 - workaround: BXID reset before 4095
 - unit test all submodules
- Missing shielding
 - causes coupling between adjacent columns
 - workaround: increase threshold voltage, reduced time resolution
 - lesson: formal checklist and DRC error signoff