UKRI-MPW1: Design and Preliminary characterisation Of An HV-CMOS Sensor For High Radiation Tolerance

Benjamin Wade

Supervisors: **E. Vilella-Figueras**

J. Vossebeld

Christmas Meeting
3rd Year

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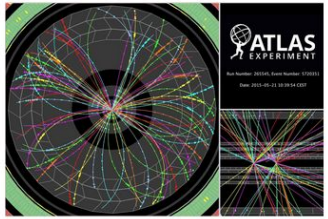
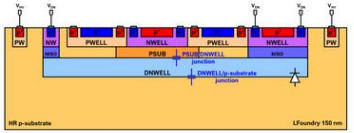
Recap

HV-CMOS
Motivations And Such





Placed close to collision center	→	Sensors receive high radiation dose
High rate of events MHz-GHz rate of bunch crossings	→	Fine spatial resolution required Good time resolution
Minimal track disruption	→	Thin sensors
Higher collision energies	→	More radiation, finer detail needed

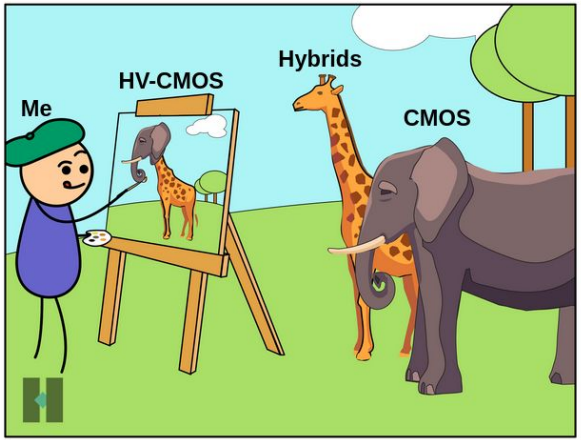
Integrated Readout Circuitry:
- ✔ Thin sensors
- ✔ Industrial standard
- ✔ Cost effective

High Voltage Pixel:
- ✔ More radiation tolerant
- ✔ Fast charge collection (Drift)

Sensors need to be thin, fast, radiation tolerant, and within budget

DISCLAIMER: I do not work for ATLAS, this is just an example

HV-CMOS
Motivations And Such



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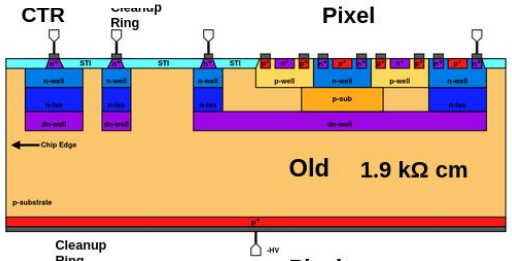
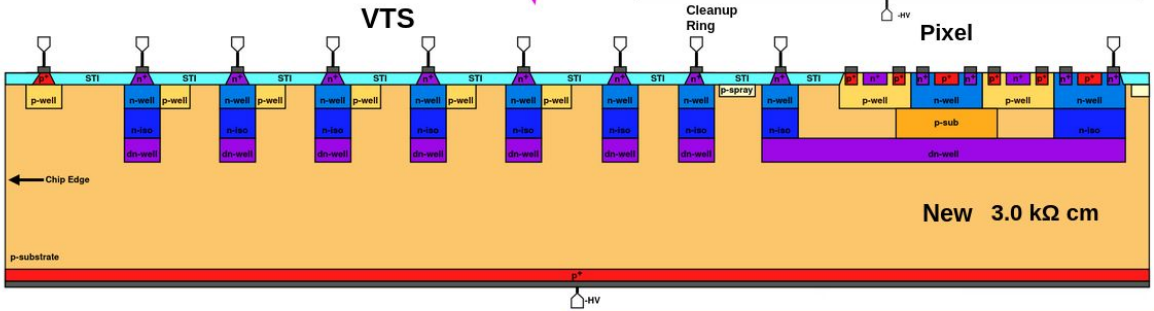
Recap

- Changed the cross section
- Change ring structure Current Terminating Ring (CTR) to Voltage Terminating Scheme (VTS)
- Implement a doping profile to stop leakage channel (p-spray)
- Increase substrate resistivity
- Keep backside biasing





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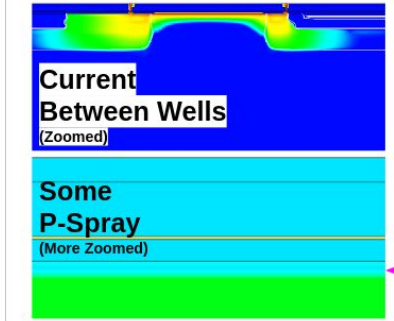

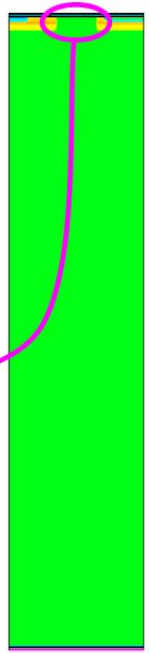

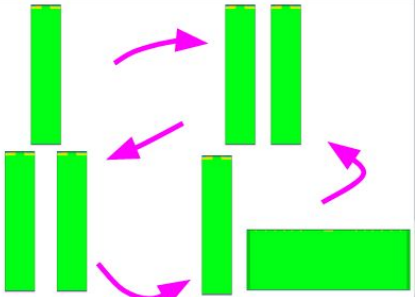

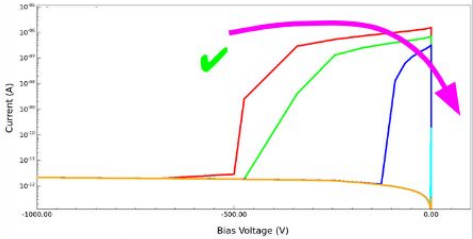

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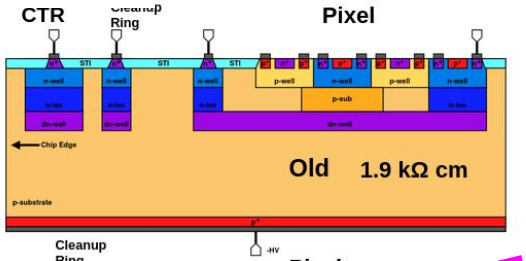

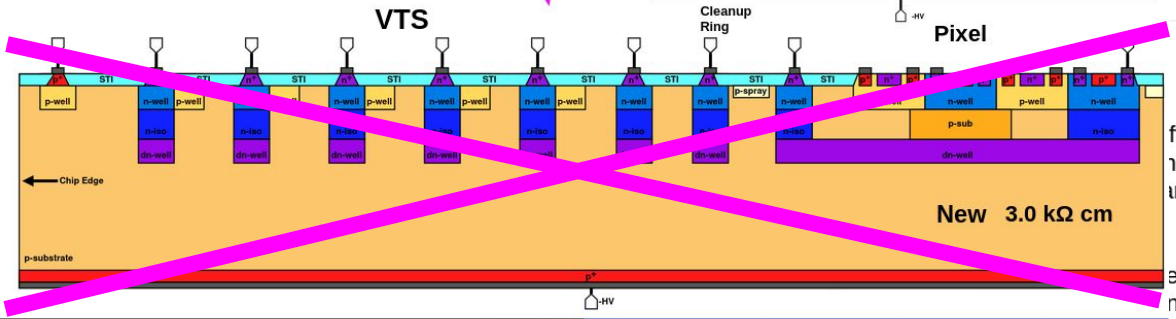

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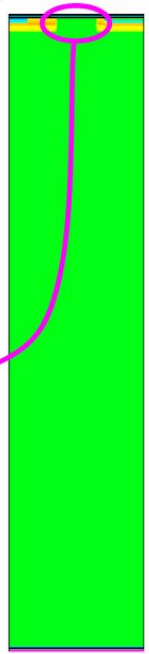
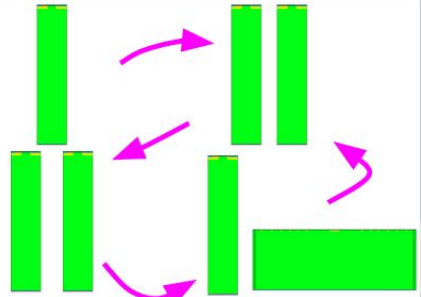
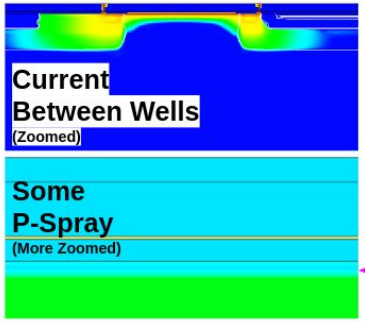
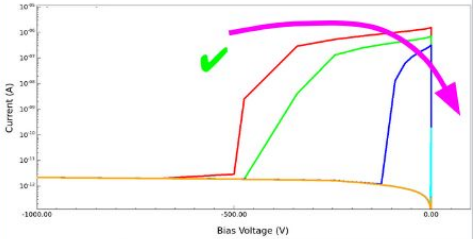






P-Spray



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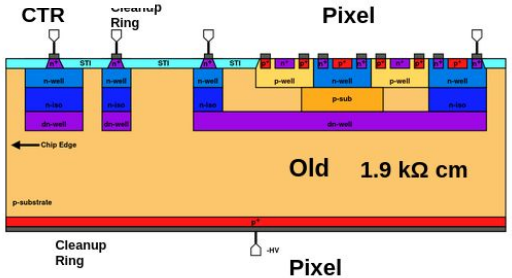

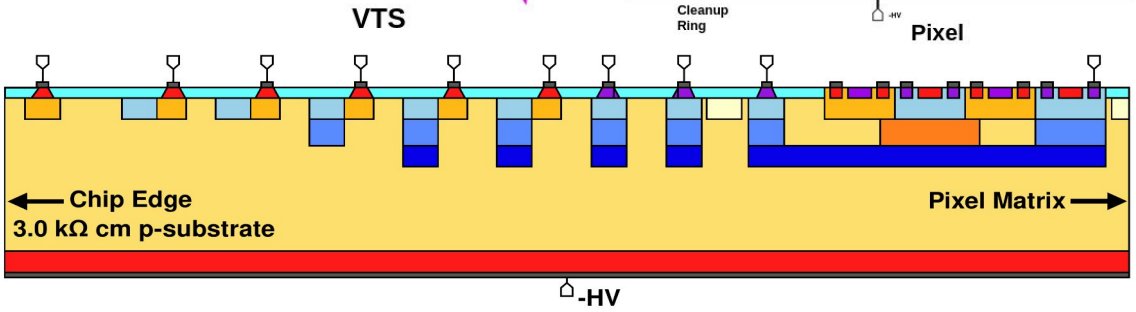

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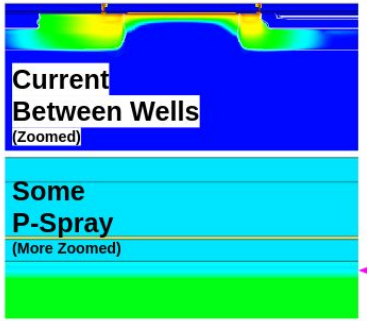

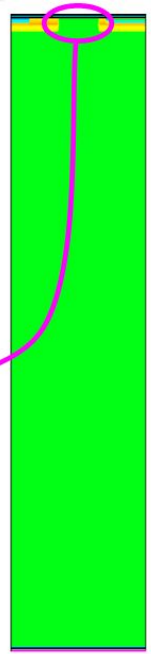

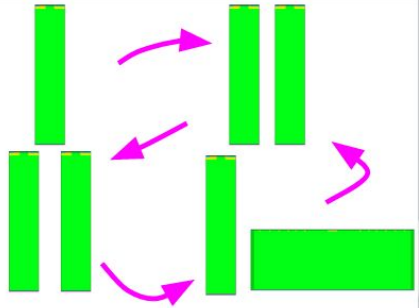

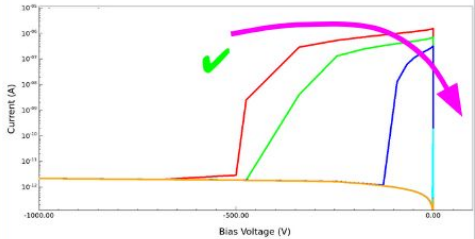

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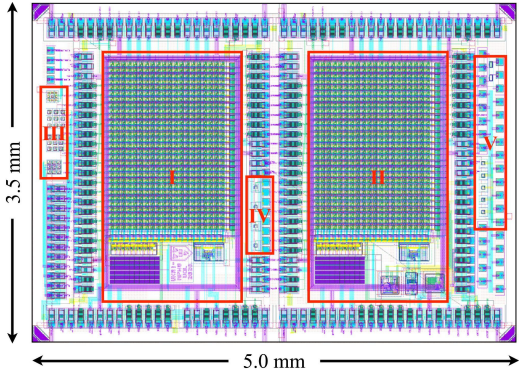
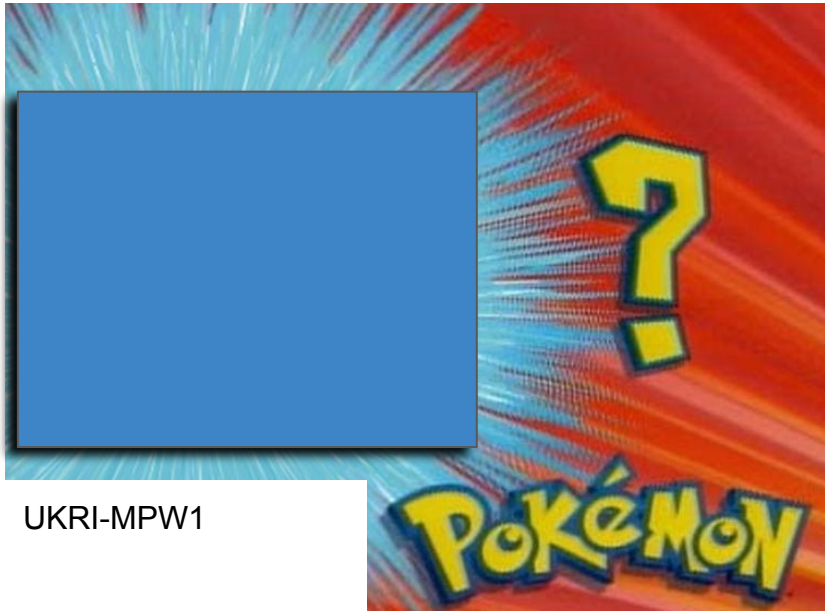
UKRI
Work Over The Last Couple Years



UKRI-MPW0

- Characterisation of depletion region (eTCT)
- Effects of Non Ionising Energy Loss (NIEL) radiation on depletion region
- Conference proceedings published



UKRI-MPW1

- TCAD simulation
- Interpixel channel reduction
- Breakdown simulations

Ultimate goal:

- Improve radiation tolerance of HV-CMOS sensors
- Replace Hybrid-pixels
- TAKE OVER THE WORLD

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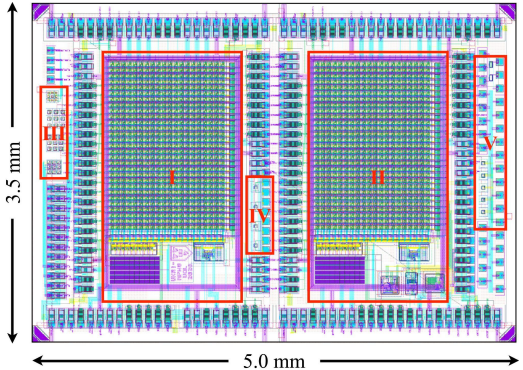
UKRI
Work Over The Last Couple Years



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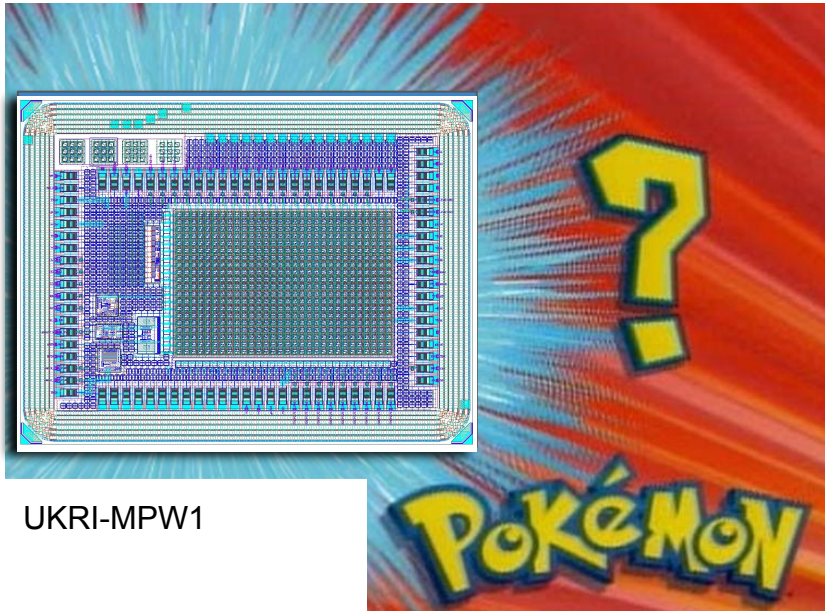

UKRI-MPW1

- TCAD simulation
- Interpixel channel reduction
- Breakdown simulations
- **Conference Proceedings (Pending)**
- **Breakdown measurements**

Ultimate goal:

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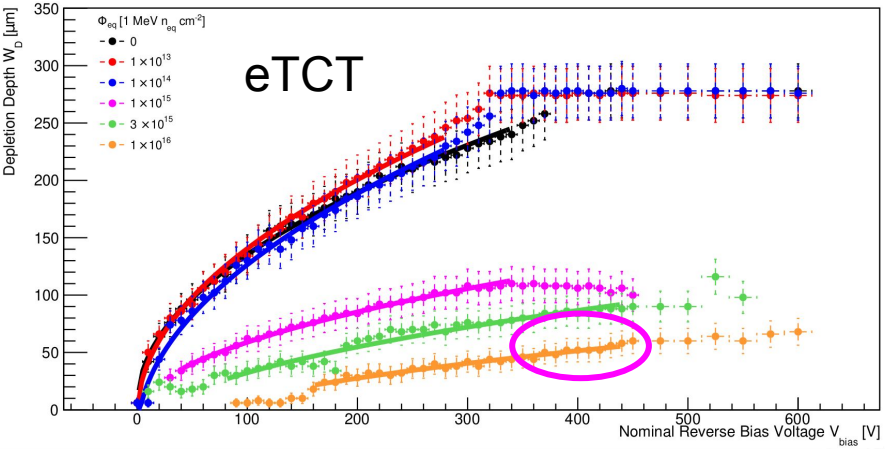
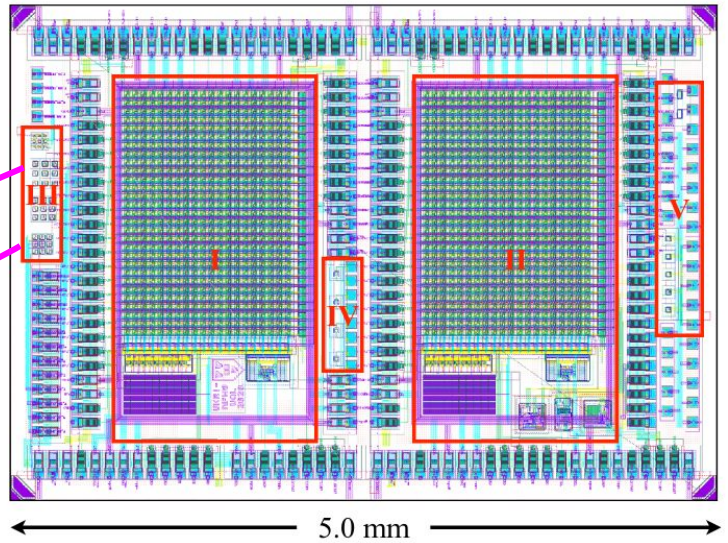
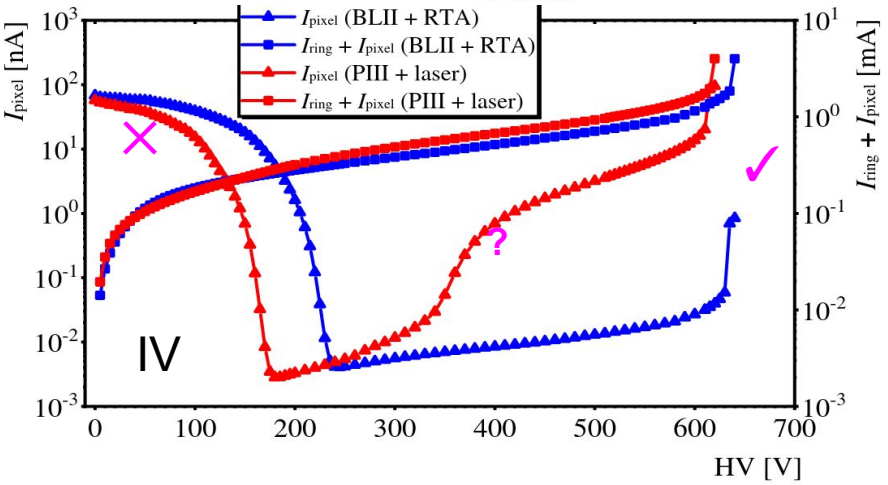
UKRI-MPW0 Characteristics

- Breakdown ~ 600 V
- 50 µm Depletion at 400 V, after 1x10^{16} 1 MeV n_{eq} cm^{-2}

- ~ 1 mA substrate leakage (pixel leakage okay)
- High Current at low bias





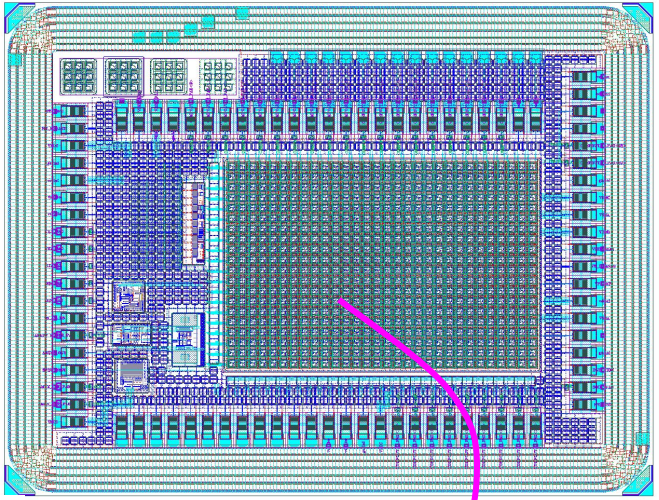


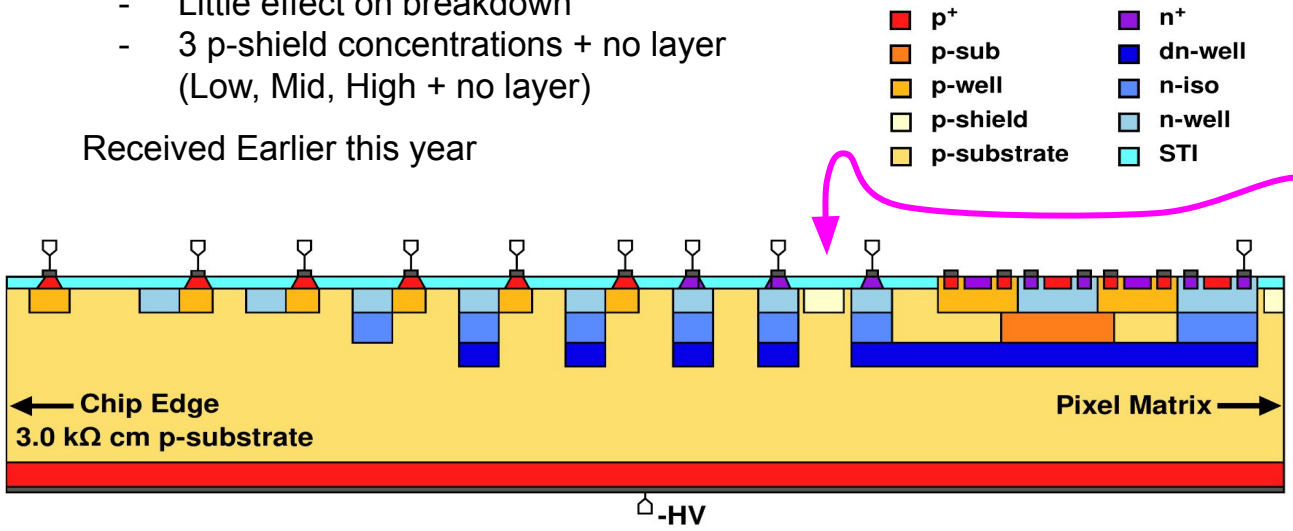
UKRI-MPW1 Chip Additions

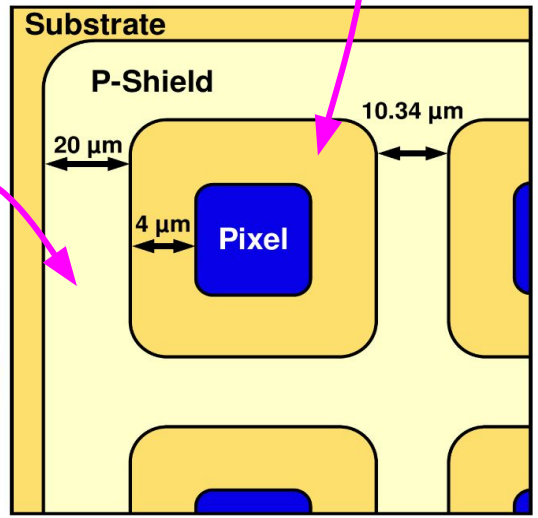
- Change ring scheme to Voltage Terminating Scheme (VTS)
  - Gradually step down potential to chip edge
  - Reduce leakage current

- Implement new p-shield layer
  - Single p-type profile
  - Targetted
  - Better isolate pixels
  - Run chip at lower voltages
  - Little effect on breakdown
  - 3 p-shield concentrations + no layer (Low, Mid, High + no layer)

Received Earlier this year





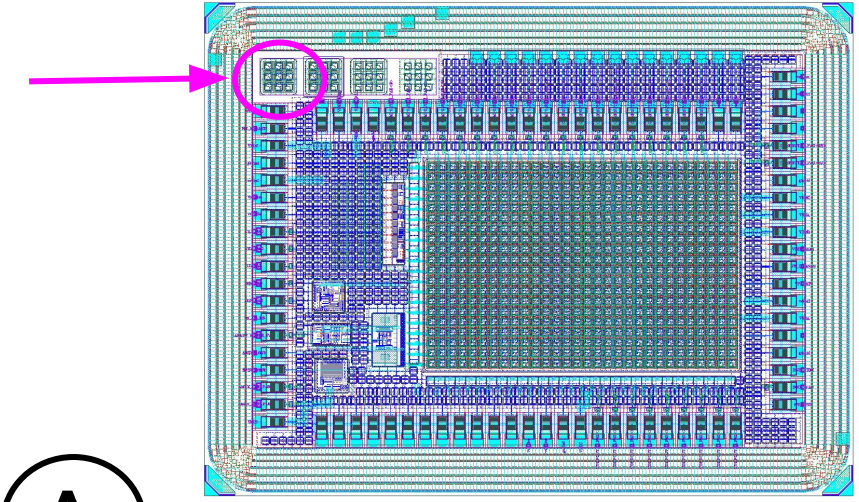


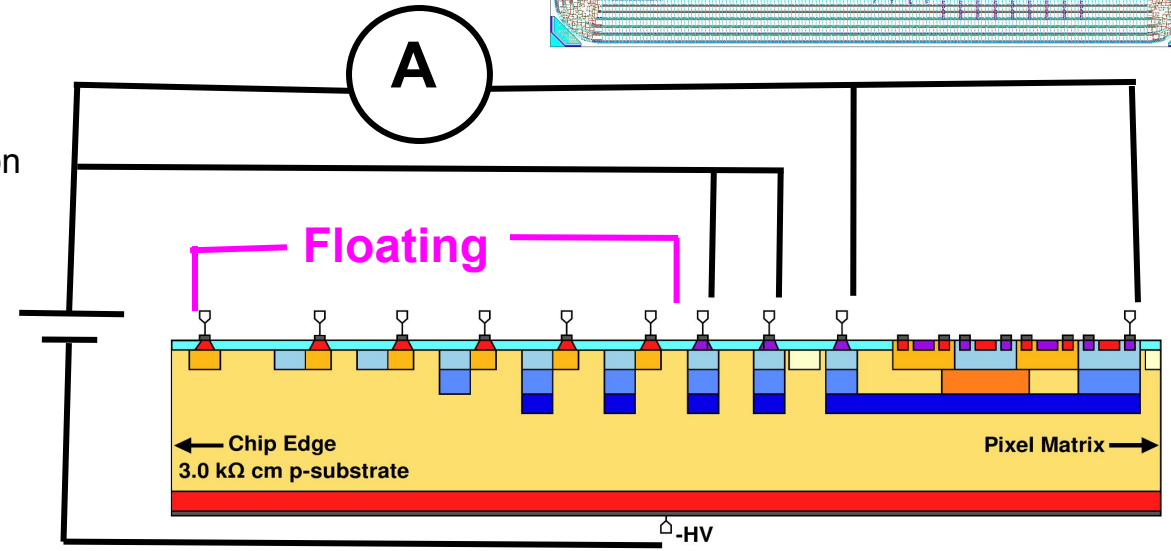
UKRI-MPW1 Preliminary

I-V Measurements

- Preliminary Current Voltage (IV) measurements
- Test structure I (3 x 3 passive pixels)
- 3 p-shield recipes + No p-shield

- Test structure pixels, n-fill, Clean-Up ring to 0 V
- Central pixel measured
- Outer 8 measured together
- Seal ring (Outer p-well) floating
- Backside to HV
- Several Chips per p-shield concentration

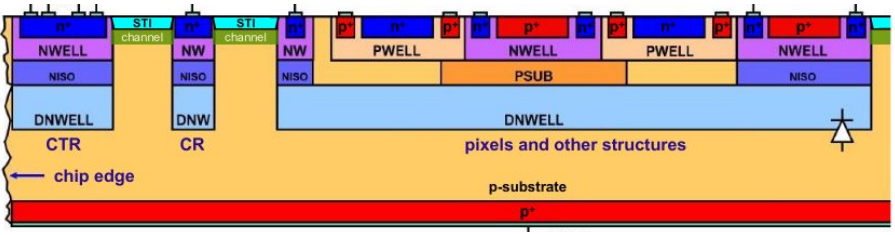


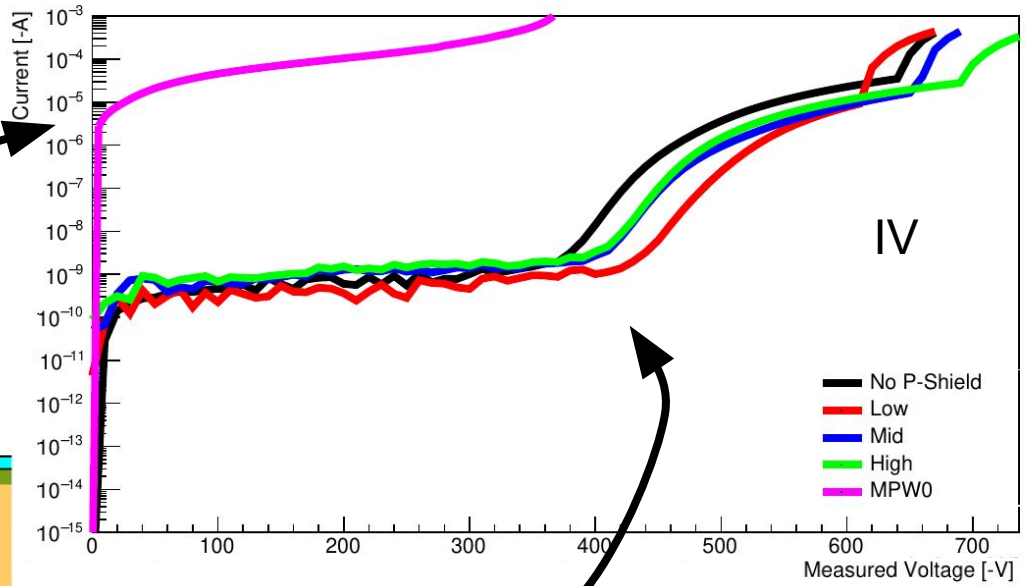


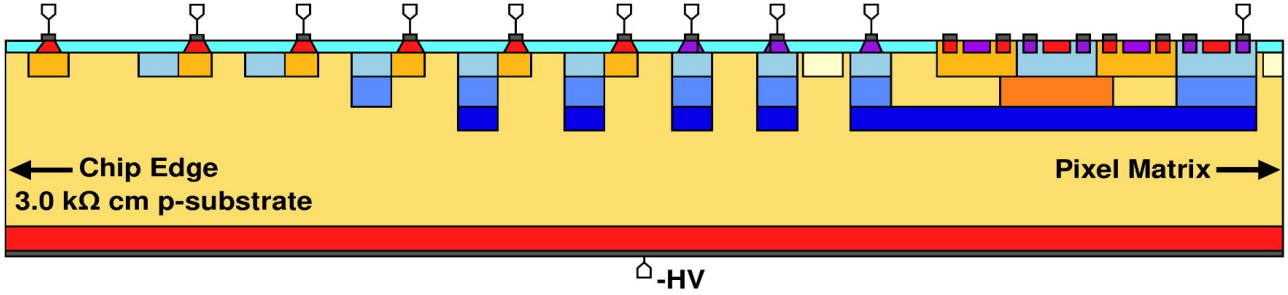
UKRI-MPW1 Preliminary

Chip Breakdown

- Substantial reduction in chip leakage
- Slight variation in breakdown (within sample and wafer variation)
- Strange shape in substrate curve

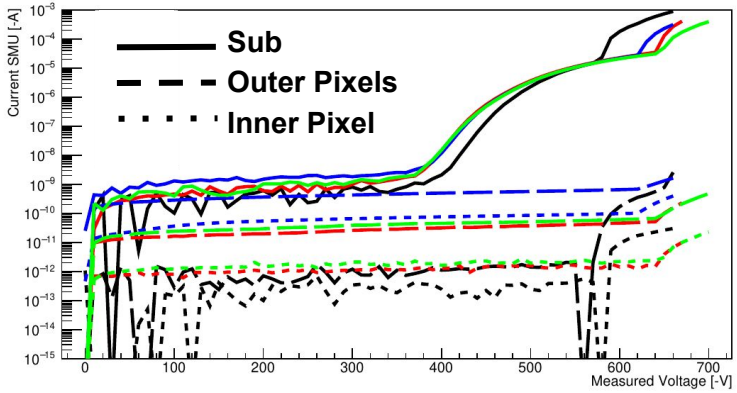




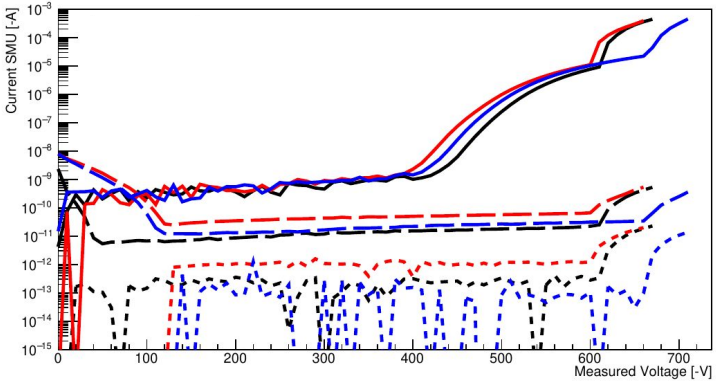


UKRI-MPW1 Preliminary

Pixel Isolation

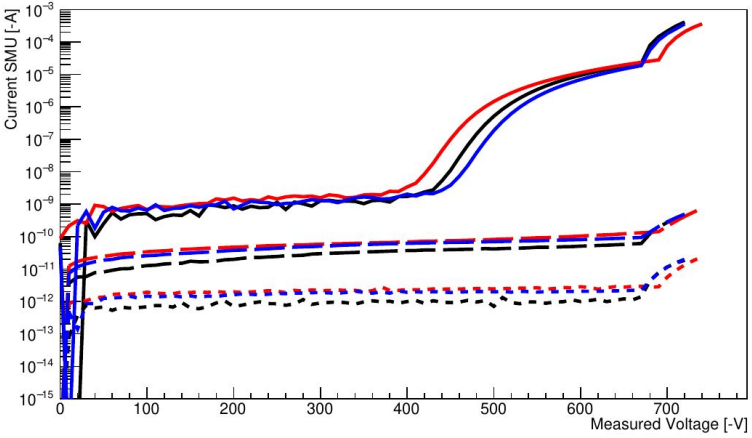


No layer

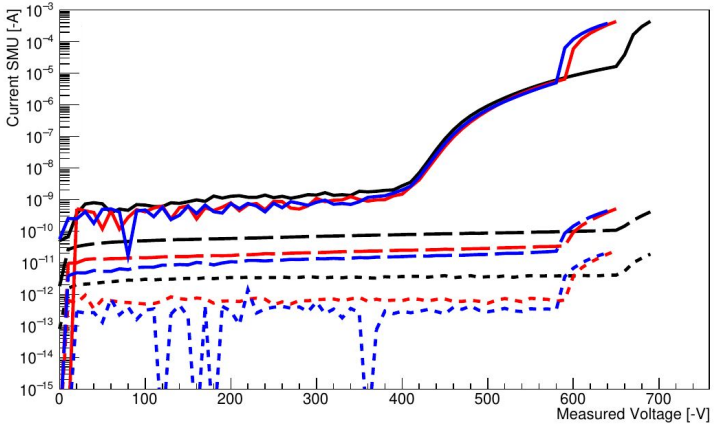


Low

Mid

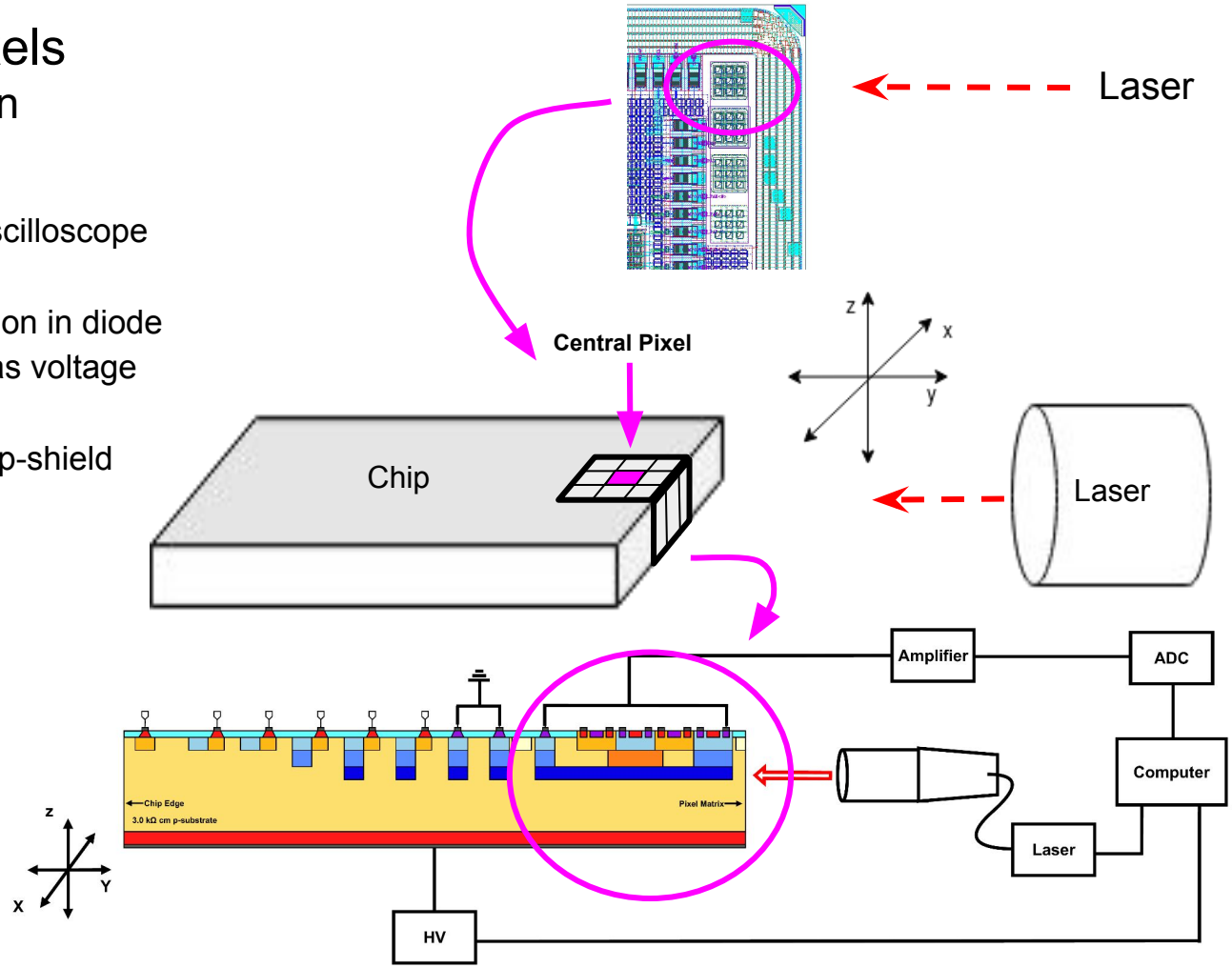


High



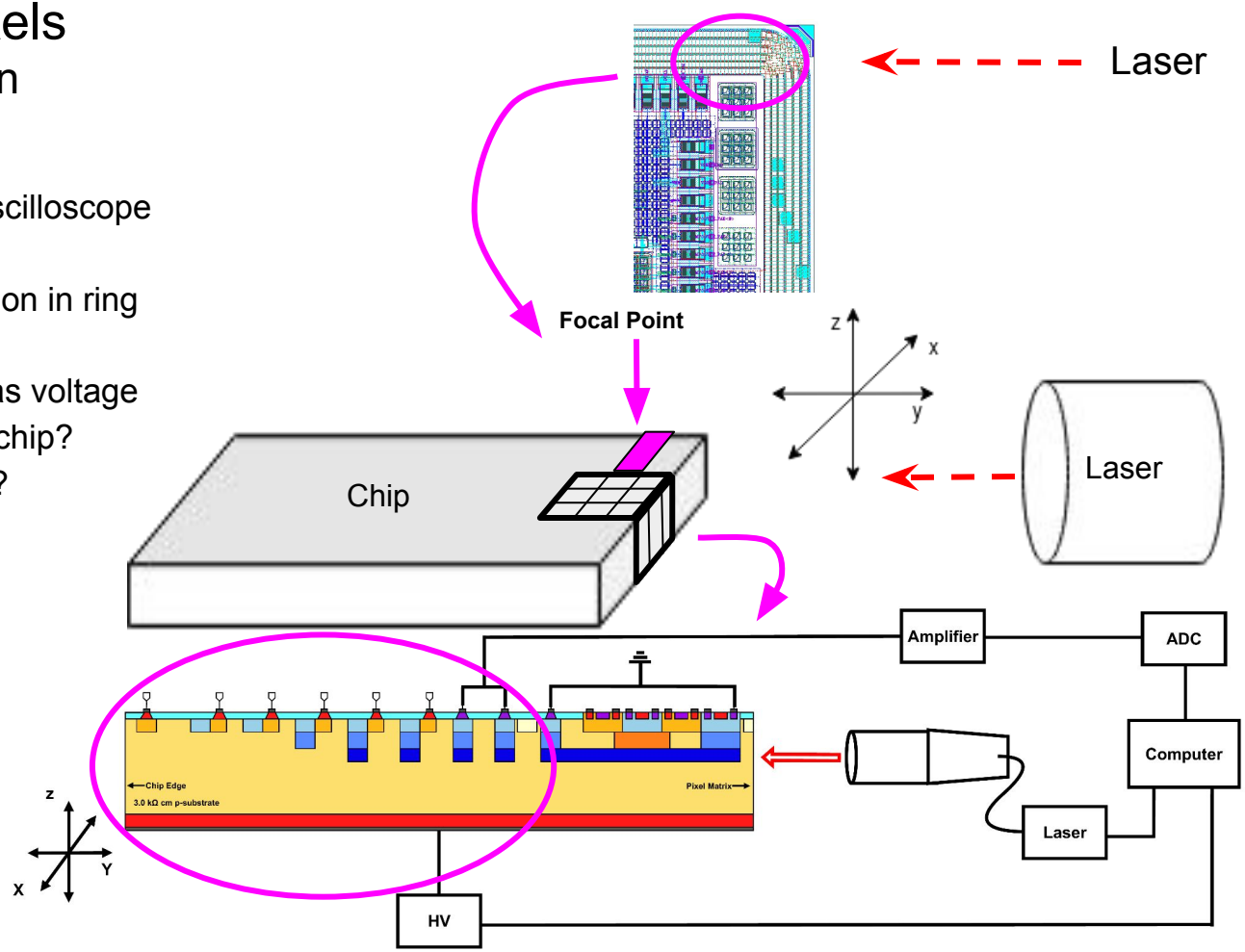
UKRI-MPW1 eTCT Pixels
Measurements To Be Taken

- Connect test structure through oscilloscope
- Focus IR laser on central pixel
- Map charge generated with position in diode
- See how depletion grows with bias voltage
- Find resistivity of chip
- See how depletion interacts with p-shield



UKRI-MPW1 eTCT Pixels
Measurements To Be Taken

- Connect ring structure through oscilloscope
- Focus IR laser on central pixel
- Map charge generated with position in ring scheme
- See how depletion grows with bias voltage
- Find locations of damage on the chip?
- Help develop better ring scheme?



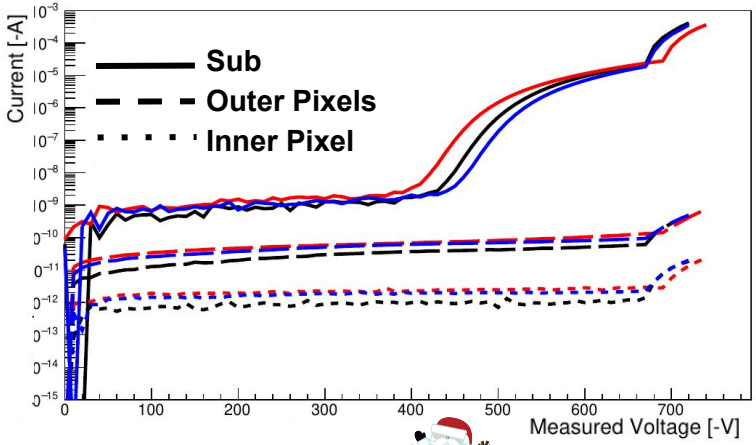
UKRI-MPW1 Outlook

- New ring scheme working (mostly)
- P-shield Reduces interpixel current
- Less noise between samples
- Minimal reduction in breakdown

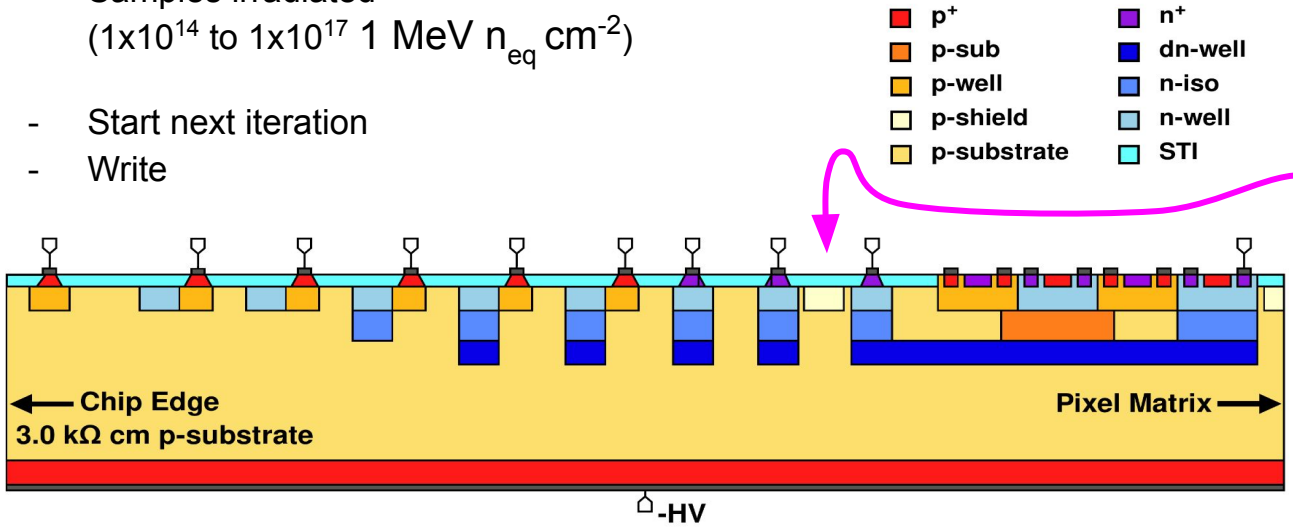
- Shape to be understood
- eTCT of p-shield/pixel effects
- eTCT of ring structure
- Samples irradiated
  ($1x10^{14}$ to $1x10^{17}$ 1 MeV n_{eq} cm^{-2})

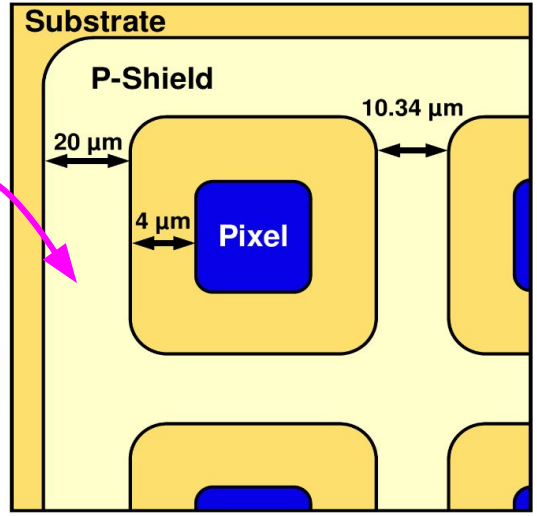
- Start next iteration
- Write

High



Merry Christmas



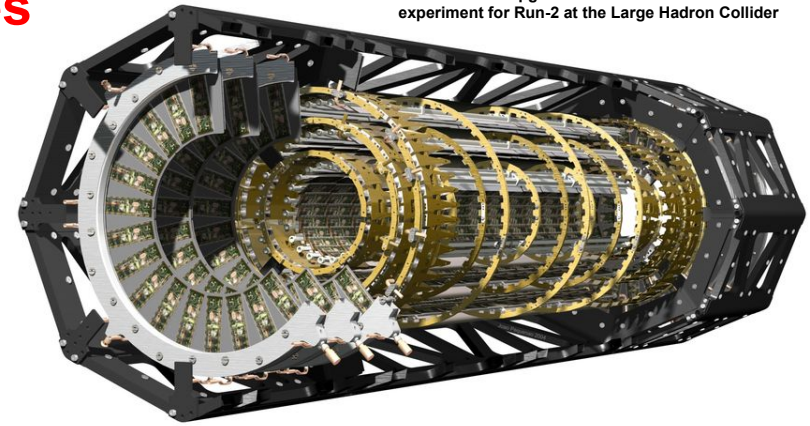


Trackers

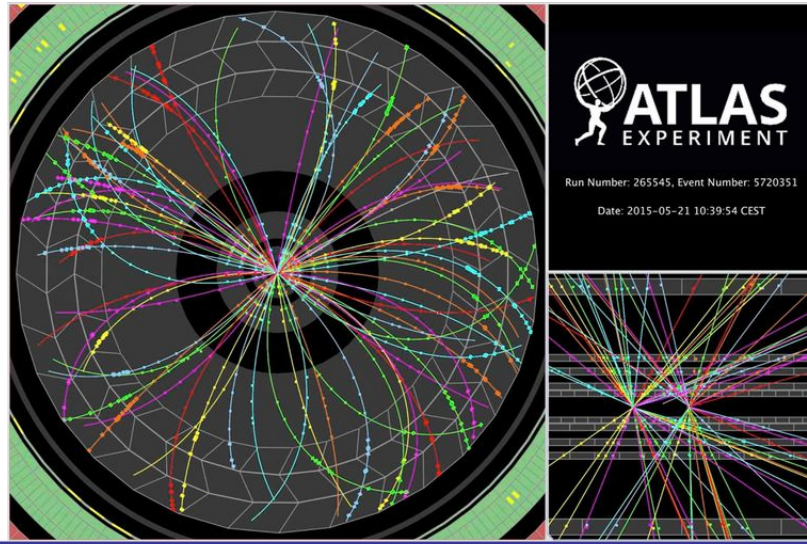
Backup Slides

- Collision event generates charged particles
- Charged particles curve in magnetic field
- Tracker follows the path
- Curvature determines charge, mass of particle

The ATLAS Inner Tracker
G. Mullier: **The upgraded Pixel Detector of the ATLAS experiment for Run-2 at the Large Hadron Collider**



Placed close to collision center	→	Sensors receive high radiation dose
High rate of events MHz-GHz rate of bunch crossings	→	Fine spatial resolution required Good time resolution
Minimal track disruption	→	Thin sensors
Higher collision energies	→	More radiation, finer detail needed

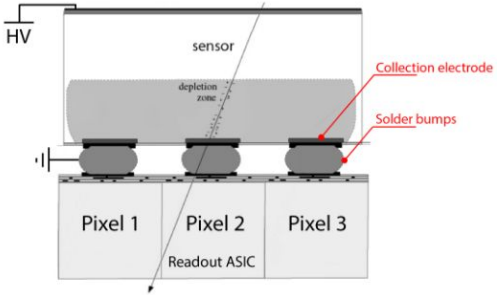


Sensors need to be thin, fast, radiation tolerant, and within budget

DISCLAIMER: I do not work for ATLAS, this is just an example

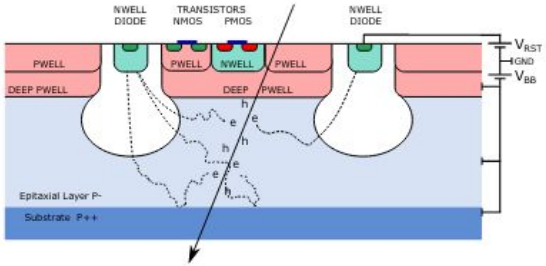
Pixel Sensors

Backup Slides



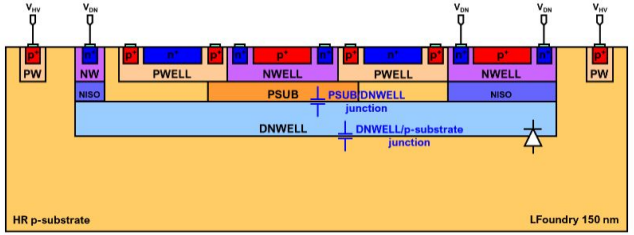
Hybrids

Cross-section of a hybrid pixel design proposed for CLiC



CMOS

Cross-section of standard CMOS pixel ALPIDE used in ALICE



HV-CMOS

Cross-section of a typical HV-CMOS pixel

External Readout Circuitry:

- ✔ Fast readout
- ✘ Specialised bump-bonding
- ✘ Increases thickness
- ✘ Limits granularity

Integrated Readout Circuitry:

- ✔ Thin sensors
- ✔ Industrial standard
- ✔ Cost effective

Integrated Readout Circuitry:

- ✔ Thin sensors
- ✔ Industrial standard
- ✔ Cost effective

High Voltage Pixel:

- ✔ More radiation tolerant
- ✔ Fast charge collection (Drift)

Low Voltage Pixel:

- ✘ Less radiation tolerant
- ✘ Slow charge collection (Diffusion)

High Voltage Pixel:

- ✔ More radiation tolerant
- ✔ Fast charge collection (Drift)

Future Requirements

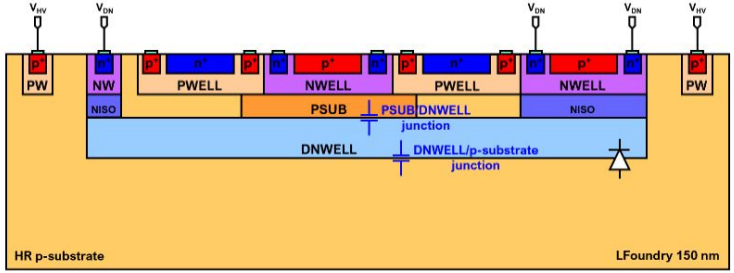
Backup Slides

Industrial Standard Manufacturing Process → No specialised (expensive) processes

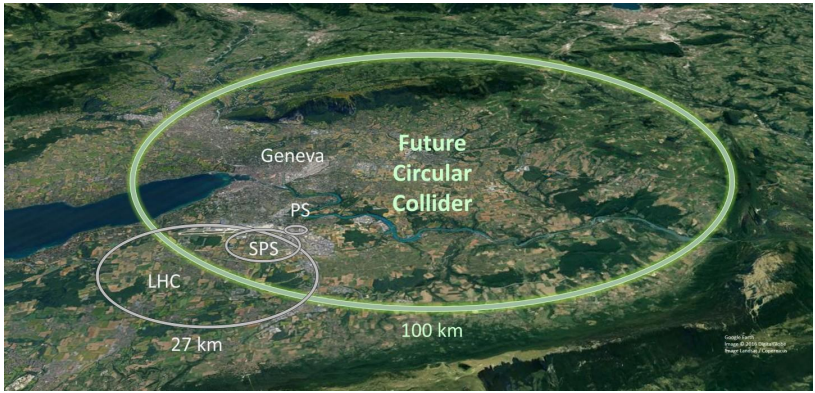
High Voltage → Radiation tolerant, Fast time resolution

Monolithic → Thin

Cross-section of a typical HV-CMOS pixel



	Pixel Size (μm^2)	System Time Resolution (ns)	Radiation Tolerance (NIEL) (1 MeV $n_{eq} cm^{-2}$ Year $^{-1}$)
HL-LHC	50 x 50	0.03	10^{16}
FCC-hh	25 x 50	0.1	10^{16} to 10^{17}
Current HV-CMOS	50 x 50	3.16	10^{15}



Future tracking detector specifications, and current HV-CMOS capabilities

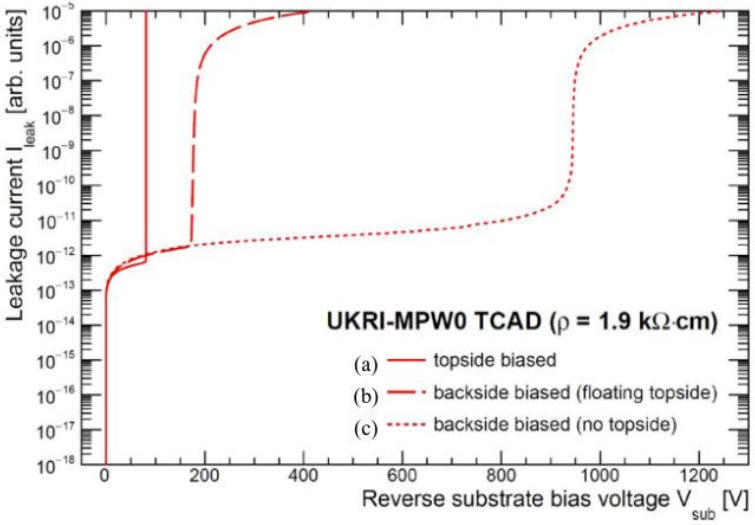
https://cds.cern.ch/record/2653532/files/FCC%20v2.jpg?subformat=icon-1440

Liverpool HV-CMOS Project **Backup Slides**

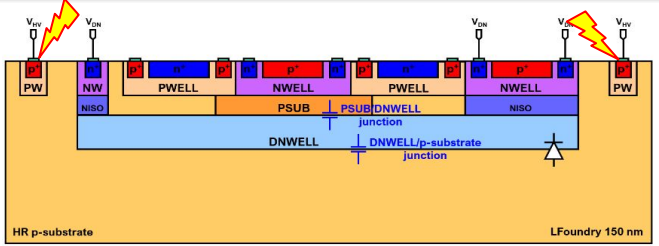
- Increase breakdown voltage
- Increase radiation tolerance

- Backside bias
- Reduce topside p-wells

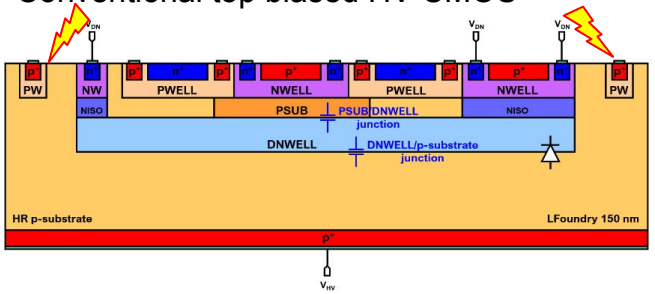
- ~ 1000 V chip breakdown in simulation



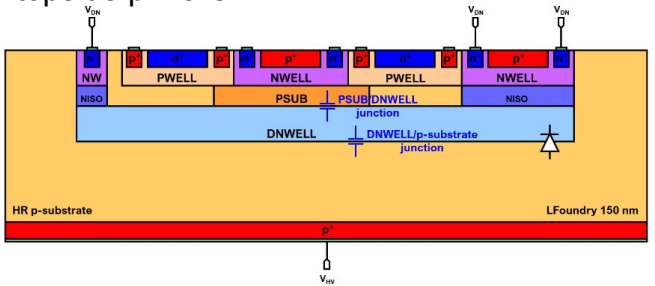
UKRI-MPW0



Conventional top biased HV-CMOS



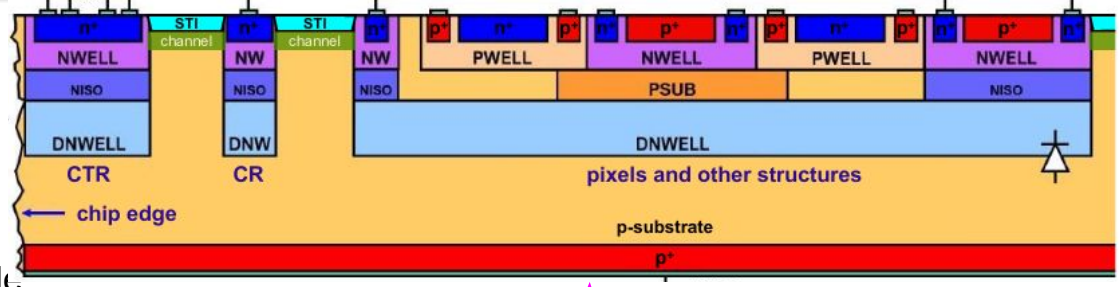
Backside biased HV-CMOS with floating topside p-wells



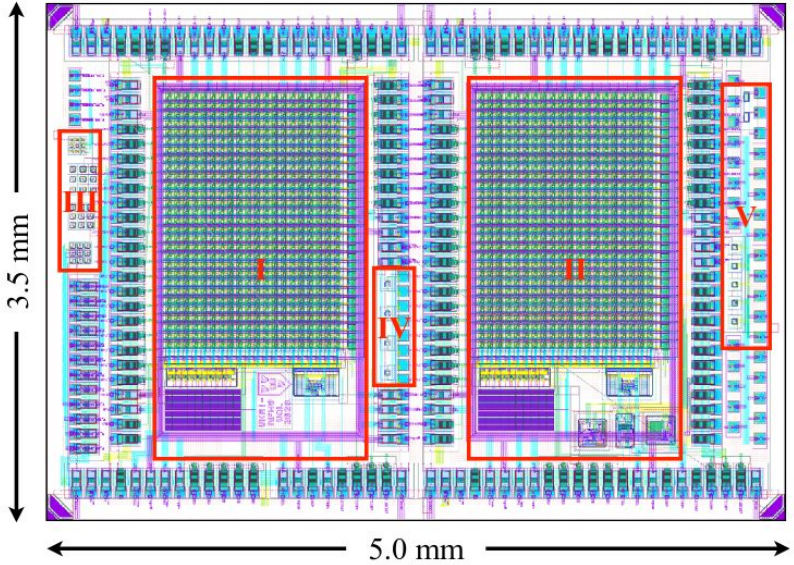
Backside biased only HV-CMOS
No topside biasing p-wells

UKRI-MPW0 Design

- LFoundry 150 nm, HV-CMOS
- 1.9 kΩ cm Substrate Resistivity
- 5.0 mm x 3.5 mm
- Thinned to 280 µm thickness before backside processing
- Current Terminating Ring structure (CTR)
- Fully backside biased only
  - Backside processing provided by Ion Beam Service (IBS)
  - 2 Processing methods offered
- 2 Active matrices
- 3 Sets of passive test structures



Cross-section of UKRI-MPW0 pixel



Layout of the UKRI-MPW0 Pixel chip

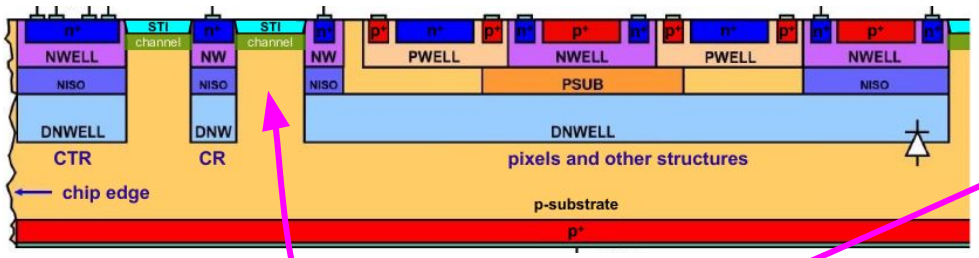
Backup Slides

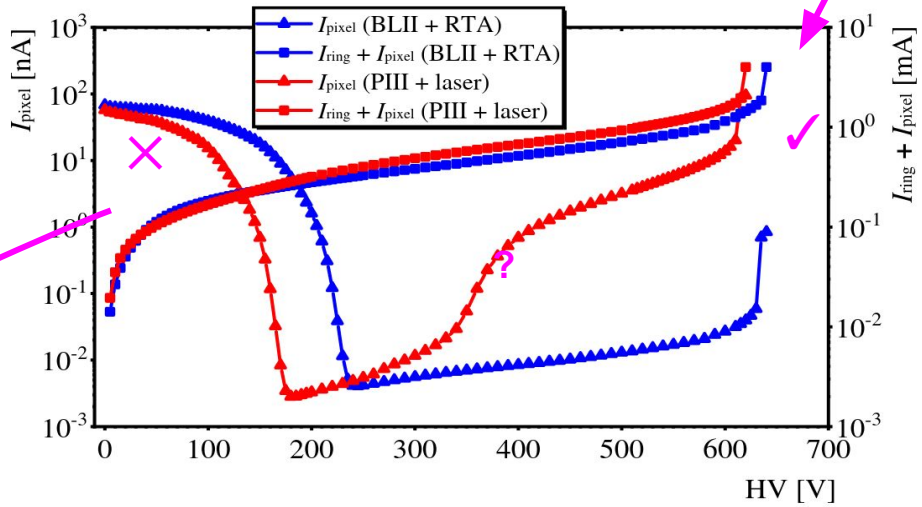
UKRI-MPW0 Characteristics

- Intrinsic charge on oxide (STI)
- Parasitic transistor forms at STI/Si boundary
- Noisey pixels
- Higher leakage

	Substrate Resistivity (Ω cm)	Breakdown Voltage (V)
UKRI-MPW0	**1900**	**~ 600**
LF-monoPix2	2000	~ 460
Astropix	100	~ 250

Cross-section of UKRI-MPW0 pixel



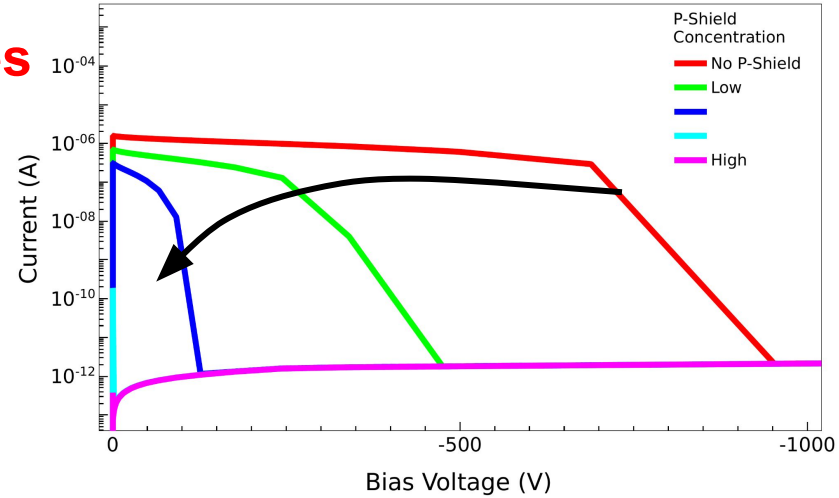


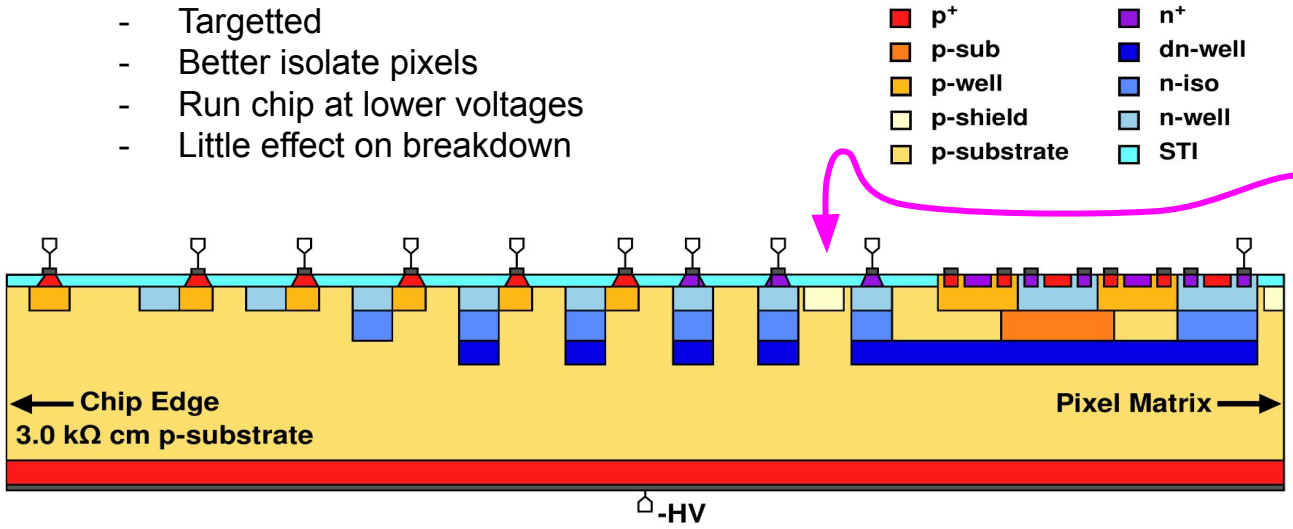
Backup Slides

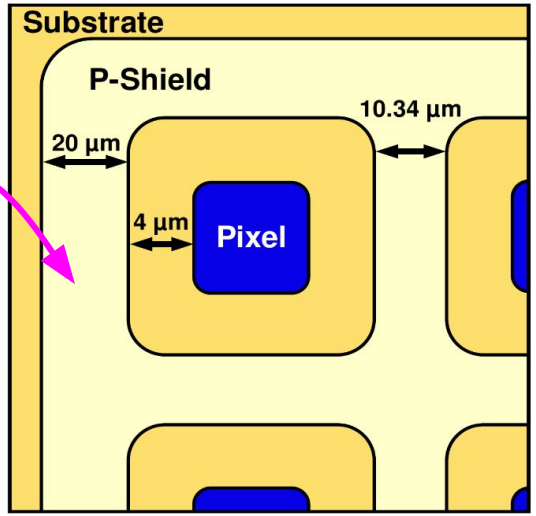
UKRI-MPW1 TCAD

Backup Slides

- Change ring scheme to Voltage Terminating Scheme (VTS)
  - Gradually step down potential to chip edge
  - Reduce leakage current
- Implement new p-shield layer
  - Single p-type profile
  - Low dose
  - Increasing conc' closes channel faster
  - Targetted
  - Better isolate pixels
  - Run chip at lower voltages
  - Little effect on breakdown



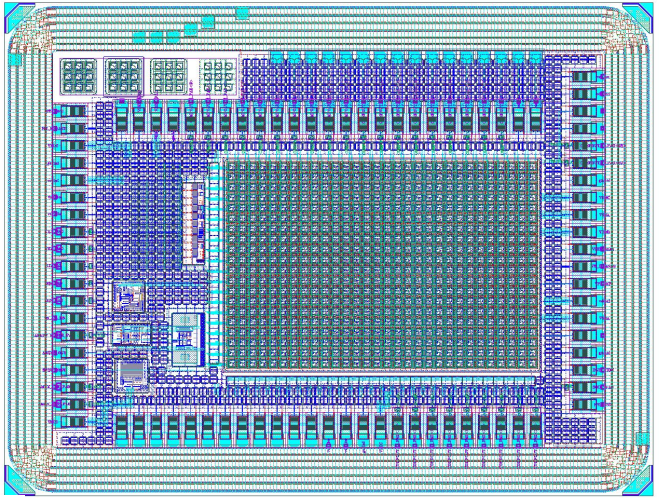


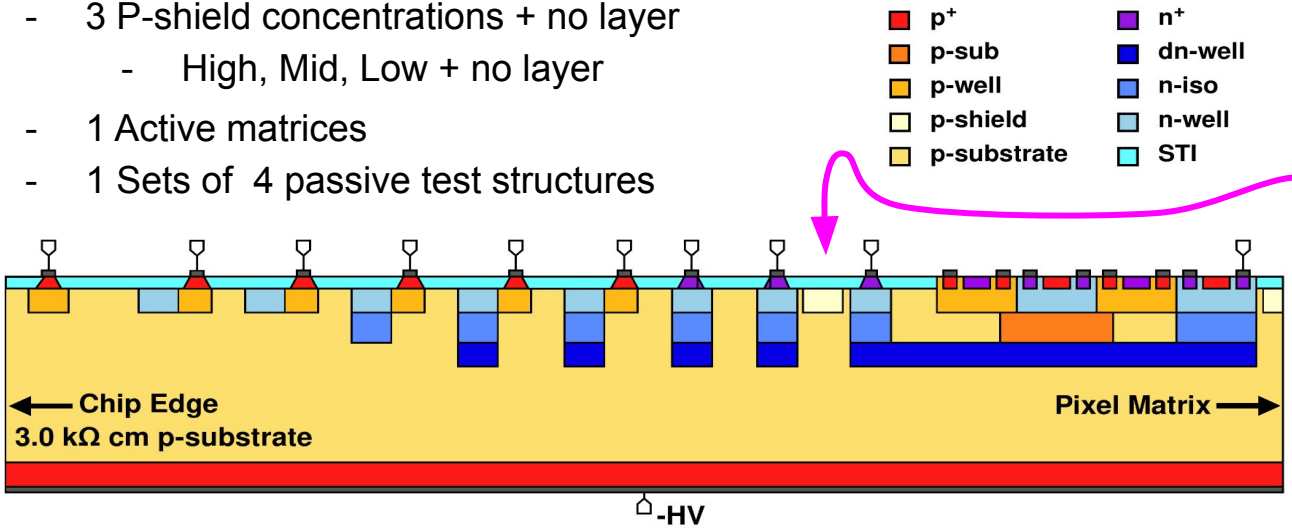


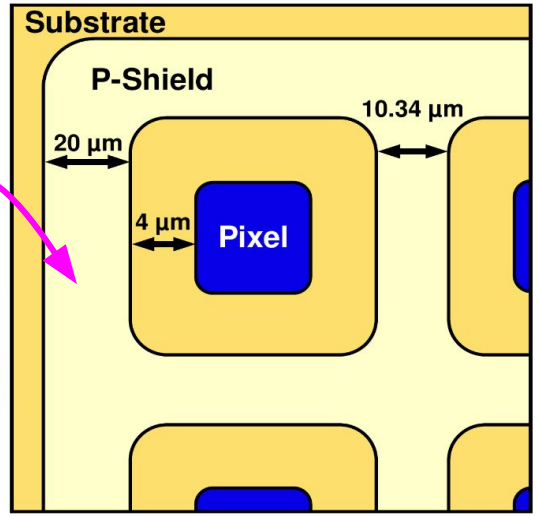
UKRI-MPW1 Chip

Backup Slides

- LFoundry 150 nm, HV-CMOS
- 3.0 kΩ cm Substrate Resistivity
- 3.8 mm x 2.7 mm
- Thinned to 280 µm thickness before backside processing
- Voltage Terminating Ring structure (VTR)
- Additional “n-fill” structures for improved performance
- Backside Biased
  - Backside processing provided by Ion Beam Service (IBS)
- 3 P-shield concentrations + no layer
  - High, Mid, Low + no layer
- 1 Active matrices
- 1 Sets of 4 passive test structures







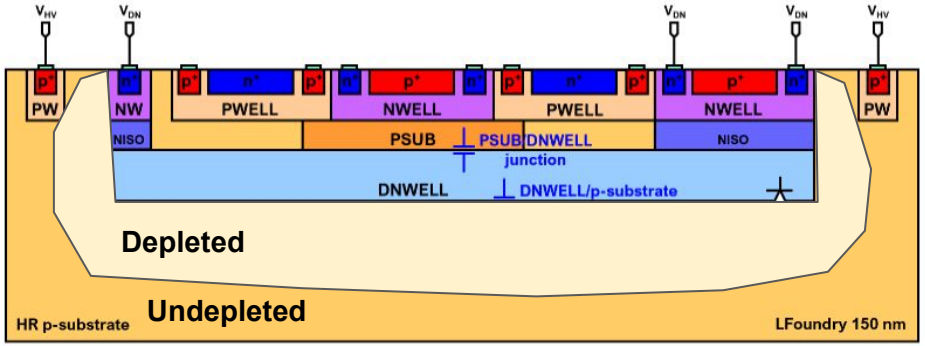
Sensing Region

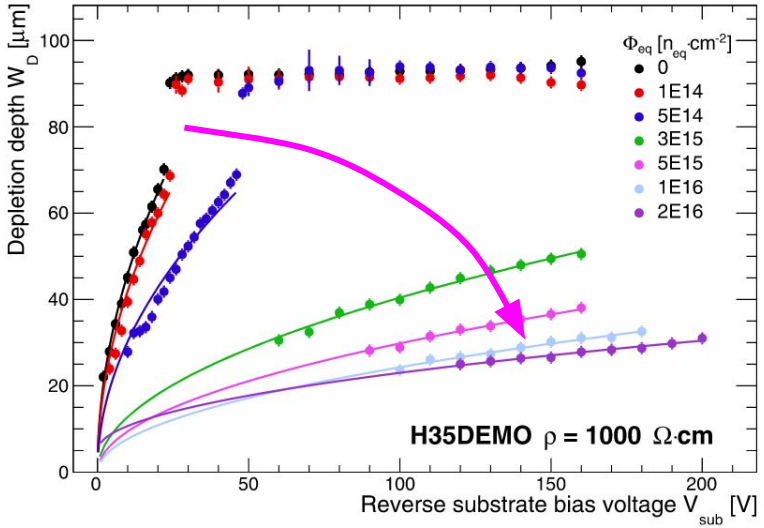
- Sensing diode increases depletion region with negative biases until diode breaks down
- NIEL reduces depletion region ability to grow
- Counteracted by increasing bias voltage
  - more room for growth
  - Increases charge collection speed
  - Charge traps less effective

$$W = W_0 + \sqrt{\frac{2\epsilon_r \epsilon_0}{qN_A} V_{bias}}$$

W	=	Depletion depth of semiconductor
W_0	=	Depletion depth at 0 V
ϵ_r	=	Relative permittivity of silicon
ϵ_0	=	Permittivity of free space
q	=	Charge of an electron
N_A	=	Doping concentration of acceptor atoms
V_{bias}	=	Reverse bias voltage

Backup Slides

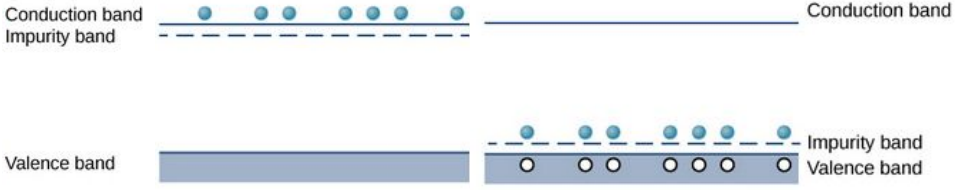




Bulk Damage:

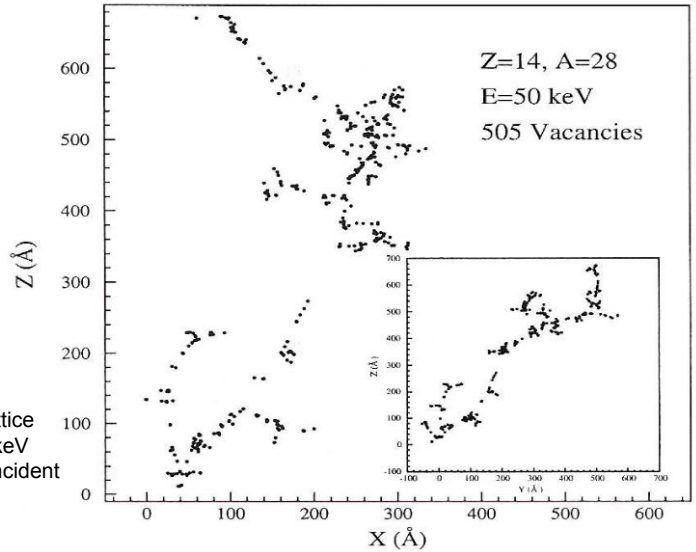
Non Ionising Energy Loss (NIEL)

- Incident radiation knocks an atom out of the lattice, Primary Knock-on Atom (PKA)
- Atom travels knocking more atoms out of the lattice, interstitial-vacancy pairs (Frenkel Pairs)
- Damage introduces acceptor removal, energy levels in the band structure, and charge traps
- **Changes doping profile and resistivity**



Band structure of n and p-type semiconductors (left to right)

S. J. Ling, J. Sanny, and B. Moebs, University Physics Volume 3, 1st ed. Houston, TX: Rice University 2016



Vacancies in a silicon lattice caused by a PKA of 50 keV generated by a 1 MeV incident neutron

F. H¨onniger, “Radiation damage in silicon. defect analysis and detector properties”, 2008.

Backup Slides