CMOS R&D for the LHCb Mighty-Tracker

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[with inputs from many others… thanks!]
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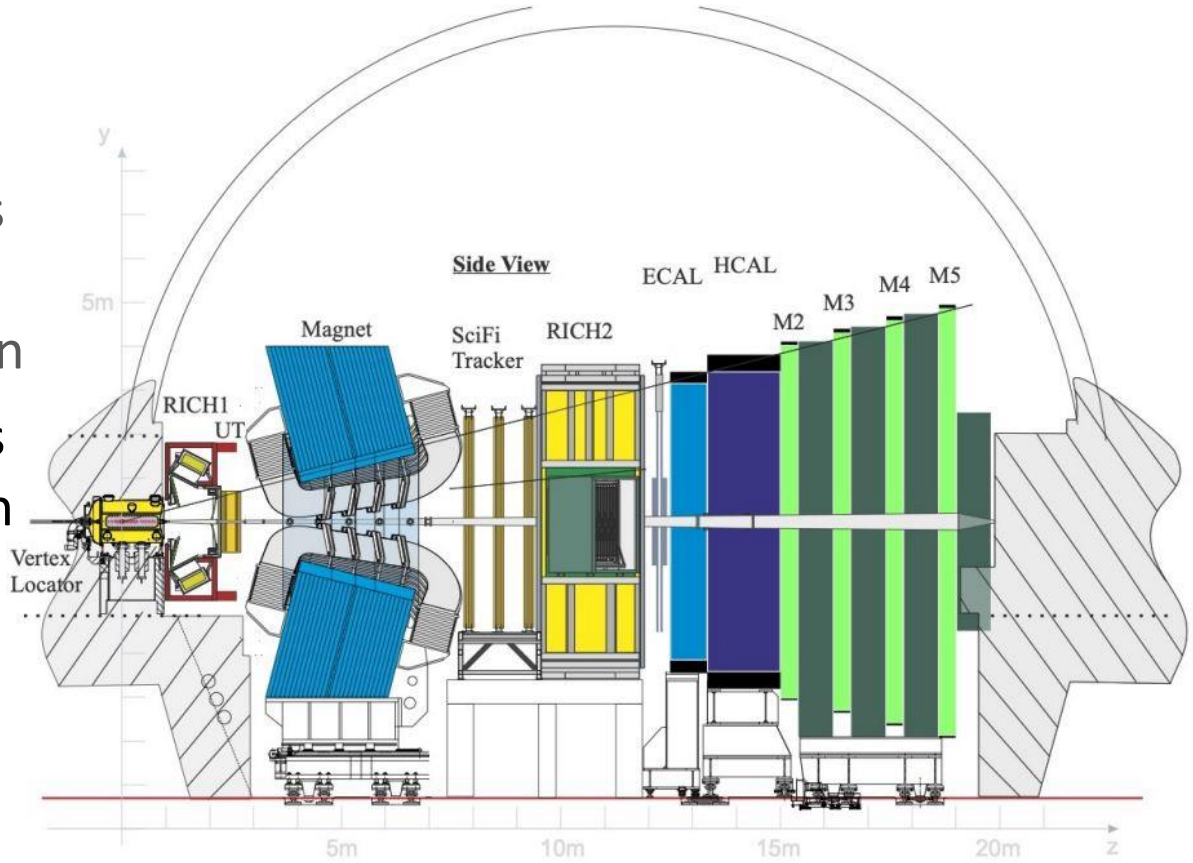
Overview

- LHCb experiment
- LHC schedule
- LHCb Upgrade II
- Mighty-Tracker
- Mighty-Pixel
  - Detector scenarios
  - Modules
  - Sensor specifications
  - Sensor R&D
  - MightyPix
  - RadPix
  - Power
- Summary and outlook

LHCb experiment

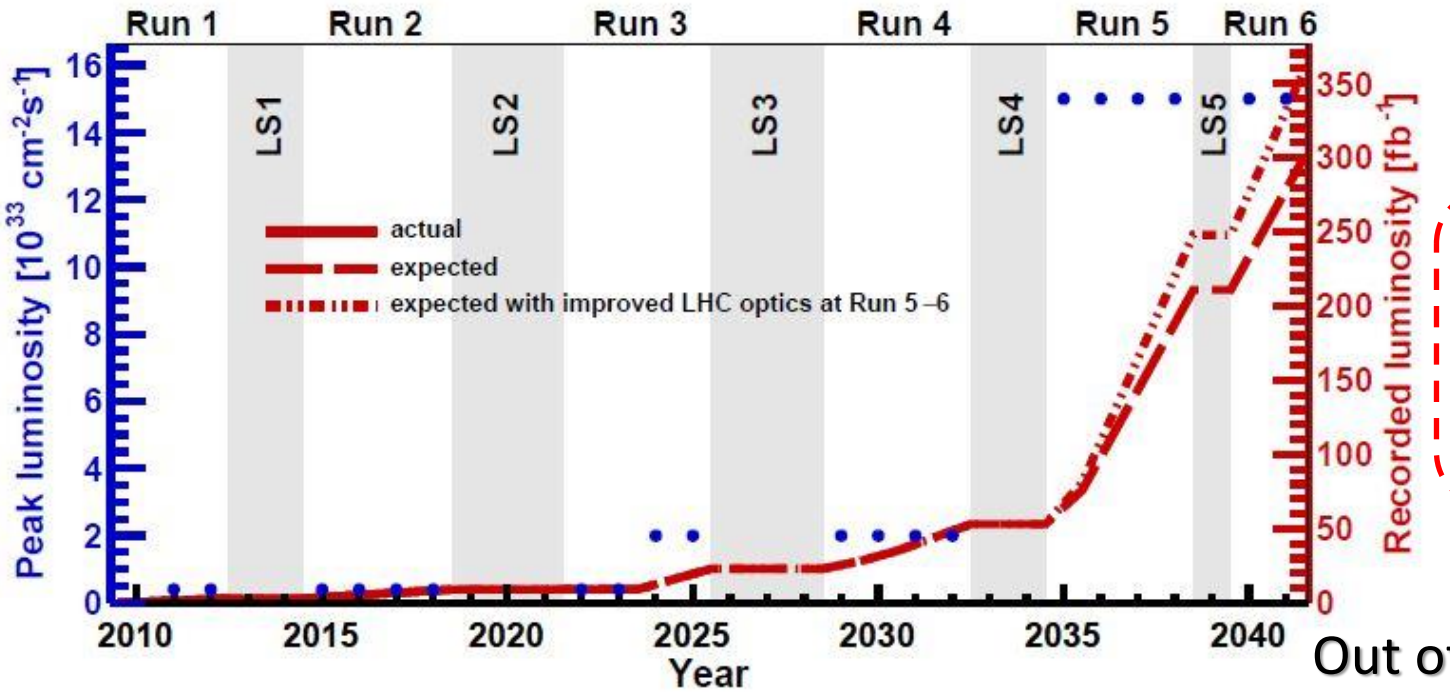
- One of the four large experiments at the LHC at CERN
- Main goal
  - To search for new physics through studies of CP-violation and decays of heavy-flavour hadrons with exceptional precision
- Single-arm forward spectrometer –LHCb does not surround the entire collision point with an enclosed detector, but uses a series of sub-detectors to detect forward particles
- Successfully operated since Run 1 (2010)
- Upgrade I during LS2 (2019-21) to allow operation during Run 3 and Run 4 ($L = 2 \times 10^{33}$ $cm^{-2}s^{-1}$)



The LHCb Upgrade I (layout view)

LHC schedule

Instantaneous luminosity increase by ~ one order of magnitude compared to Upgrade I



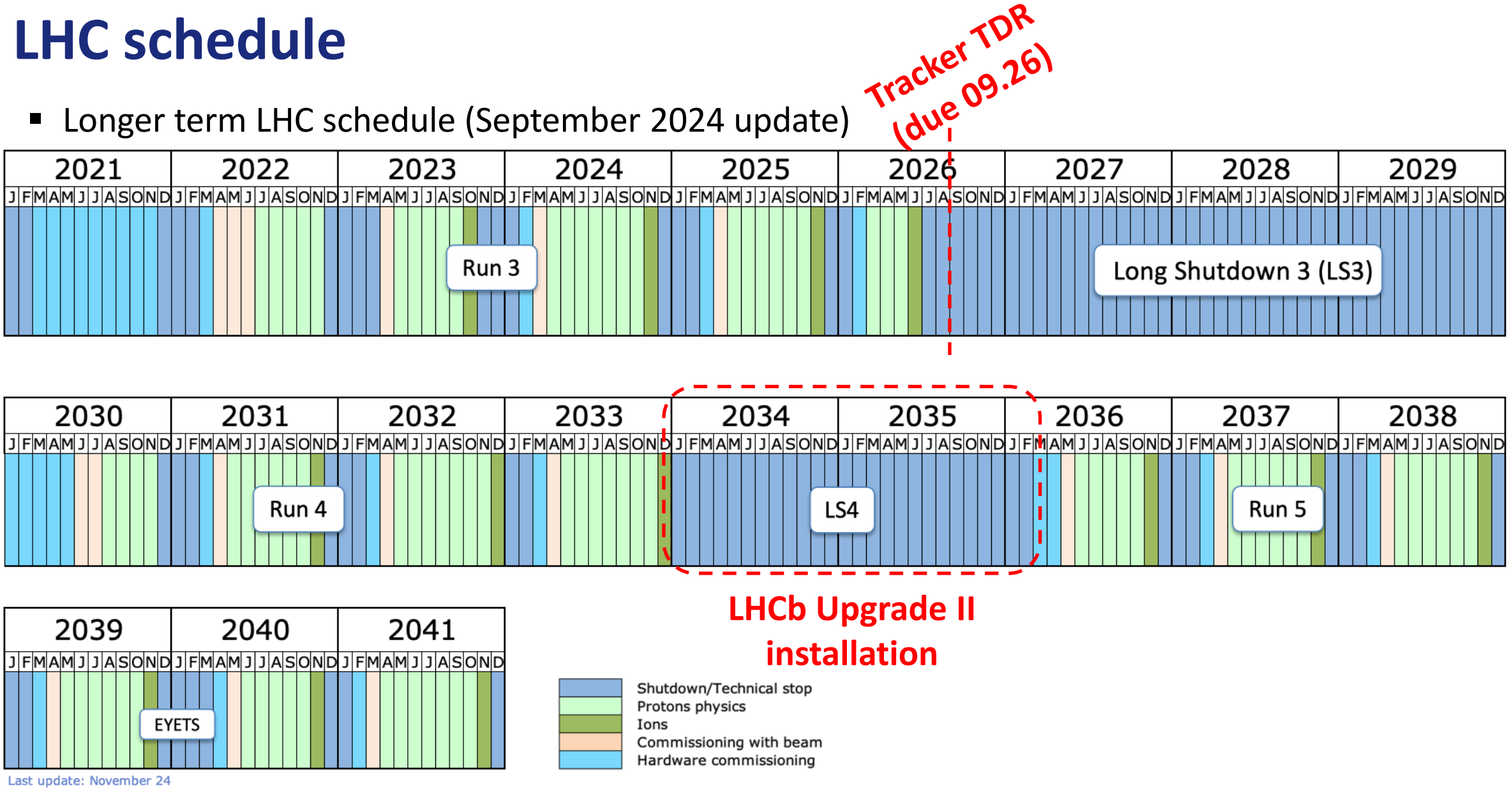
To accumulate a sample of 300 fb^{-1} of high energy pp collision data

Out of date!

- **Run 5 and Run 6** → Much increased instantaneous (peak) and integrated (recorded) luminosity
  - Unprecedented and unique discovery potential (precision searches for new physics in the flavour sector, direct searches for dark sector particles and QCD studies)
- To handle the much-increased particle flux and radiation level → **A second major upgrade is necessary** (detector technology with improved granularity and radiation tolerance)

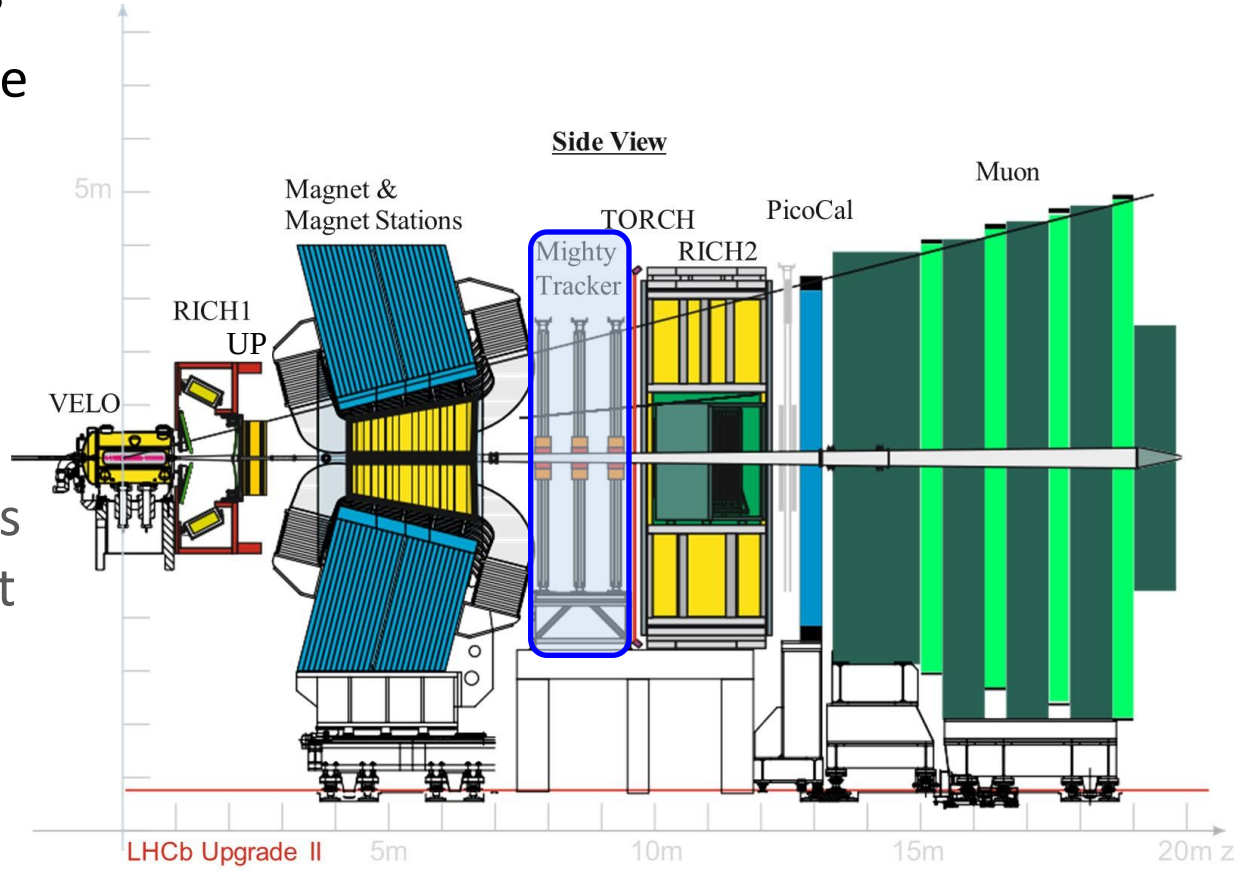
LHC schedule

- Longer term LHC schedule (September 2024 update)



LHCb Upgrade II

- Maximum peak luminosity of 1.5×10^{34} cm^{-2}s^{-1}
- Key features for successful physics programme
  - Efficient tracking of charged particles
  - Correct association of secondary heavy flavour decays to their primary vertices
  - Excellent particle ID
- Same footprint as existing spectrometer
  - Tracking system = VELO + tracking stations upstream and downstream of the magnet (UP + **Mighty-Tracker**)
  - PID system = RICH1 + RICH2 detectors upstream and downstream
  - Electromagnetic calorimeter (PicoCal)
  - Muon stations
  - Time-of-Flight detector (TORCH)

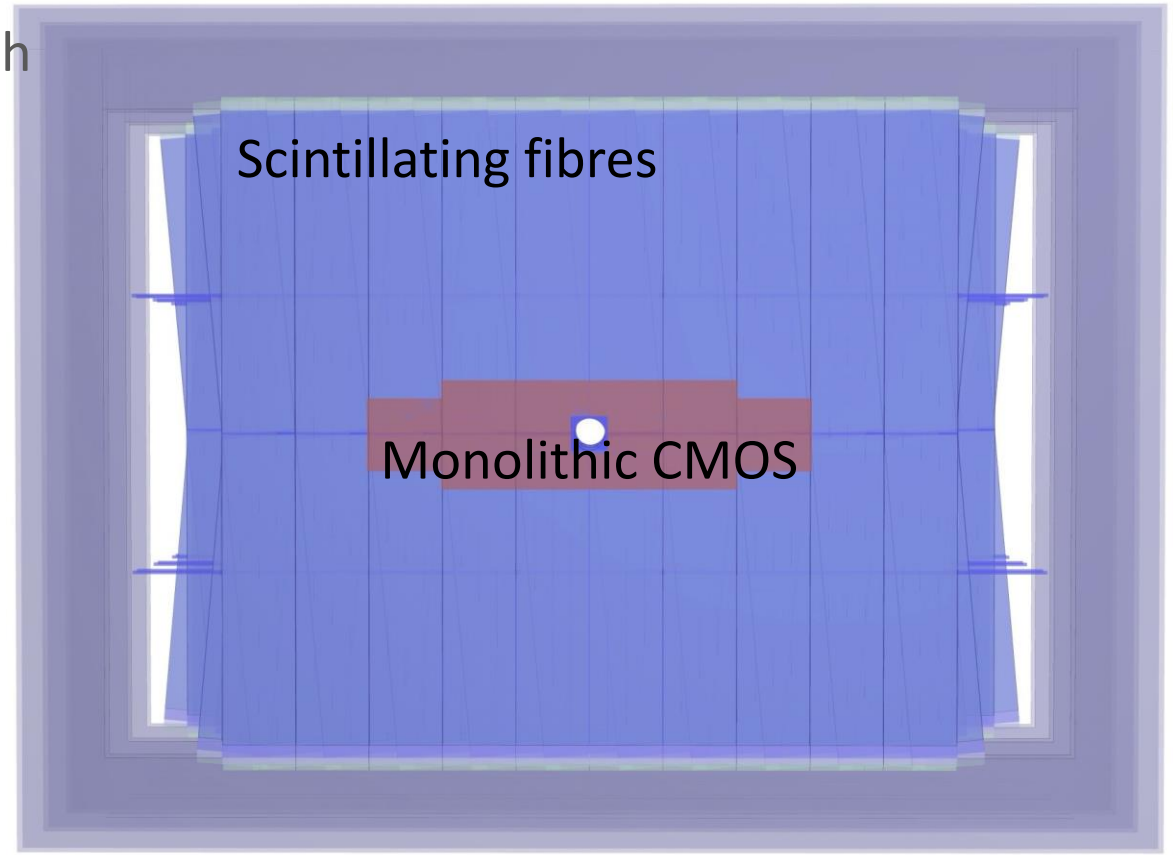


The LHCb Upgrade II (layout view)

Mighty-Tracker

- **New hybrid detector** for LHCb Upgrade II
  - To cope with high particle density and high radiation damage, and to minimise incorrect matching of upstream and downstream track segments
- **Mighty-Pixel: Inner Mighty Tracker region**
  - High granularity
  - High radiation tolerance

  → **Monolithic CMOS**
- **Mighty-SciFi: Outer Mighty Tracker region**
  - **Scintillator fibres**, as in Run 3, but with significant improvements
- Installation at tracking stations T1 to T3 (six layers)

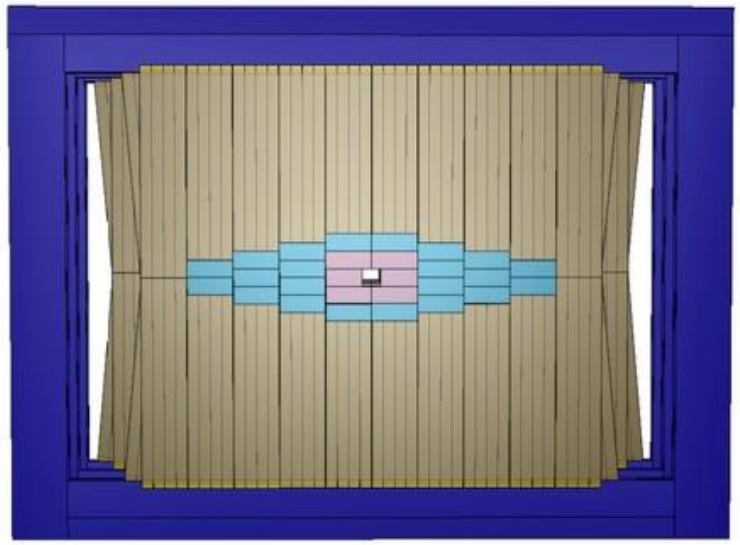


The Mighty Tracker – Scoping document baseline design (from Tai-Hua Lin)

Mighty-Pixel: *Detector scenarios*

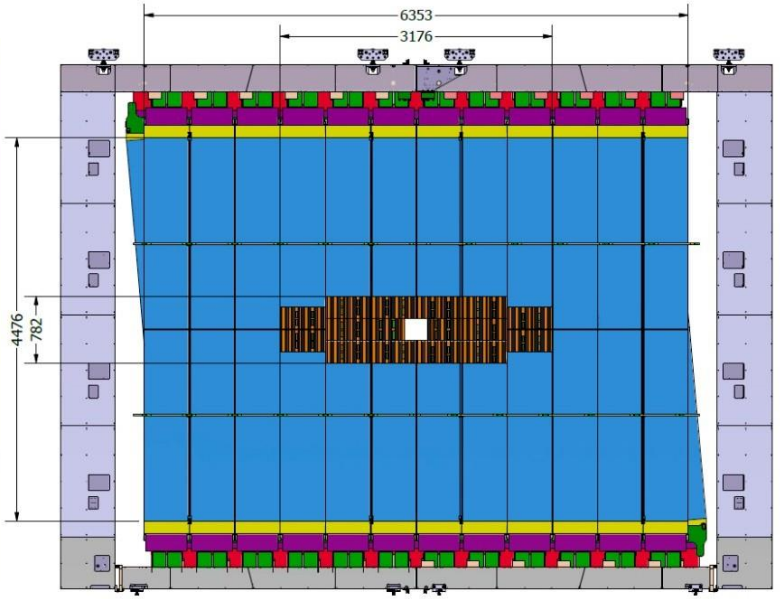
- Different scenarios for Mighty-Pixel region

FTDR baseline:
18 m^2

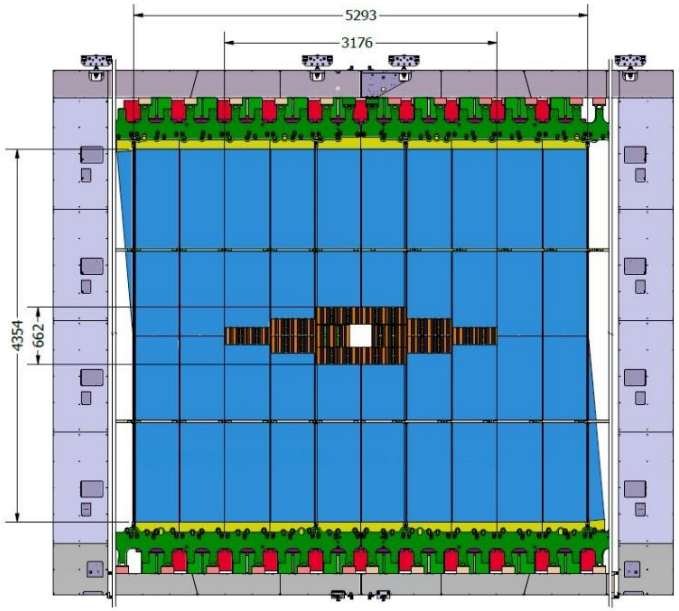


LHCb Upgrade II FTDR

Scoping document baseline:
12.6 m^2



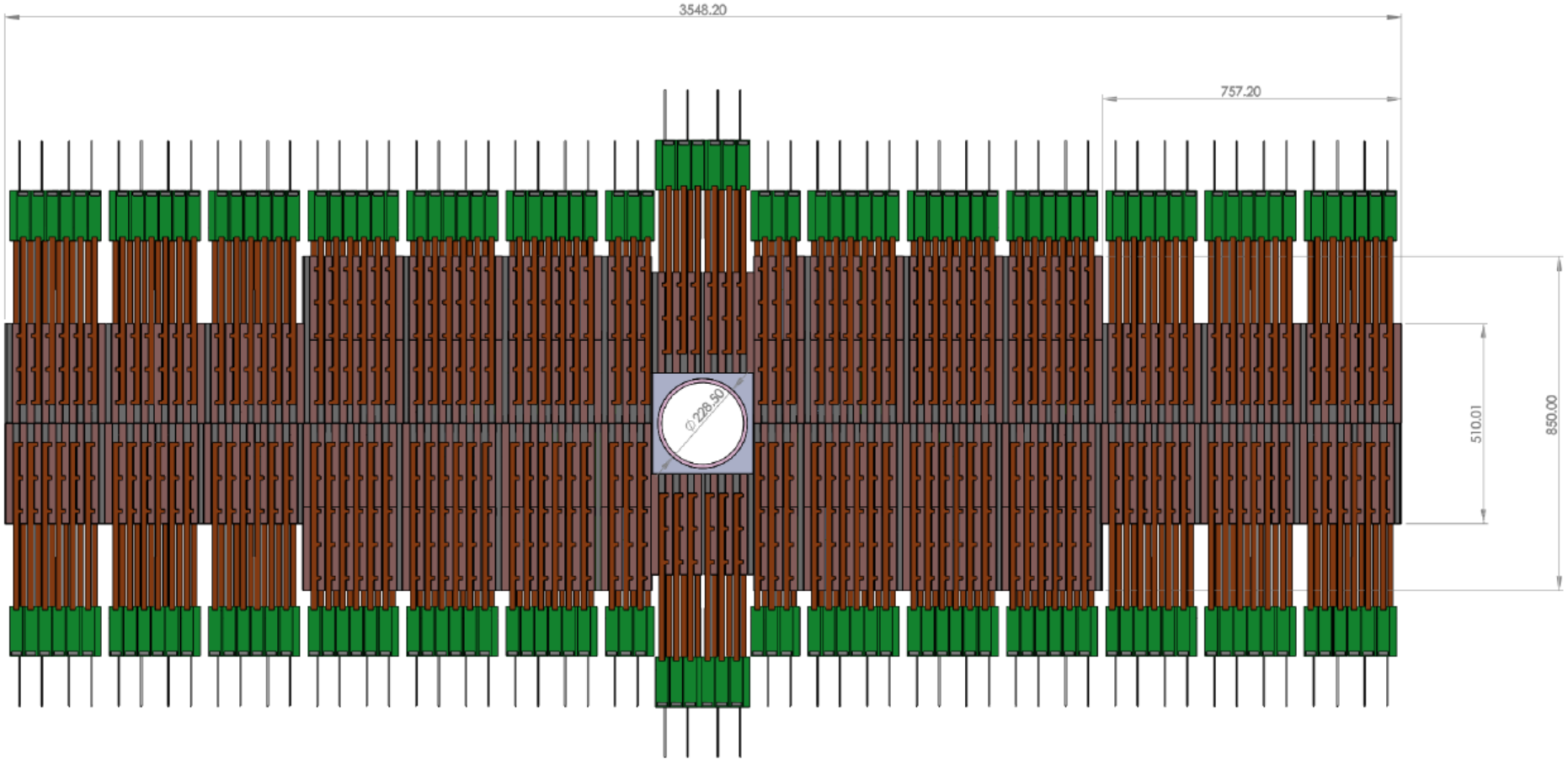
Scoping doc. low:
7.8 m^2



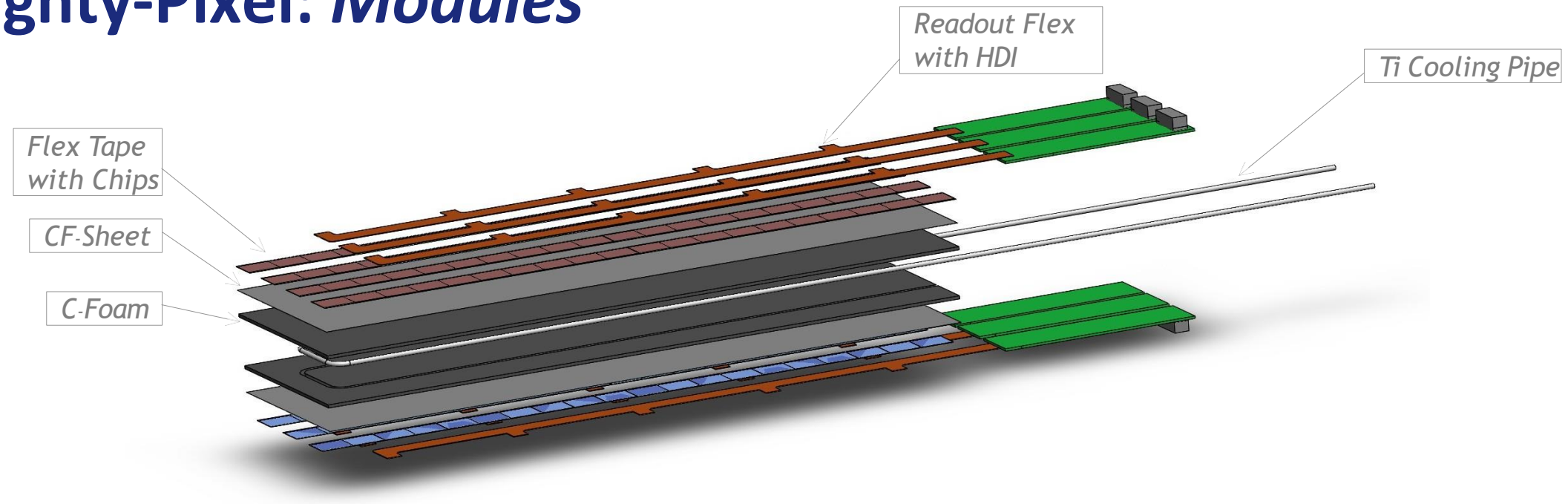
LHCb Upgrade II Scoping Document

Mighty-Pixel: *Modules*

- Stave topology (new for the Mighty-Tracker)
  - Elongated support structure that houses multiple monolithic CMOS sensors
  - Allows moving readout electronics away from high occupancy region



Mighty-Pixel: *Modules*



- Staves are double-sided, with monolithic CMOS sensors on the front and back, to avoid acceptance gaps
- Sensors are glued to the flex tapes/circuits
- Staves are made of carbon-fibre, and come with integrated cooling
- Distribution of electrical signalling and power is via High Density Interconnect Flexible PCBs
  - Integrated into the stave core (co-curing of flex onto a carbon-fibre face sheet)
  - Data links operating at 1.28 Gbit/s

Mighty-Pixel: *Sensor specifications*

- Updated specifications to be released as an internal LHCb note

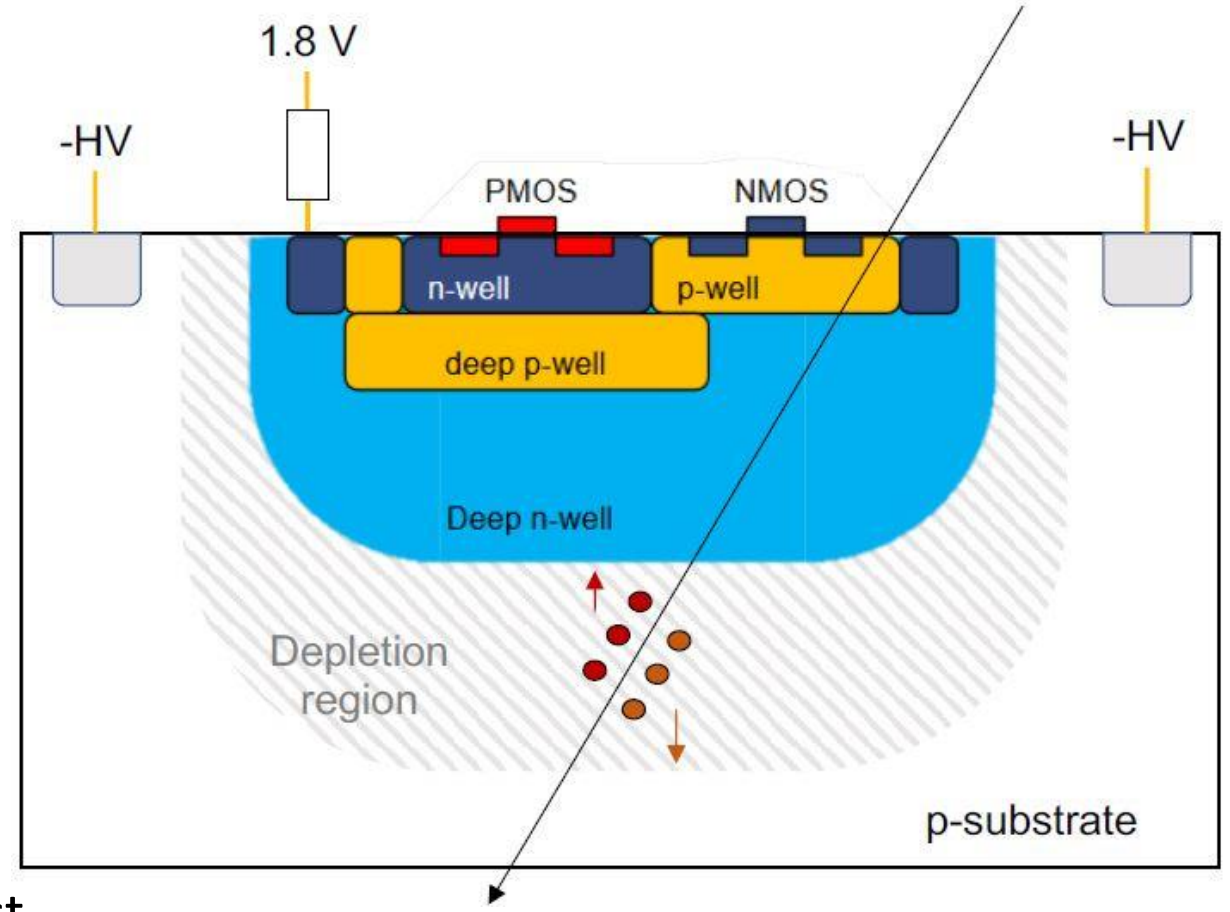
Parameter	Required value
Chip size	~ 2 cm × 2 cm
Pixel size	≤ 100 µm × 200 µm
Chip thickness	≤ 200 µm
Particle rate	17 MHz/cm^2
Hit rate	34 × 10^6 cm^{-2}s^{-1}
Data word length	32 bit
In-time efficiency	> 99% within 25 ns
Transmission rate	4 links per chip of 1.28 Gbit/s each
NIEL	3 × 10^{14} n_{eq}/cm^2
TID	40 Mrad
Power consumption	≤ 150 mW/cm^2

Mighty-Pixel: *Sensor specifications*

- **Compatibility with the LHCb readout system**
  - Run with the LHC clock at 40 MHz
  - Use the lpGBT protocol (low-power GigaBit Transceiver) for communication
    - lpGBT is a high-speed communication protocol and chip for data transmission between detectors and data acquisition systems in physics experiments
    - Maximum input voltage 1.2 V (HV-CMOS chip has VDD = 1.8 V)
    - Protocol compliance (VELO scrambler (8b/10b encoding), clock-data recovery, etc.)
    - I/O standards (LVDS, CML)
    - Clocking requirements and latency
    - Data rate (≤10.24 Gbps)
  - Meet Timing and Fast Control (TFC) + Experiment Control System (ECS)
    - TFC controls the entire readout of the LHCb detector. It is essential for ensuring that the entire detector is working in a synchronised manner, with minimal delays between collision events and data collection.
    - ECS manages and controls all sub-systems involved int eh experiment.

High Voltage CMOS technology

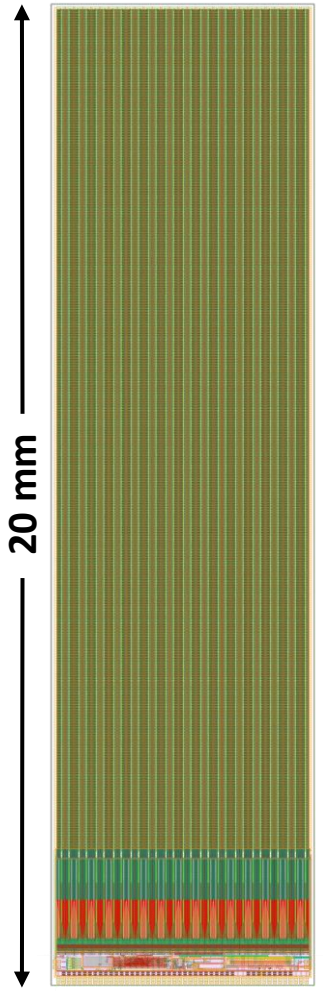
- Sensing and readout chip integrated in single device –sensors can be very thin (~ 50 µm), and pixel sizes very small (~ 50 µm × 50 µm)
- Deep n-well/p-substrate sensing junction
- High reverse bias voltage applies to the substrate creates thick depletion region –good radiation tolerance
- Deep n-well hosts readout electronics, which are isolated from substrate high bias voltage
- Charged particles create electron/hole pairs, collected via drift –fast charge collection
- Fabricated in industry standard processes –fast production, high yields, cheaper than other technologies



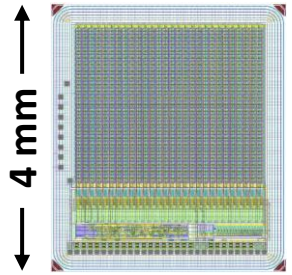
Typical cross-section of an HV-CMOS sensor

Mighty-Pixel: *Sensor R&D*

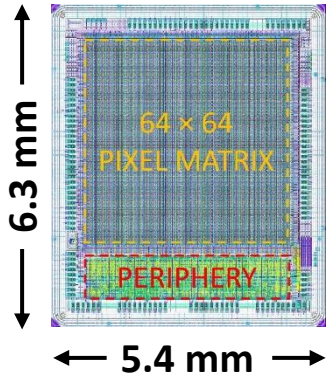
- **MightyPix (180 nm HV-CMOS ams OSRAM)**
  - Based on existing designs developed by Ivan Peric's group at KIT (ATLASPix proposed for ATLAS, MuPix produced for Mu3e)
  - MightyPix1 (full-length, ¼ width) is available, in 180 nm HV-CMOS from TSI* (ams OSRAM and TSI are largely compatible), largely compatible with LHCb, performance has been evaluated
- **LF-MightyPix (150 nm HV-CMOS LFoundry S.r.l.)**
  - To study portability between ams OSRAM and LFoundry S.r.l. (project de-risking) + new LHCb features, currently being fabricated
- **RadPix (150 nm HV-CMOS LFoundry S.r.l.)**
  - Derivative of CERN-RD50 HV-CMOS sensor, currently being adapted to LHCb



MightyPix1



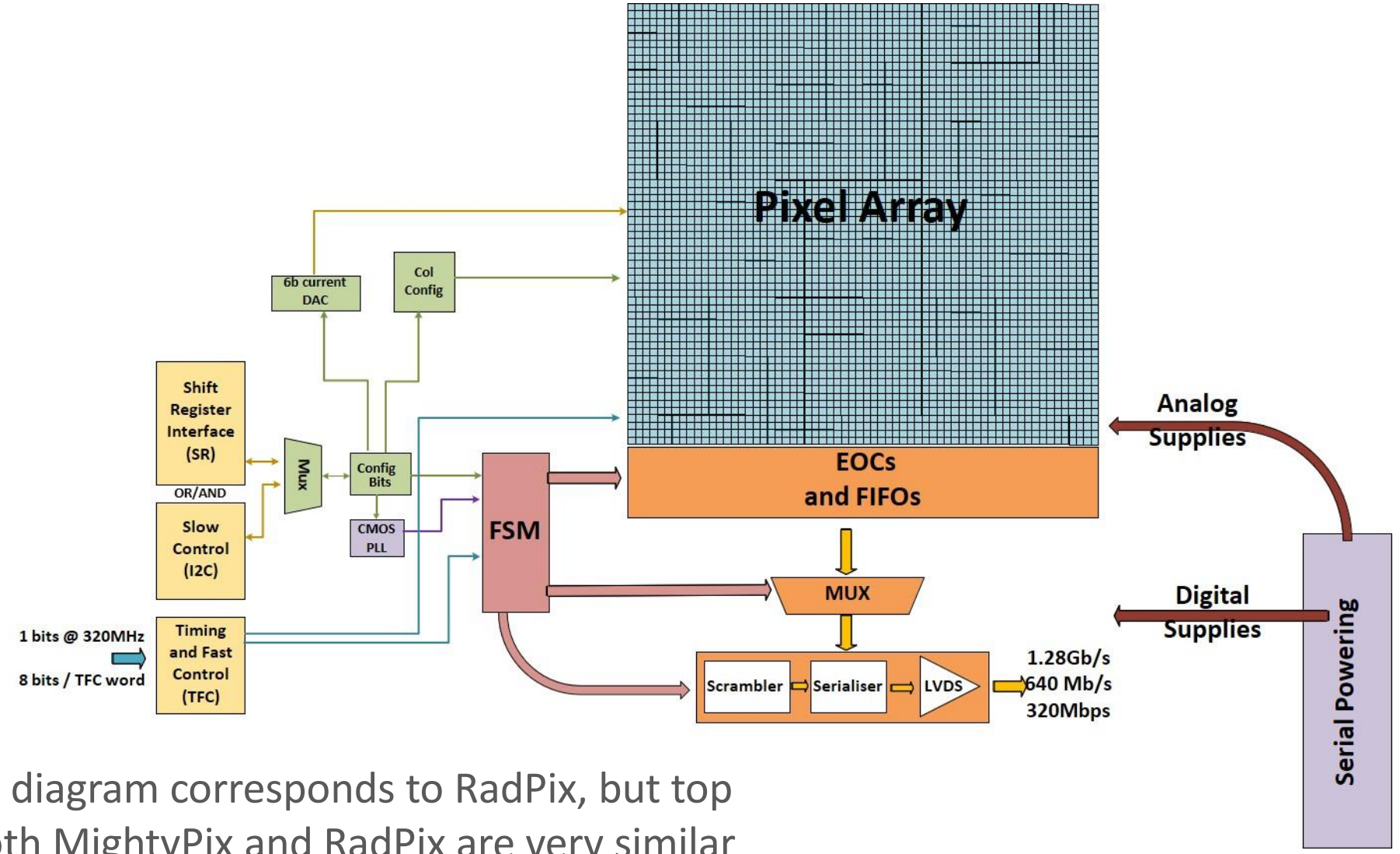
LF-MightyPix



RD50-MPW4

*TSI discontinued their 180 nm HV-CMOS process end of 2023

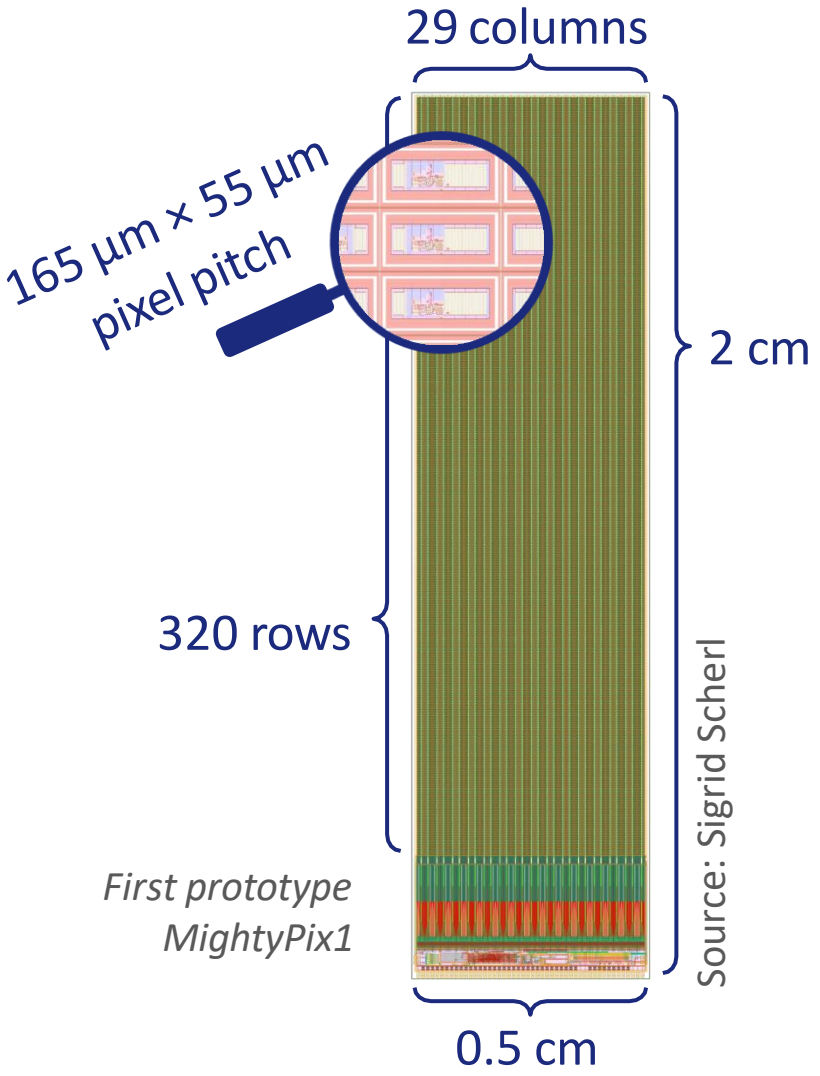
Mighty-Pixel: *Top level view*



Schematic diagram corresponds to RadPix, but top level of both MightyPix and RadPix are very similar

MightyPix1: *Overview*

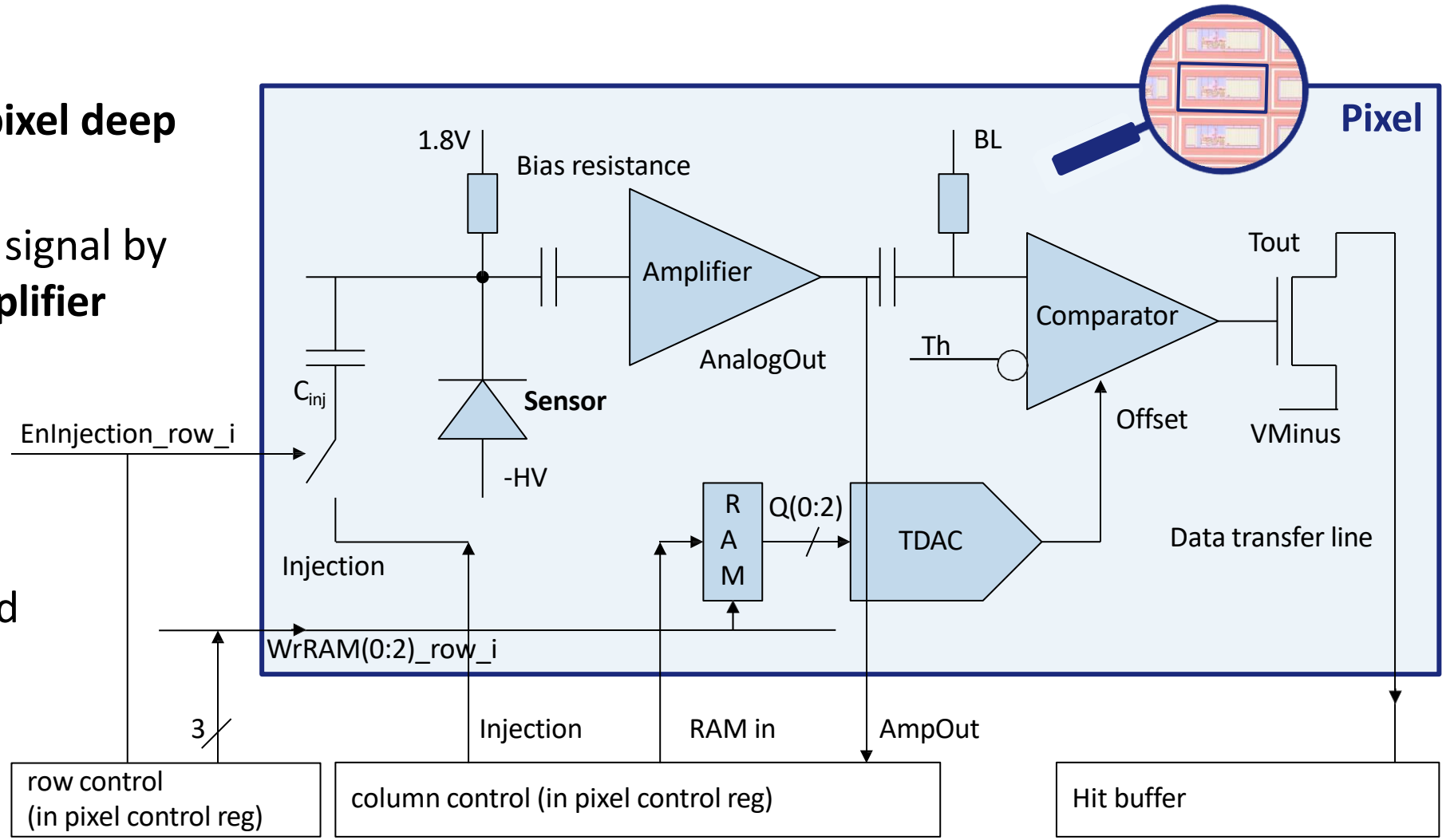
- **Pixel electronics**
  - CMOS amplifier and CMOS comparator
- **Data format**
  - 2 x 32 bit words per hit
- **Data output rate**
  - 1.28 Gbit/s going to lpGBT
- **Digital interfaces**
  - TFC: Timing and Fast Control
  - I2C: Slow control
  - SR: Config. shift register interface
- **Clock generation**
  - External: 40 MHz and 640 MHz coming from lpGBT
  - Internal: CML and CMOS PLL with 40 MHz reference clock
- **Bias voltages**
  - Integrated 10 bit voltage DACs



MightyPix1: *Analogue readout*

Hit detection

- Charge collected by **pixel deep n-well**
- Converted to voltage signal by **Charge Sensitive Amplifier**
- Analogue voltage pulse converted to digital signal by **comparator**
- Hit information stored in **hit buffer**



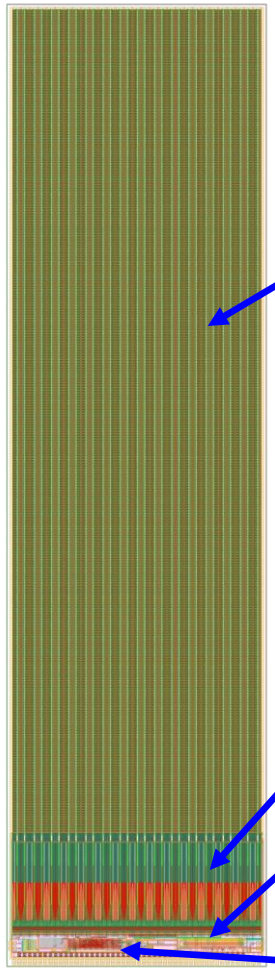
Schematic of the MightyPix1 Analogue Pixel (Adapted from: Ivan Peric, KIT)

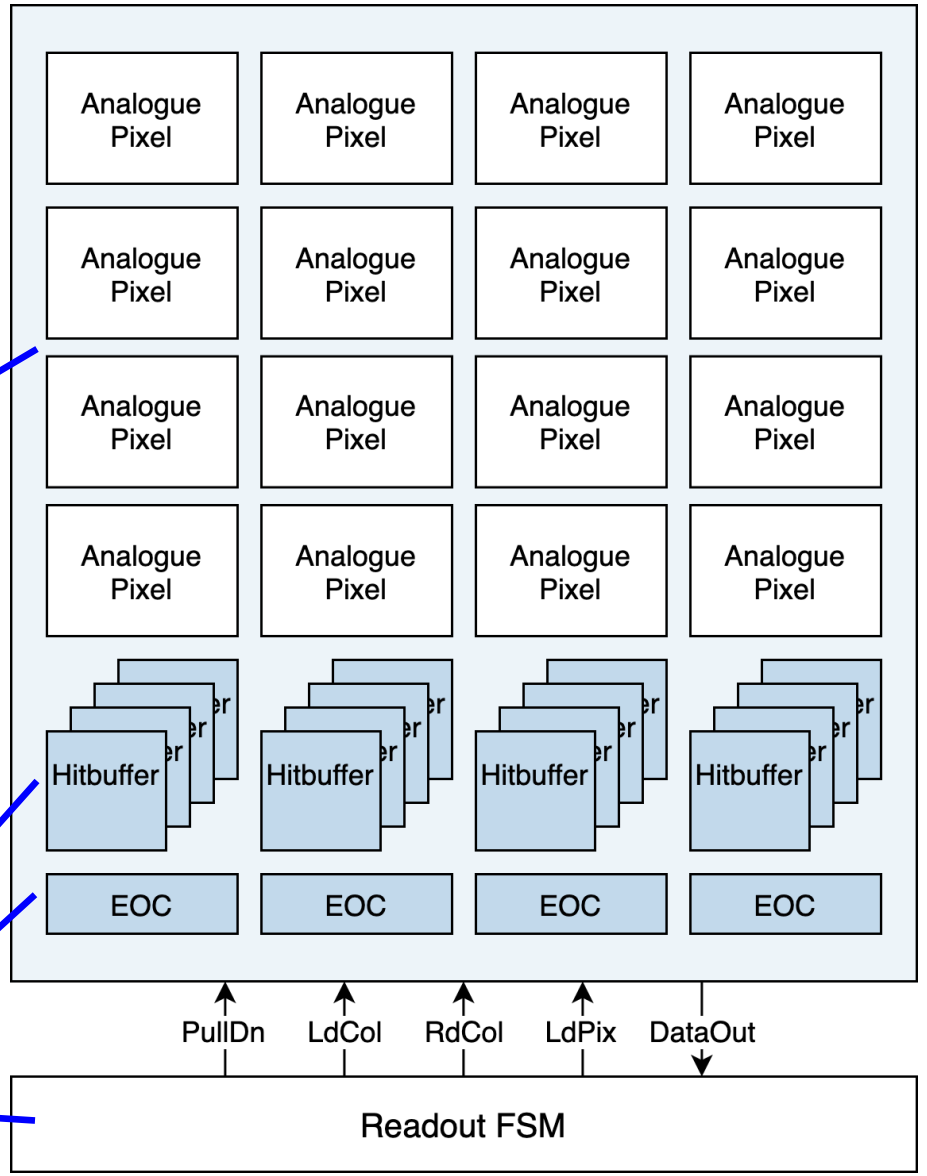
MightyPix1: *Digital readout*

- Readout driven by Readout Control Unit (RCU) Finite State Machine (FSM)

Working principle

- Hit information stored in **hit buffer**
- Data loaded from highest active hit buffer to End of Column (EoC) buffer
- Read data from EoC
- For every hit 2 x 32 bit data word is generated
- Parallel scrambler analogue to VELOPix
- Data sent to serialiser tree and sent out



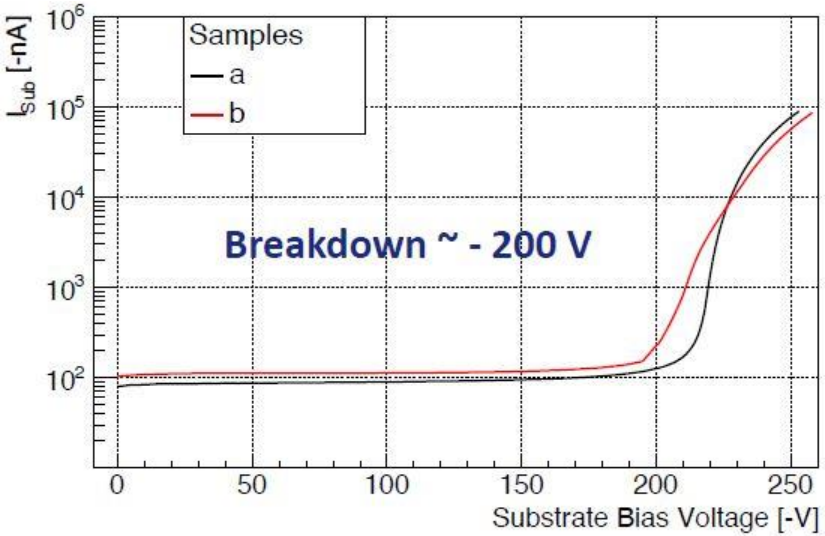


Source: Nicolas Striebig

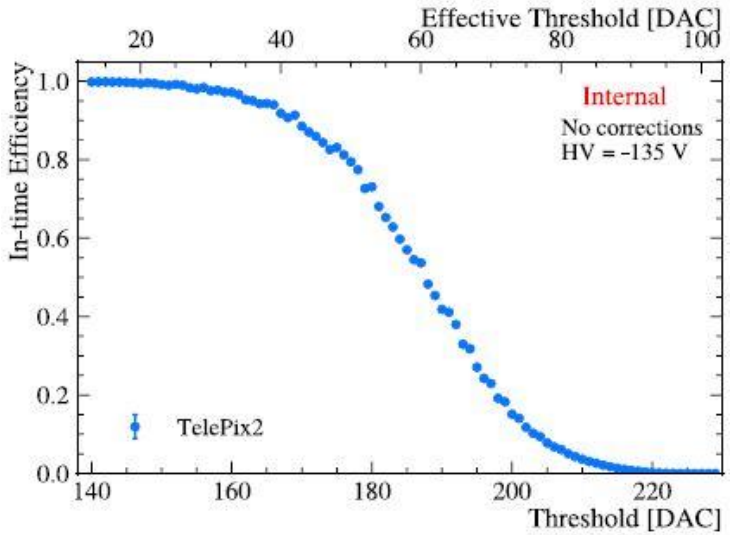
MightyPix1: *Evaluation*

- Basic functionality and digital interface successfully tested
- Evaluation with other *similar* HV-CMOS chips as well (TelePix2)
  - In-time efficiency > 99.9%
  - Irradiated TelePix2: In-time efficiency at test beam in December 2024

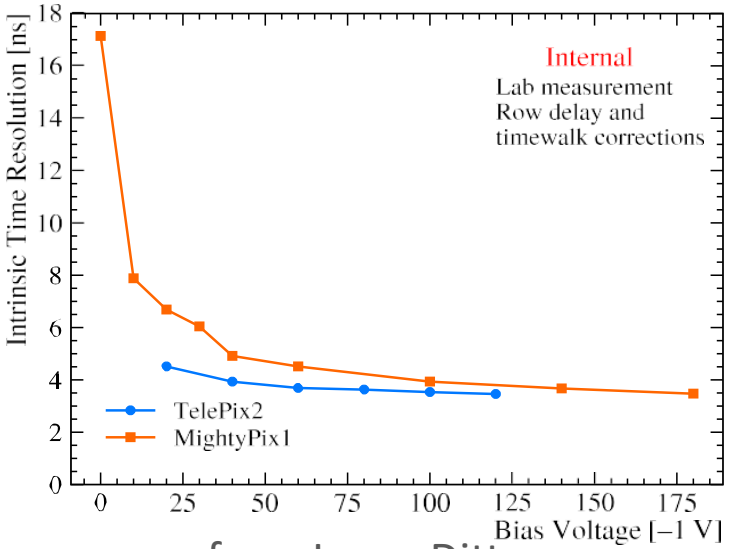
Parameter	MightyPix1	TelePix2
Chip size	0.5 cm × 2 cm	2 cm × 1 cm
Pixel size	165 µm × 50 µm	165 µm × 25 µm
Breakdown	-210 V	-150 V
Amplifier	CMOS	CMOS
Comparator	CMOS	CMOS



from Jan Hammerich



from Lucas Dittman

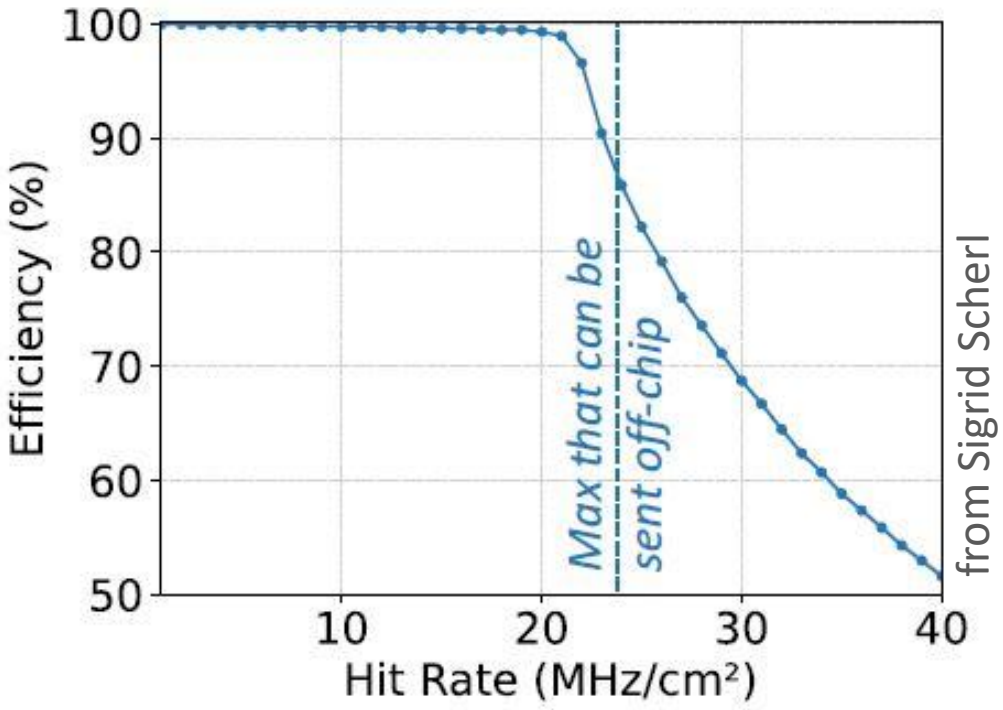


from Lucas Dittman

MightyPix1: *Efficiency simulations*

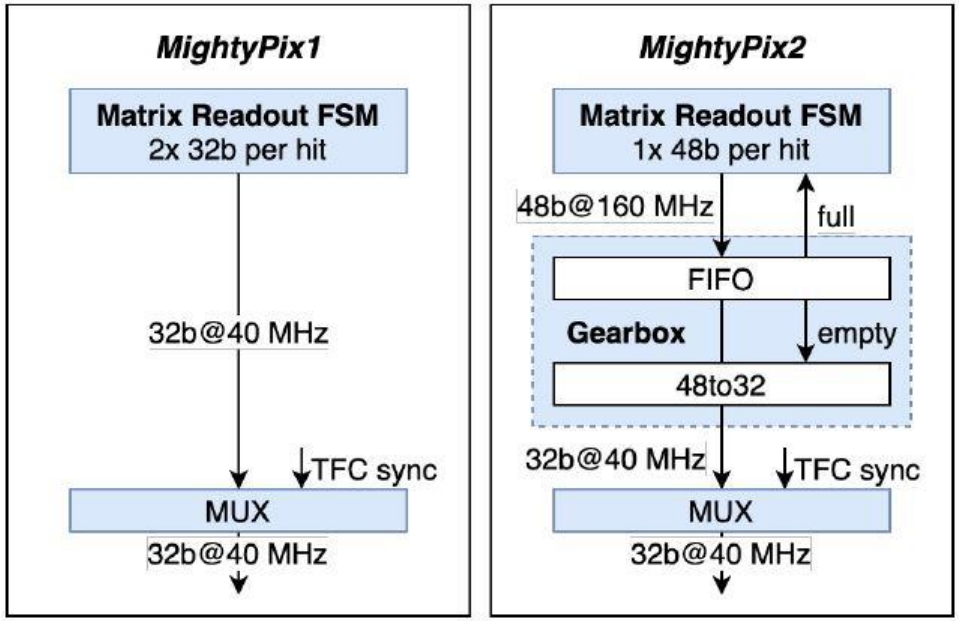
- **Can MightyPix1 handle the expected Mighty-Tracker rates of 17 MHz/cm²?**
  - Simulation of MightyPix1 digital readout with LHCb simulated particle hits

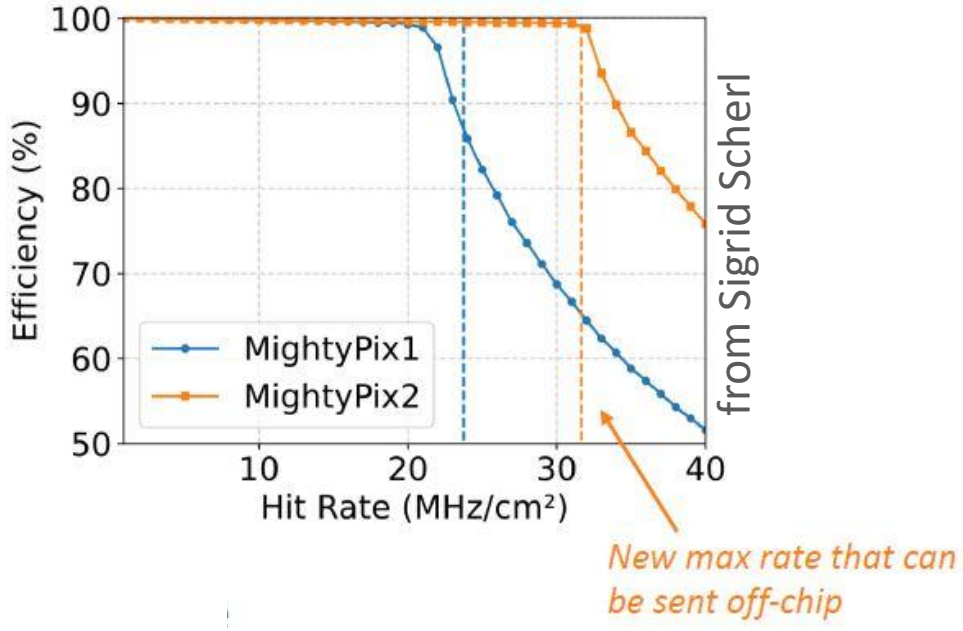
- Simulated efficiency of MightyPix1 readout mechanism > 99% up to 20 MHz/cm²
- Drop at 20 MHz/cm² as readout times reach 89.1 µs
  - Hit buffers are not fast enough → new hits are missed
- Need faster readout for larger safety margin



Towards MightyPix2: *New readout*

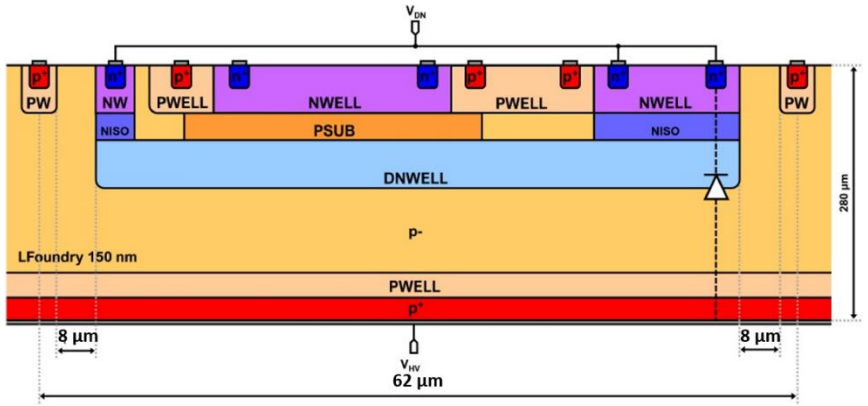
- **Decreased data size**
  - 2 x 32 bit per hit → 1 x 48 bit per hit
  - Can send up to 31.66 MHz/cm^2 off-chip
- **Increased FSM readout speed**
  - 32 bit at 40 MHz → 48 bit at 160 MHz
  - Hit buffers read out faster, less hits missed
- **New on-chip memories**
  - 16-bit depth FIFOs which store hits before they are sent off-chip
- Simulated efficiency of improved readout mechanism > 99% up to 31.66 MHz/cm^2 → larger safety margin
  - Drop as 1.28 Gbit/s readout link works at full capacity

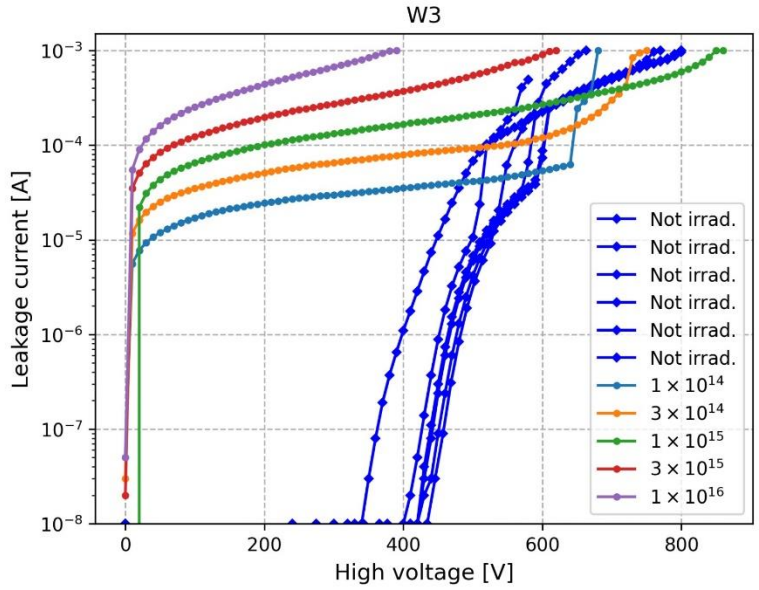




RadPix: *Based on CERN RD50-MPW4 design*

- **High breakdown voltage and high radiation tolerance**
  - Multiple ring structure around the chip edge
  - Substrate backside-biasing to high voltage
- **Fabrication details**
  - 150 nm High Voltage CMOS LFoundry (LF15A)
  - P-type substrate with nominal 3 kΩ·cm high resistivity
  - 280 µm thin
- **Chip contents**
  - Pixel matrix with FE-I3 style readout
    - 64 x 64 pixels
    - 62 µm x 62 µm pixels with large collection electrode
    - Analogue and digital readout embedded in sensing area
  - Digital periphery (I2C slow control, data transmission)
- **Irradiation campaign**
  - Neutrons → several fluence from 1×10^{14} to 3×10^{16} n_{eq}/cm^2

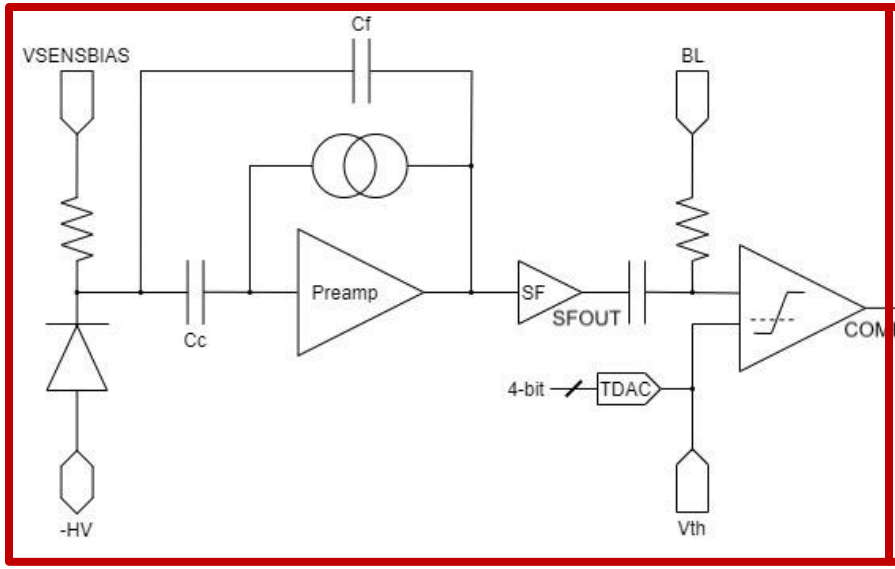




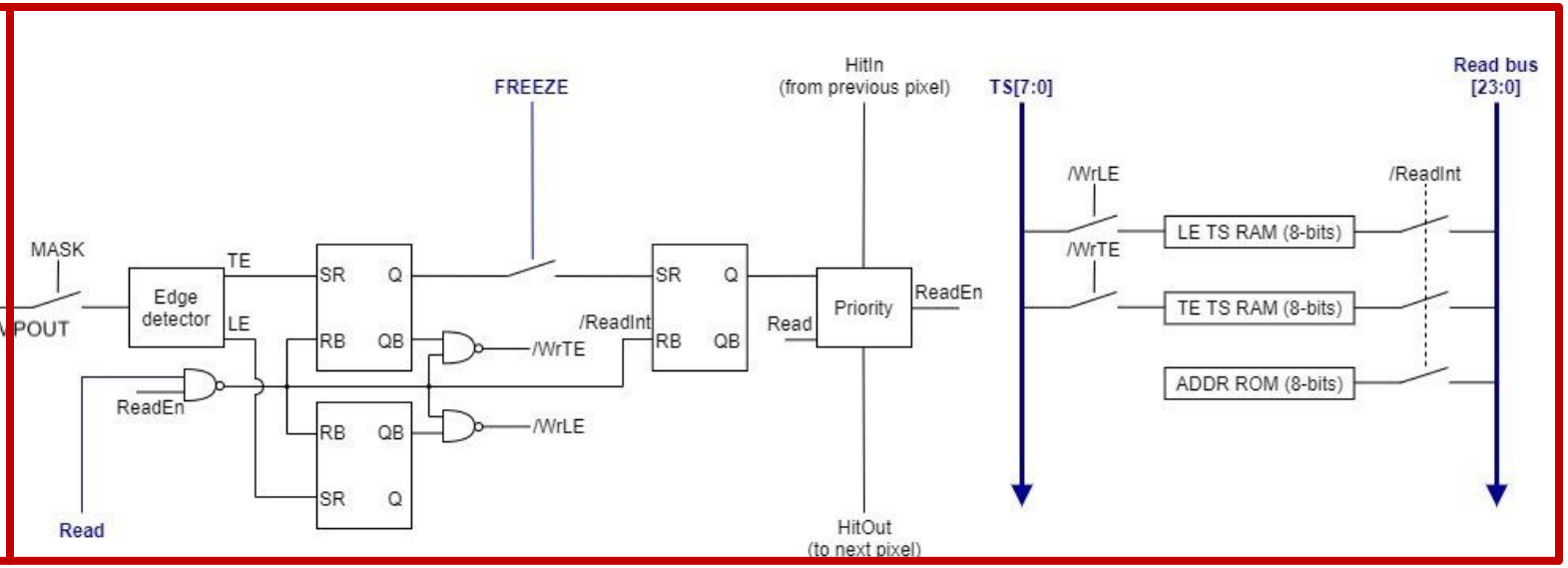
RD50-MPW4: *Pixel electronics*

Hit data = 8-bit LE time-stamp + 8-bit TE time-stamp + 8-bit pixel address

Analogue readout



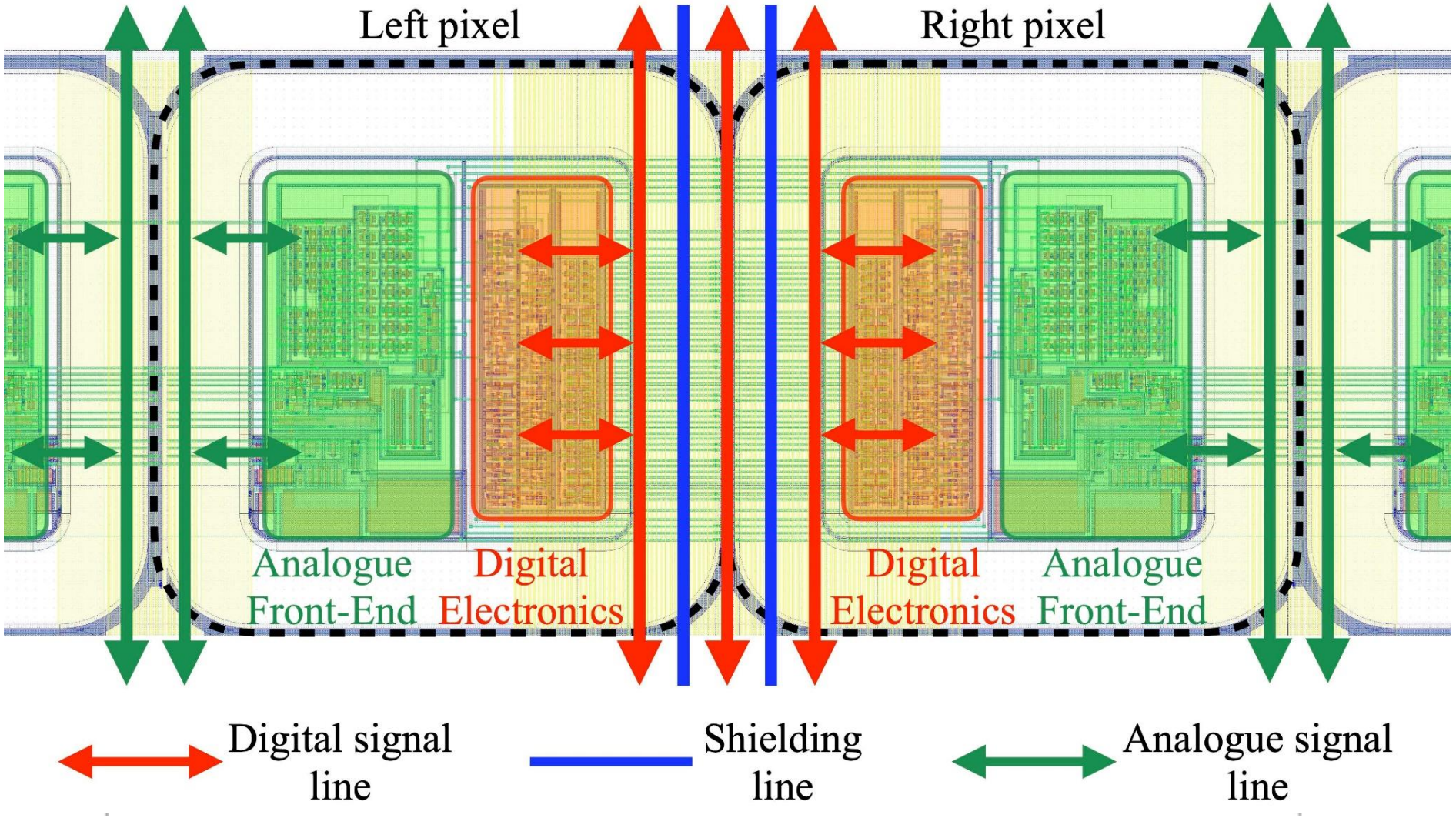
Digital readout



Time-stamp @ 40 MHz, Gray encoded

- **Column drain architecture (FE-I3 style)**
- **Electronics to**
  - Mask noisy pixels (MASK)
  - Possibility to pause digitisation of new hits until readout is complete (FREEZE)
  - 8-bit SRAM shift register for serial configuration (not drawn in schematic)
    - Pixel-trimming to compensate for threshold voltage variations (4-bits)
    - Flag to mask noisy pixels (1-bit)
    - Signals to enable/disable calibration circuit (1-bit), SFOUT (1-bit), COMPOUT (1-bit)

RD50-MPW4: *Pixel layout*

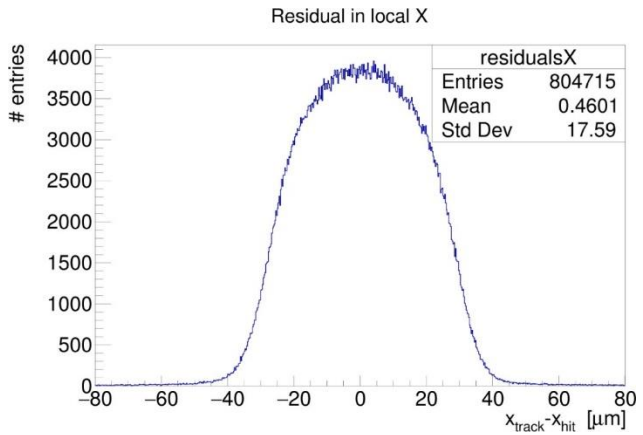


Double column scheme to alleviate routing congestion and minimise crosstalk

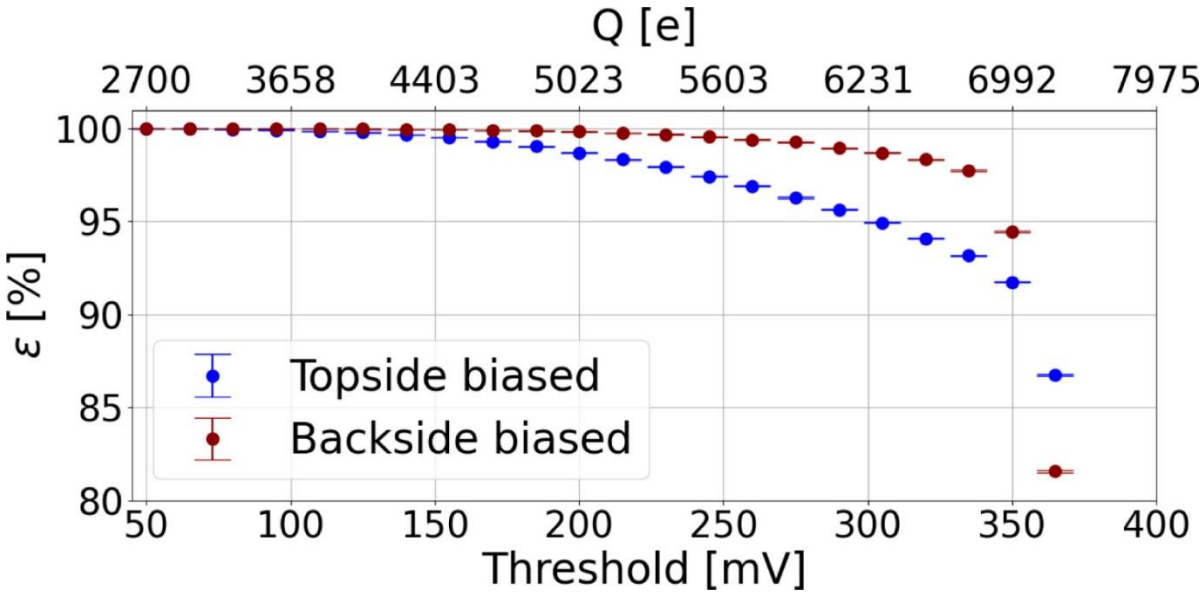
RD50-MPW4: *Evaluation*

- **Test beam: *Experimental methods***
  - *Beam* 4.2 GeV electrons (DESY, April '24)
  - *DUT* Un-irradiated RD50-MPW4
    - V_HV = -190 V
    - V_TH = 50 mV = 2500 e-
  - *DAQ* Caribou
  - *Trigger* 2-scintillators via AIDA2020-TLU
  - *Telescope* Adenium (6 Alpide planes)
  - *Analysis* Corryvreckan

Binary resolution (62 µm /√12 = 17.9 µm) is exceeded due to cluster size of 1.3 pixels & charge weighted centre of gravity calculation for the cluster positions



- **Test beam: *Results***
  - Efficiency >99% up to V_TH = 200 mV = 5000 e-
  - Efficiency drop at higher V_TH due to degraded efficiency at pixel corners
  - **Backside biasing gives more uniform electric field → Better efficiency**



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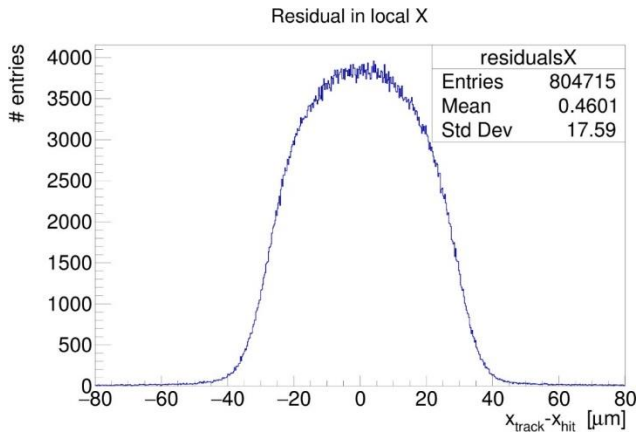
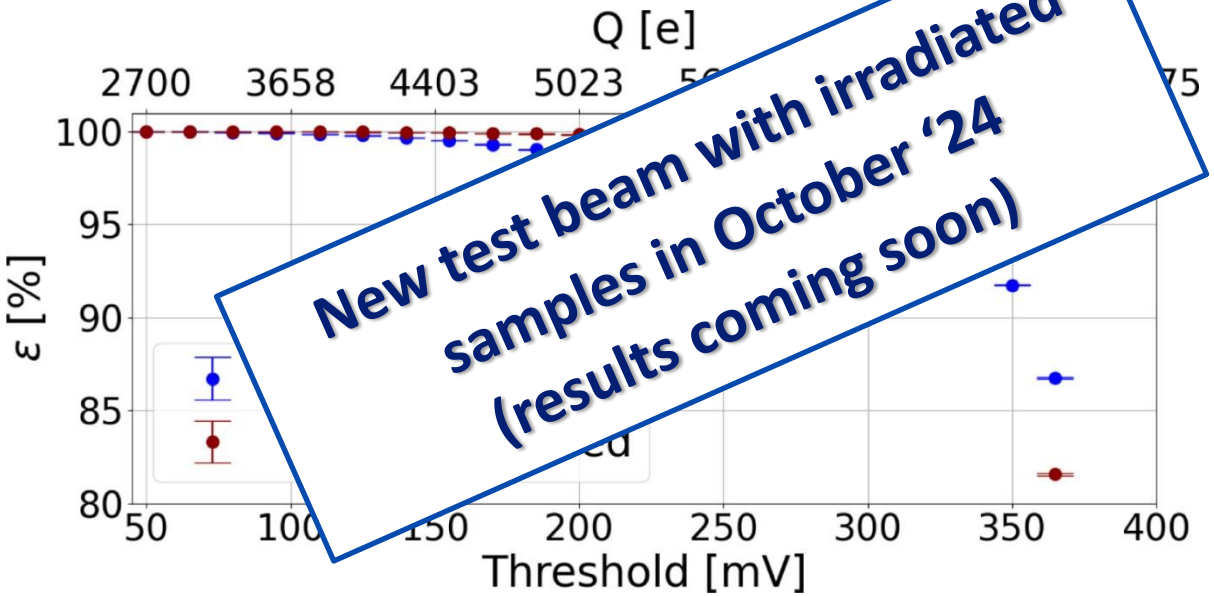
  - *DUT* Un-irradiated RD50-MPW4
    - V_HV = -190 V
    - V_TH = 50 mV = 2500 e-
  - *DAQ* Caribou
  - *Trigger* 2-scintillators via AIDA2020-TLU
  - *Telescope* Adenium (6 Alpide planes)
  - *Analysis* Corryvreckan

Binary resolution (62 µm /√12 = 17.9 µm) is exceeded due to cluster size of 1.3 pixels & charge weighted centre of gravity calculation for the cluster positions



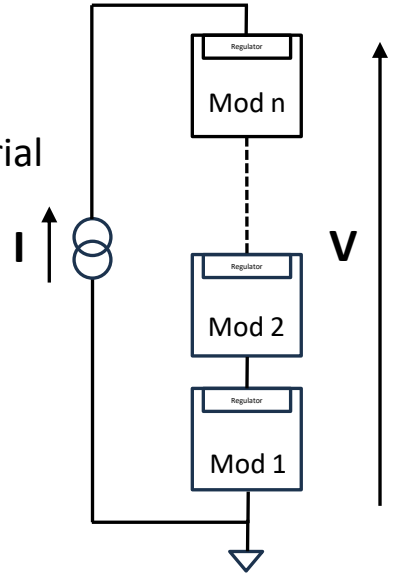
- **Test beam: *Results***
  - Efficiency >99% up to V_TH = 200 mV = 5000 e-
  - Efficiency drop at higher V_TH due to degraded efficiency at pixel corners
  - **Backside biasing gives more uniform electric field → Better efficiency**



Mighty-Pixel: *Powering*

- Motivation
  - Point-to-point or parallel powering of multiple modules is highly inefficient and not viable
  - DCDC works, but still not a low-mass solution (mainly due to shield box and coil)
- **Proposal to use serial powering**
  - A low-mass high-efficiency solution, but with increased system complexity
  - Modules powered in series by a constant current with voltage conversion done on CMOS sensor

Schematic of Serial Powering

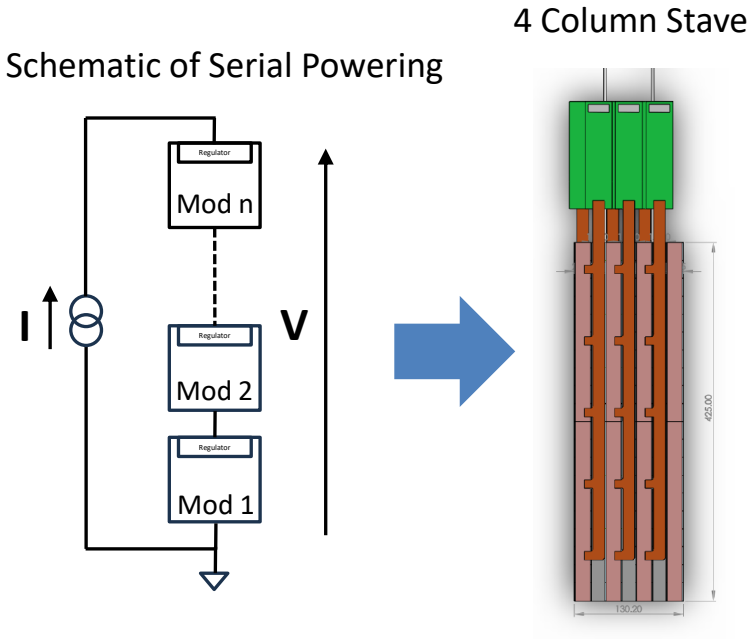


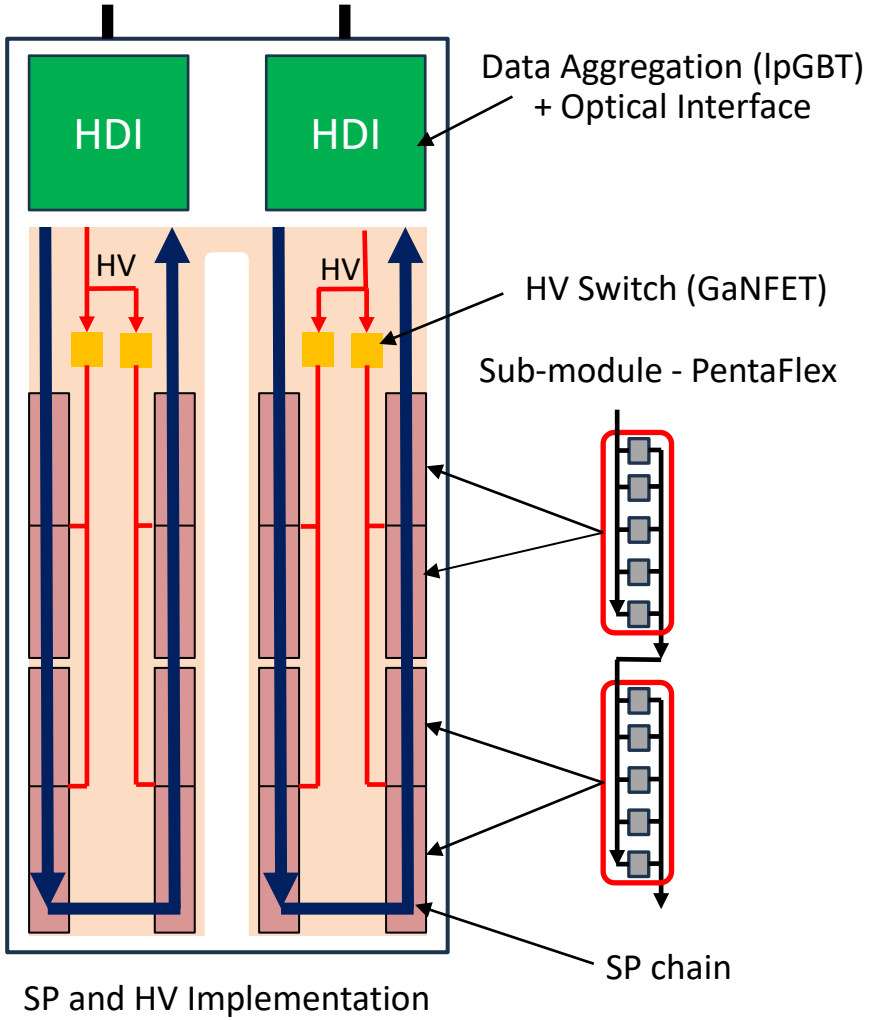
For reference, from ATLAS Phase II Upgrade ITk Pixels:

- *Serial Power modules come as quads wired in parallel*
  - For redundancy (failure of power regulation)
  - A single ASIC should be able to carry full module current
- *Up to 16 modules per SP chain, trade off between efficiency and risk*
  - Need to be careful of volt drop across modules - introduces a 'ground rise'
  - Attenuating the on-module HV as it traverses the SP chain
- *Two HV lines per chain*
  - One HV 8 modules

Source: Ashley Greenall

Mighty-Pixel: *Powering and HV of a stave*





SP and HV Implementation

- Columns of 20 ASICs split into smaller sub-modules
  - 5 x ASICs per sub-module (PentaFlex)
    - ASICs wired in parallel – current sharing
  - 4 x sub-modules/column
- 2 serial chains per stave, 8 sub-modules per chain
- 1 x HV feed per serial chain
  - Switched across 2 columns

Source: Ashley Greenall

Mighty-Pixel: *Planned prototypes*

- **MightyPix**
  - MightyPix2
    - Large MightyPix prototype
    - Submission planned for Q1 2025
    - 180 nm HV-CMOS from ams OSRAM
    - Implements new readout mechanism
    - 4 x 1.28 Gbit/s readout links per chip
  - MightyPix3
    - Could be final MightyPix prototype
    - Submission planned for Q1 2026
    - 180 nm HV-CMOS from ams OSRAM
- **RadPix**
  - RadPix1
    - ¼ or large RadPix prototype
    - Submission planned for Q3 2025
    - 150 nm HV-CMOS from LFoundry S.r.l.
    - Largely compatible with LHCb readout
    - (Largely) compatible with UP specifications
    - Implements voltage regulators
  - RadPix2
    - Could be final RadPix prototype
    - Submission 12-18 months after RadPix1
    - 150 nm HV-CMOS from LFoundry S.r.l.

Summary and outlook

- **The Mighty-Tracker is a new hybrid tracker planned for LHCb Upgrade II**
  - Mighty-Pixel
  - Mighty-SciFi
- **HV-CMOS R&D for Mighty-Pixel**
  - 180 nm HV-CMOS from ams OSRAM
    - MightyPix1 fabricated and tested
    - MightyPix2 currently being designed
    - Similar prototypes in this process also being evaluated
  - 150 nm HV-CMOS from LFoundry S.r.l.
    - LF-MightyPix currently being fabricated
    - RD50-MPW4 currently being tested
    - RadPix1 currently being designed, for the Mighty-Tracker and the UP

Back up slides

Requirements – From physics (discussion in progress)

- **RadPix must have (for UP):**

- Main differences between MT and UT

Key numbers :

Characteristics	Specification
Hit rate in hot event and region	160 MHz / cm^2 pp * (~52.5 hits / cm^2 / BX for Pb/Pb)
Time resolution	O(1 ns) for BX tagging (> 99% In-Time Eff.)
Space resolution	~ 5 µm
Power consumption	O(100-300 mW/cm^2)
Radiation dose for 350 fb^{-1}	3×10^{15} 1-MeV n$_{eq}$/cm^2, 240 Mrad

Hit rate

** From FDTR ; the hit density is currently under revision*

From LHCb upgrade electronics workshop 2024 (Fabrice Guilloux)