# Status of ARCADIA project


## Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

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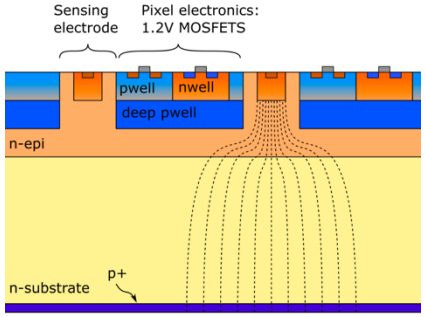
# ARCADIA DMAPS R&D

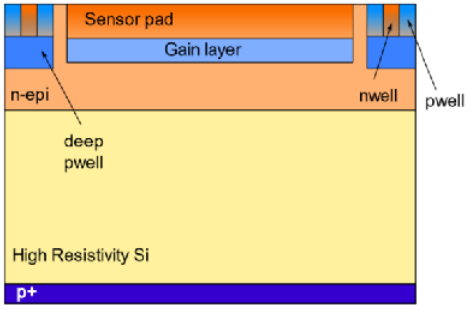
**ARCADIA: Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays**

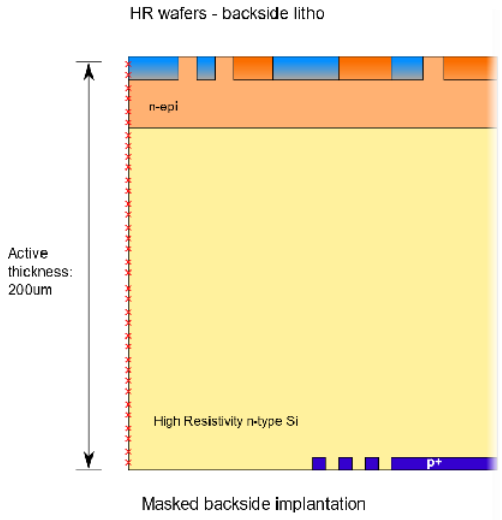
- CMOS sensor design and fabrication using LF 110nm technology
  - Sensor R&D, CMOS IP Design, Chip Integration, Data Acquisition
  - MD3: demonstrator full-chip FDMAPS for Medical (pCT), future leptonic colliders and space instruments
  - Scalable FDMAPS architecture with very low-power: 10 mW/cm2
  - Fully-depleted monolithic active micro strips with fully-functional embedded readout electronics
  - Ongoing R&D for the implementation of monolithic CMOS sensors with gain layer for fast timing
  - Custom BSI process allow to develop fully-depleted thick sensors (400μm) for X-ray imaging

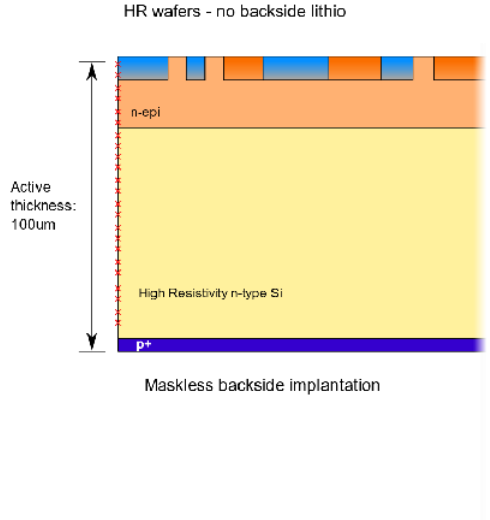
# Sensor Concepts and post-processing

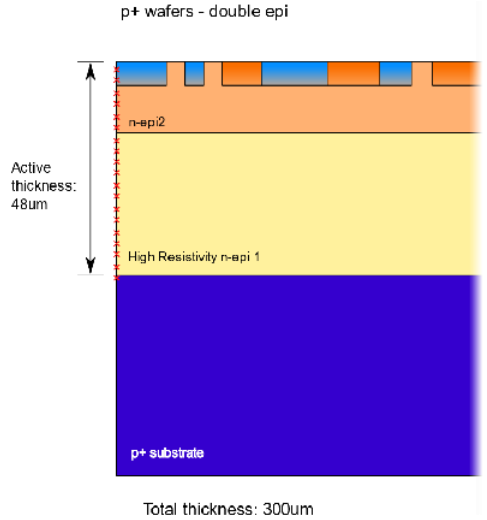



- n-type high resistivity active region + n-epi layer (reduces punch-through current between p+ and deep pwells)
- sensing electrodes can be biased at low voltage (< 1V)
- BSI Reverse-biased junction: depletion grows from back to top
- Ongoing R&D: Fully Depleted PAD sensors with gain layer




Courtesy of L. Panchieri

- thinning, lithography, backside p+ implantation and laser annealing, insulator and metal deposition to create backside guardring structures
- thinning, backside p+ implantation and laser annealing, no patterning on backside
- thinning down to 100μm total thickness on a p+ starting substrate, active thickness below 50μm



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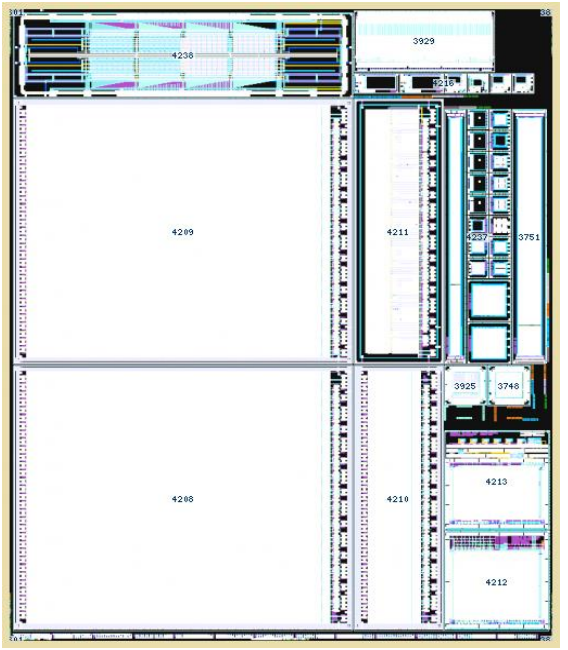
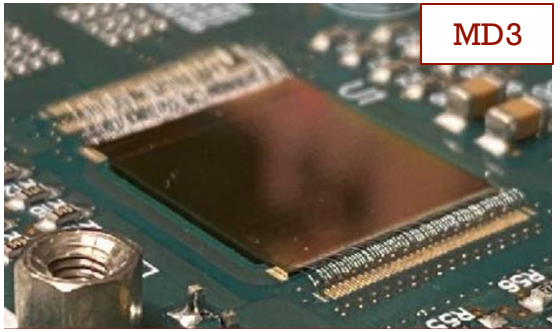
# Different R&Ds in the same platform

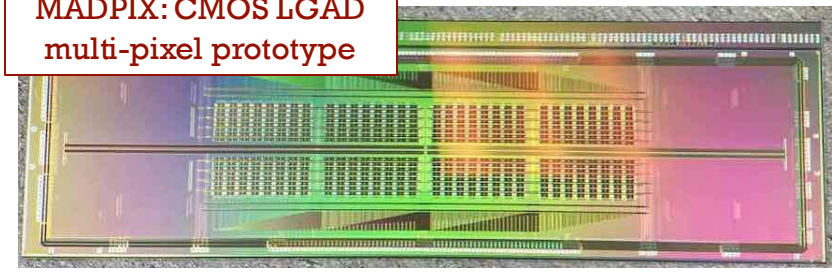
- MD3: Main Pixel Demonstrator
- MAPS and test structures for PSI (CH)
- MATISSE Low Power (ULP front-end for space instruments)
- pixel and strip test structures down to 10μm pitch
- ASTRA 64-channel mixed signal ASIC for Si-Strip readout
- 32-channel monolithic strip and fully-functional readout electronics
- (ER2) HERMES: small-scale demonstrator for fast timing
- (ER3) Small-scale demonstrator of a X-ray multi-photon counter
- (ER3) Wafer splits with timing layer, new R&D towards <<50 ps timing performance: test structures and
- (ER3) MADPIX: multi-pixel active demonstrator chip for fast timing

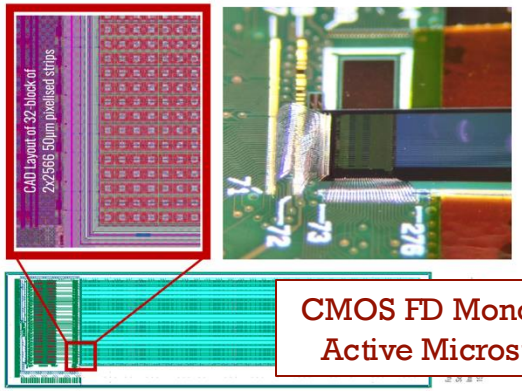


MD3



MADPIX: CMOS LGAD multi-pixel prototype



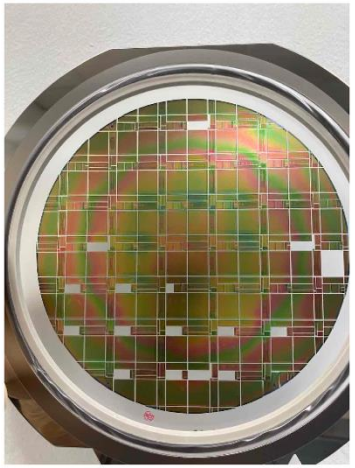



CMOS FD Monolithic Active Microstrips

Nice summary in the M. Rolo's talk @ a recent workshop

# MD3: pixel main demonstrator

- Monolithic active pixel with sensor thickness between 50 µm and 500 µm
- Operation in full depletion with fast charge collection by drift, small collecting electrode for optimal signal-to-noise ratio
- Scalable readout architecture with ultra-low power capability (10 mW/cm2)
- Compatibility with standard CMOS fabrication processes
- Technology LF11, 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk
- Custom patterned backside, patented process developed in collaboration with LFoundry



# MD3: chip floorplan


Top Padframe
Auxiliary supply, IR Drop Measure

Matrix
512x512 pixels, Double Column arrangement
Pixel size 25 x 25 $\mu m^2$

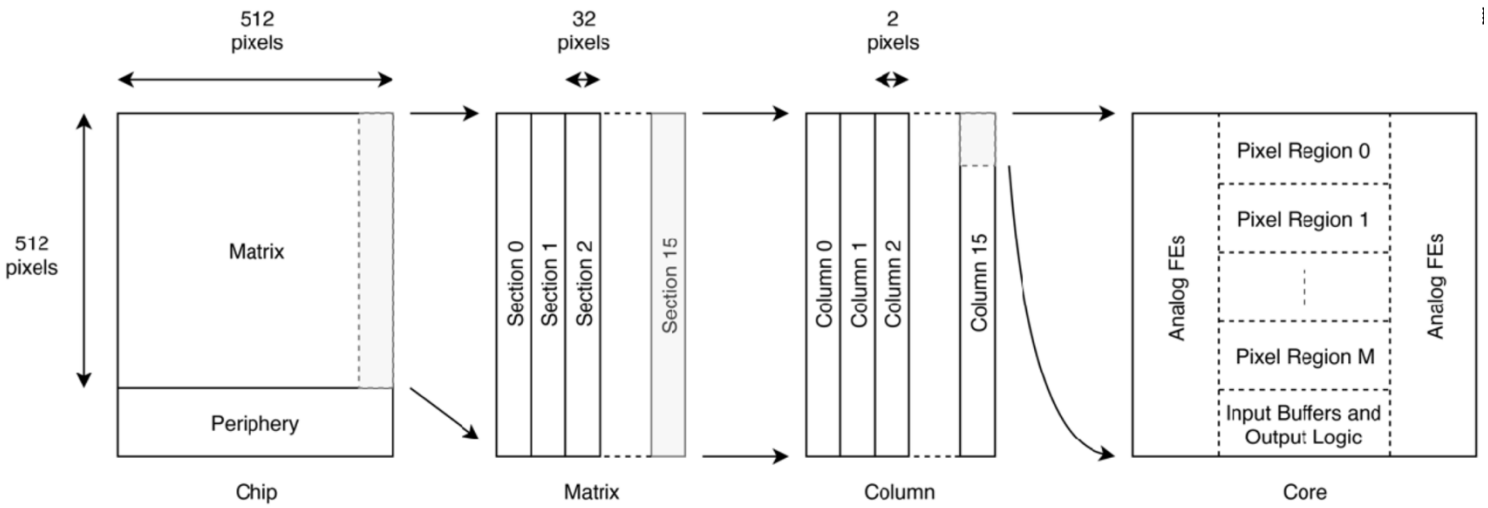
End of Sector (x16)
Reads and Configures 512x32 pixels

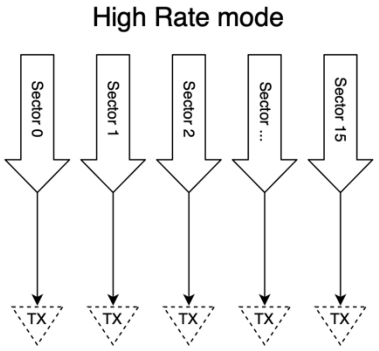
Sector Biasing (x16)
Generates I/V biases for 512x32 pixels

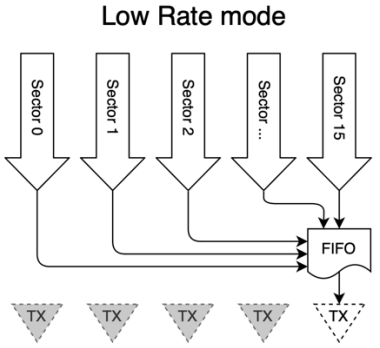
Periphery
SPI, Configuration, 8b10b enc, Serializers

Bottom Padframe
Stacked Power and Signal pads

# MD3: chip architecture

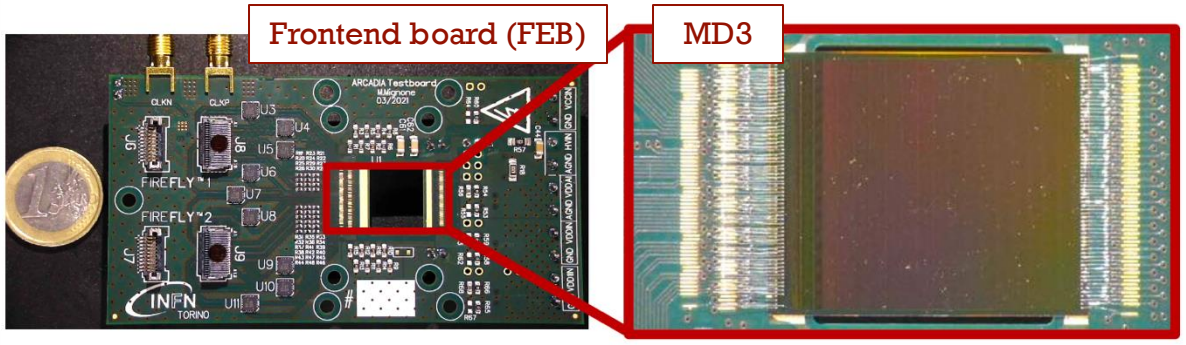


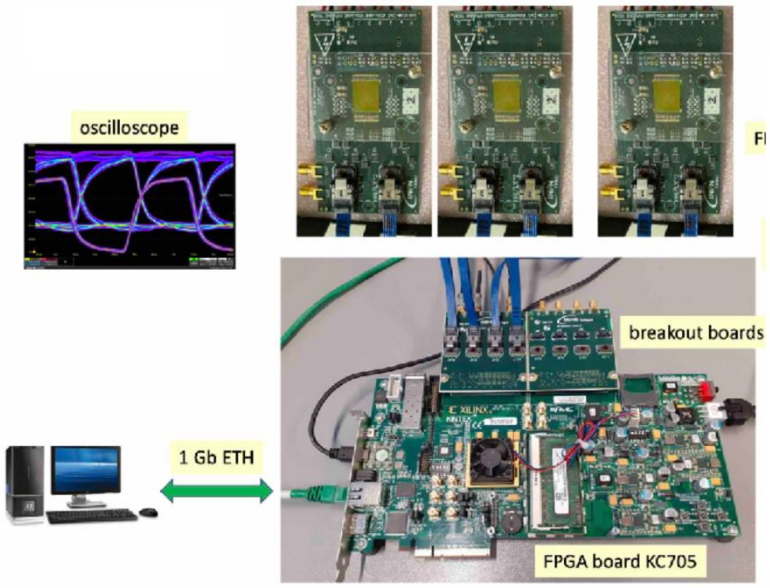




- Pixel size 25 μm x 25 μm, Matrix core 512 x 512, 1.28 x 1.28 $cm^2$ silicon active area, "side-abuttable"
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to 100 MHz/cm2 (from design and post-layout simulations: to be demonstrated)
- High-rate operation (16 Tx): 17-30 $mW/cm^2$ depending on transceiver driving strength (measured)
- Low-power operation (1 Tx): 10 $mW/cm^2$ (measured)

# Front-end board and DAQ





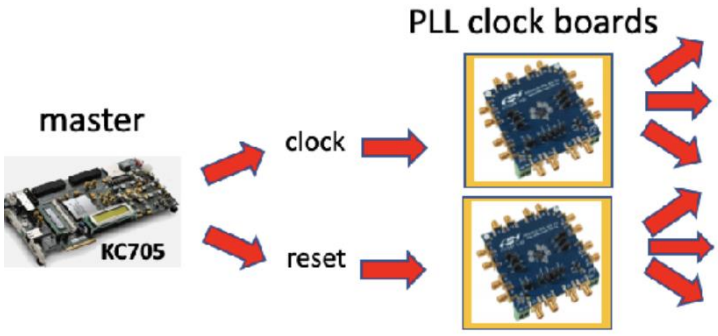



- Each FEB is equipped with 1 MD3
  - Connection to external low jitter Clock (via SMA connectors)
- 2 Samtec FireFly connectors for one MD3 (clock, SPI, data, testpulse, reset)
- One FPGA board (KC705) serves up to 3 FEBs (mini-telescope)
- Breakout board to convert FMC to Samtec Firefly connectors
- 1Gb ETH protocol for data transmission

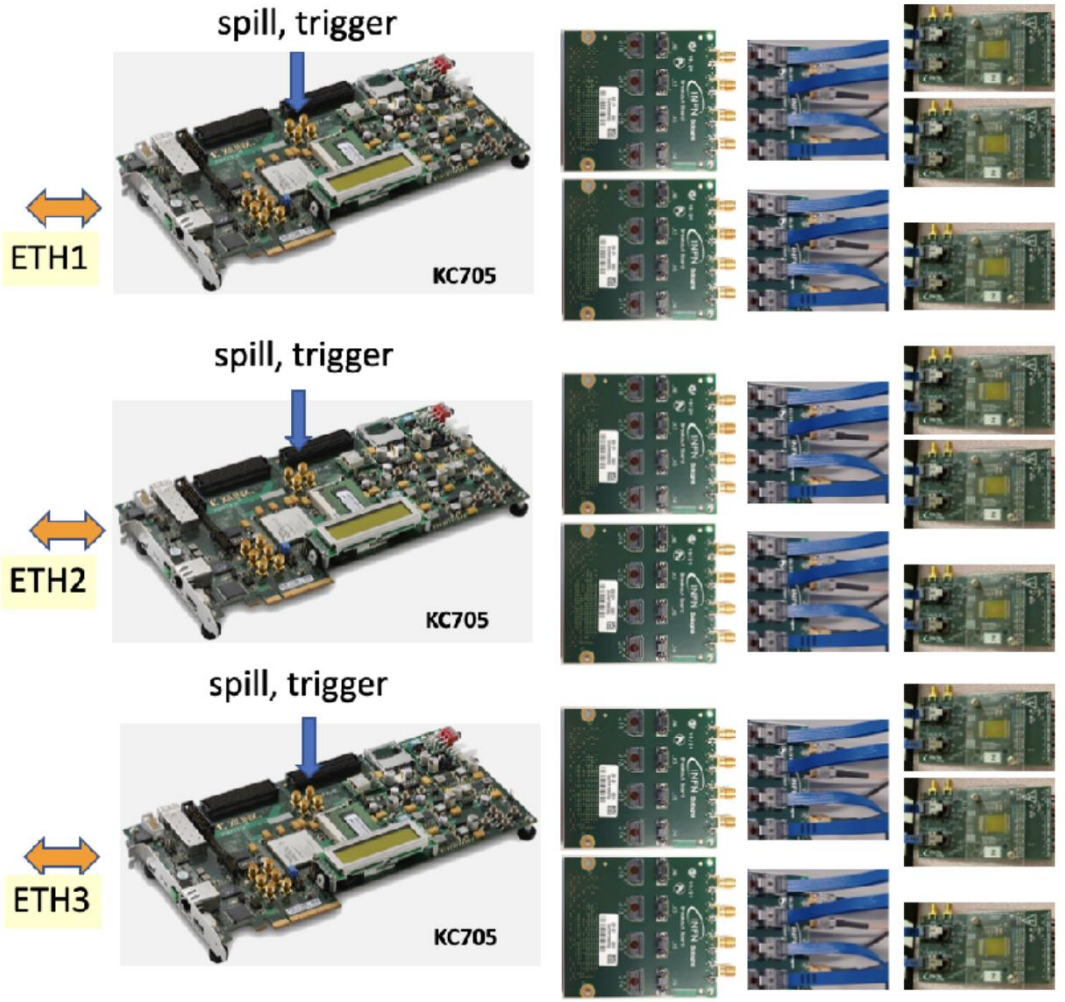
# DAQ hardware

Scalability with current hardware:
reasonable for beam test studies

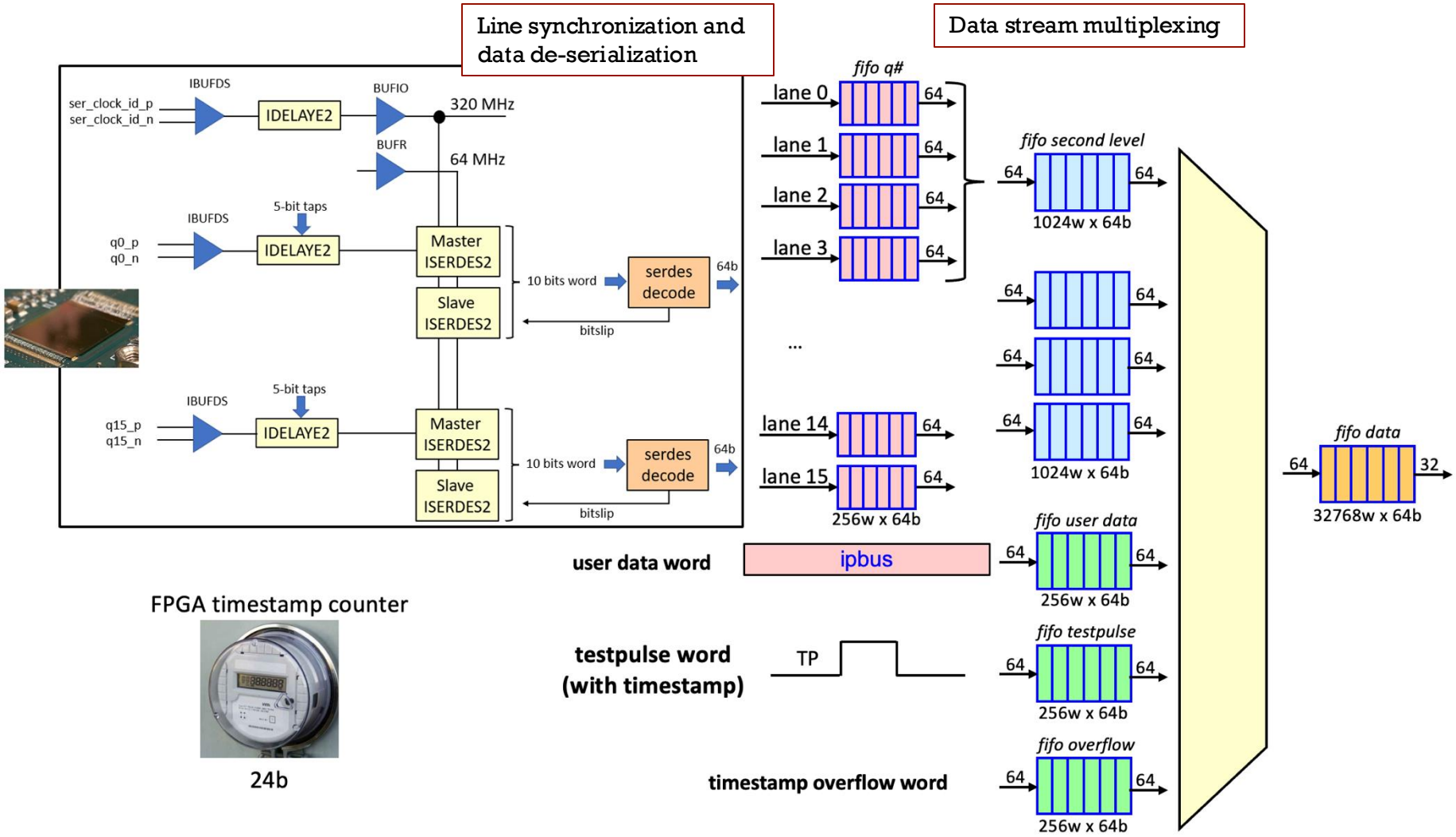
Scheme qualified on beam
in EPIC dRICH





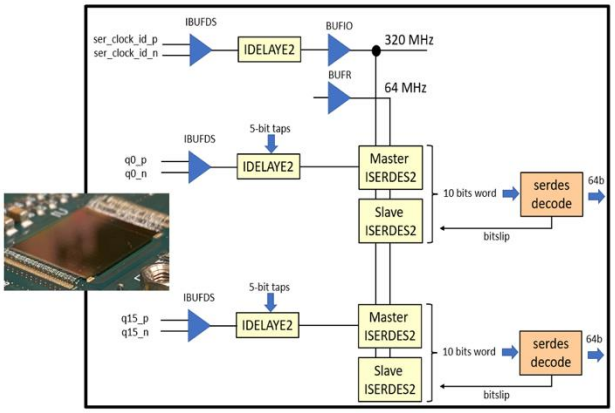


# DAQ firmware: data push architecture

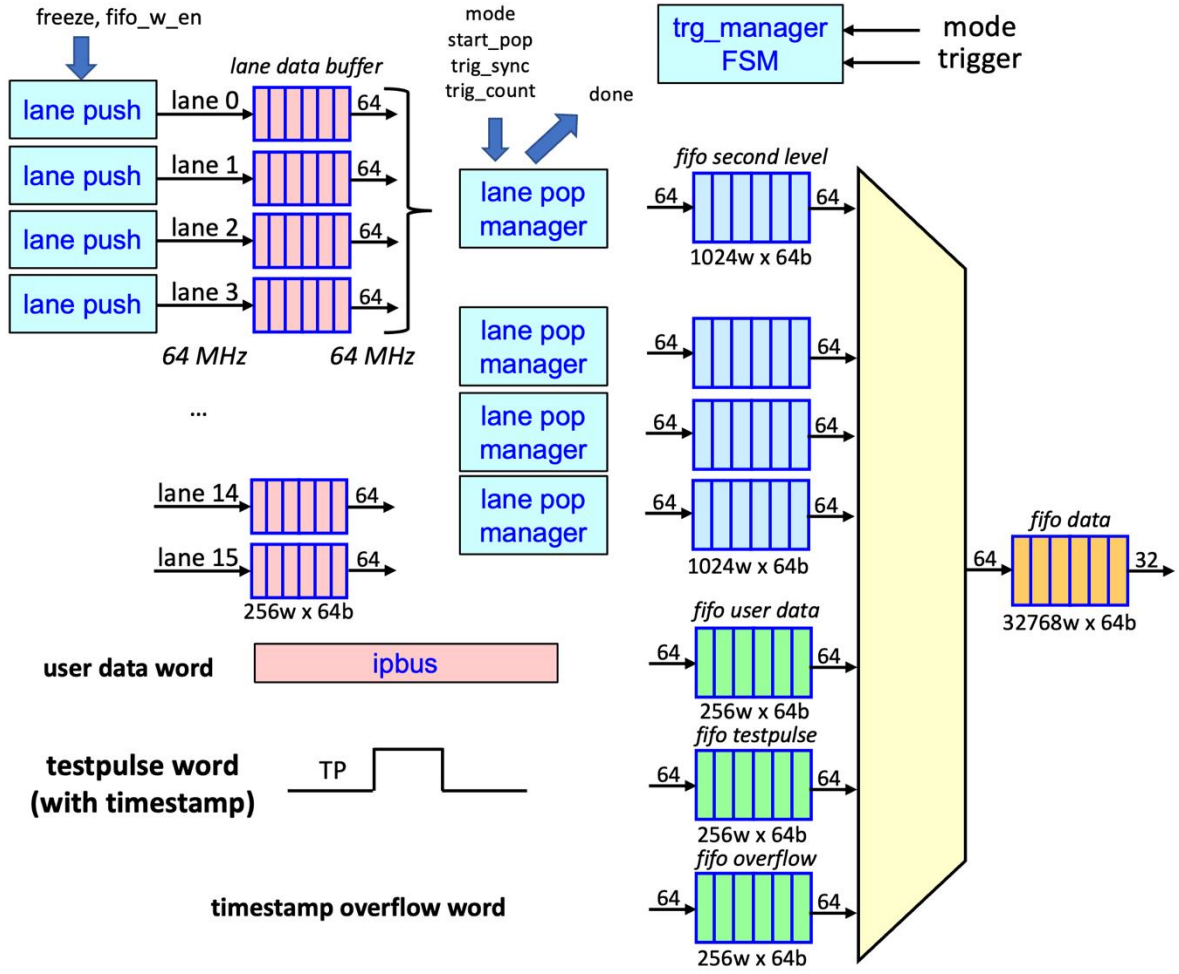


# DAQ firmware: triggered architecture

Line synchronization and data de-serialization





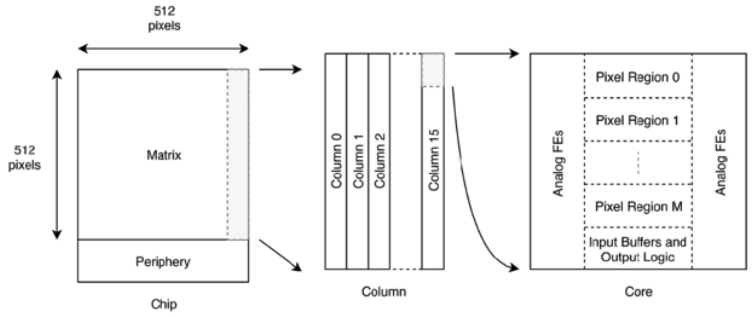

FPGA timestamp counter

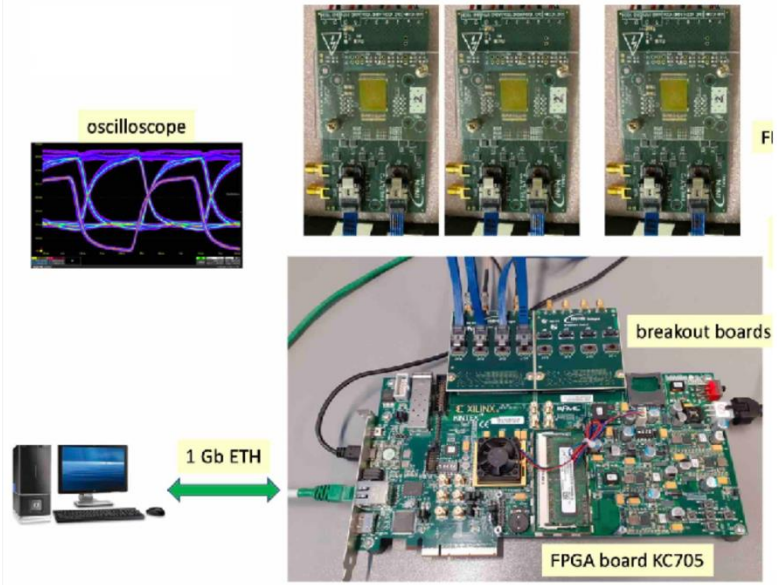
24b

# MD3: readout rate

**ARCADIA Target: 100MHz/cm2**

- Chip readout rate in details:
  - 16 serial links operated in parallel: 640 Mbit/s (nominal speed): used @ 200 Mbit/s (sync stability)
  - 1 pixel requires 32 bit (coordinates + time stamp)
    - If more pixels share the same core they are readout in the same 32bit data stream
  - Chip data flow = 100 M hits/s*
- Present DAQ serves up to 3 MD3 with a maximum data flow of 1Gbit/s
  - Measured 10 MHz/chip: bottleneck set by the communication protocol
- 3 MD3 at full speed requires 10Gbit/s
  - Optical link (10Gbit) would allow to reach the target performance




**Additional information:**

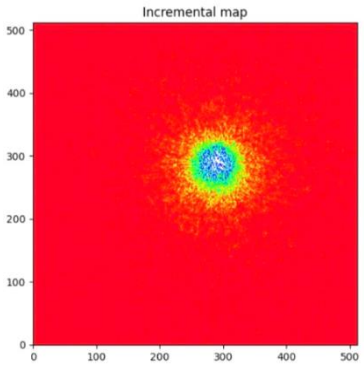
- Time tag resolution = 200 ns (5MHz clock cycle)
- Power consumption in high rate mode < 30 mW/cm$^2$ (measured)

*Chip data Flow = (200 Mbit/s*16 Lines) /32 bit ≈ 100 M hits/s

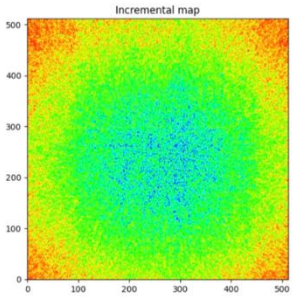
# First tests with particles

$^{90}Sr$

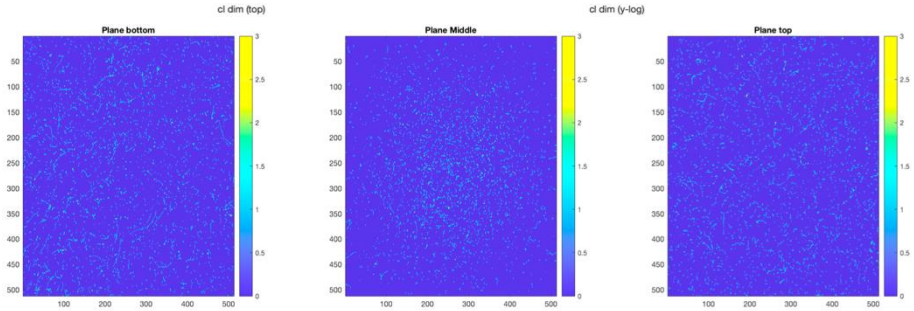
(collimated 1mm)

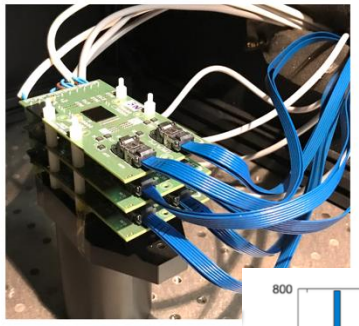



(uncollimated)

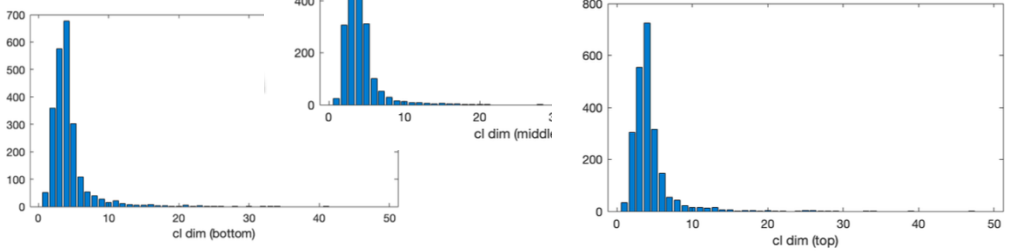



Cosmic run



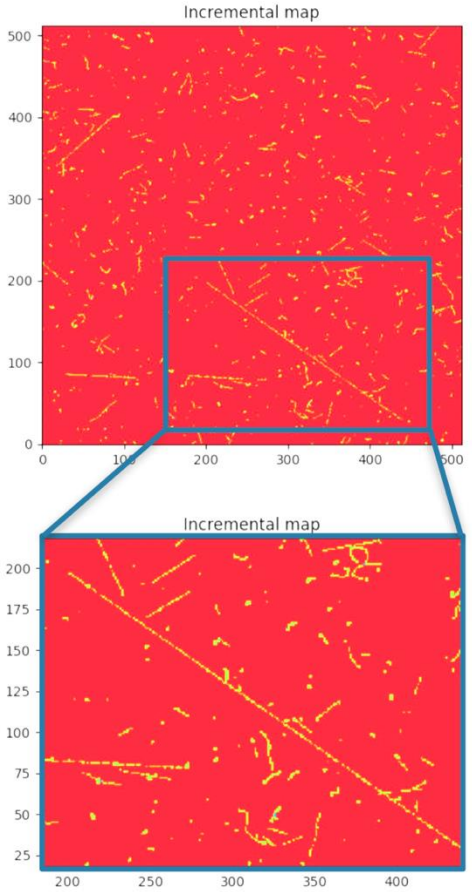



- Threshold ≈ 290 e-, MPV = 4 pixels
- More than 90% of clusters with less than 6 fired pixels



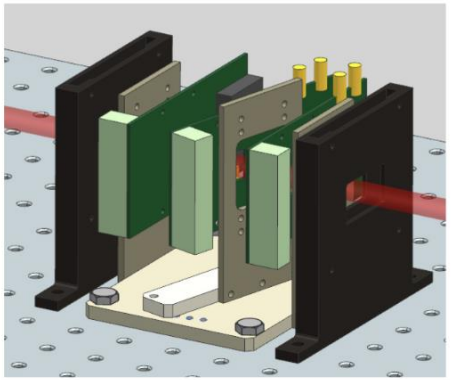

**Cosmic rays**

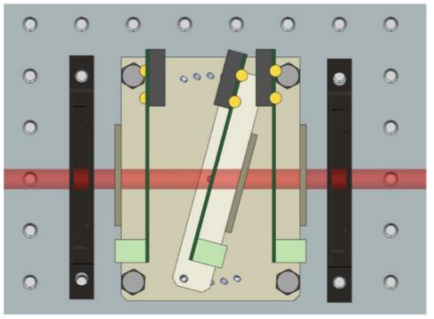
(tilted sensor)

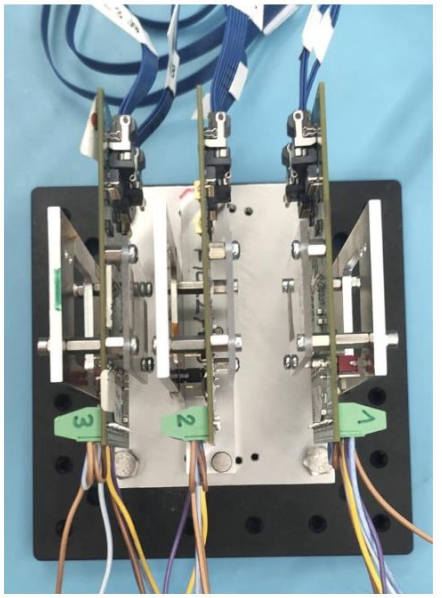


# Test beam at FNAL

- Mini-telescope with 3 MD3, 200 μm thick sensors
- 120 GeV proton beam
- Performance studies as a function of sensor HV, thresholds and tracks angle
- Parameters under study: cluster size, collection efficiency and spatial resolution
- All results are preliminary: analysis still on-going







***The INFN-PD Test-beam Team:***

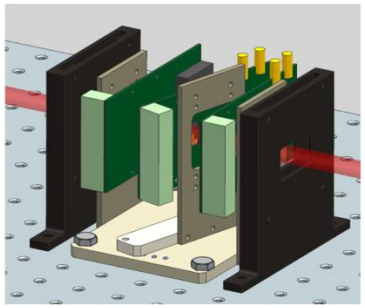
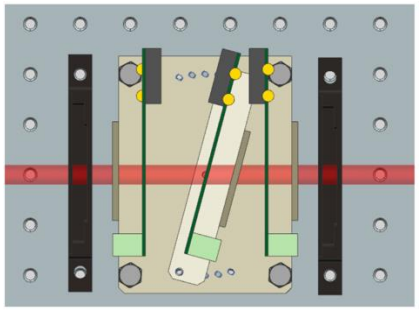
*Sabrina Ciarlantini, Caterina Pantouvakis, Michele Rignanese, Alessandra Zingaretti, Piero Giubilato, Jeffery Wyss, Serena Mattiazzo, Chiara Bonini, Davide Chiappara, Devis Pantano, Patrizia Azzi e Rosario Turrisi*

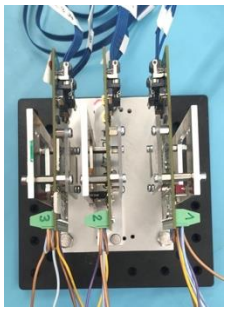
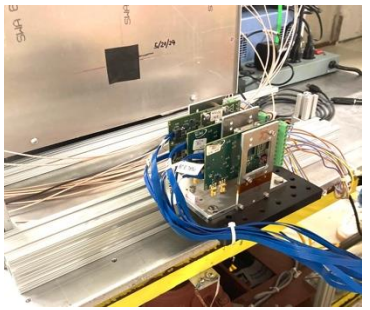
***At FNAL:***

*Irene Zoi, Nicola Bacchetta, Artur Apresyan, Aram Hayrapetyan, Pierce Affleck*

# Data analysis strategy

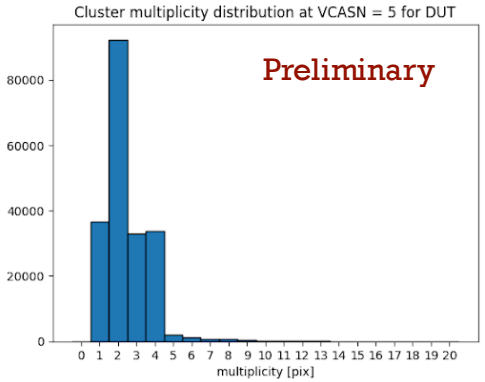
- Clusters definition: adjacent pixels (no "holes") close in time (time window)
- Tracking performance measured selecting clean events: one cluster per plane
- Alignment procedure:
  - One of the external planes used as reference
  - Preliminary alignments based on cluster correlation plots
  - Central plane aligned using residual distributions (tracks – cluster position)
  - Tilt correction using y-residual VS x-coord and viceversa (x-residual VS y-coord )
  - Final alignment performed after tilt correction with residual distributions
- Efficiency measured in a fiducial region of 275 $\mu m$ correlated to the extrapolated track

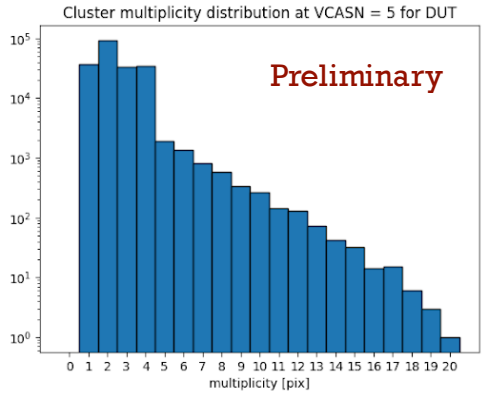



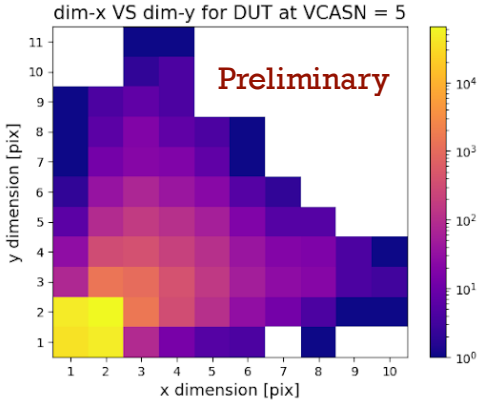



# Data analysis: cluster size

DUT cluster size analysis @VCASN = 5 (~ 600 e-)



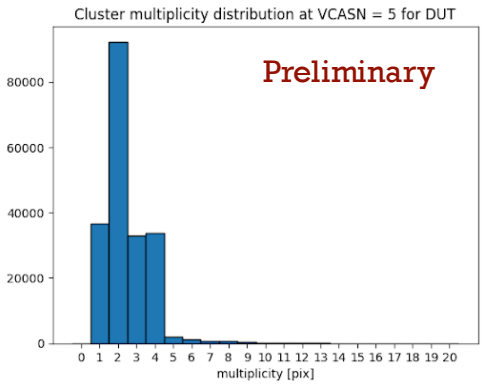



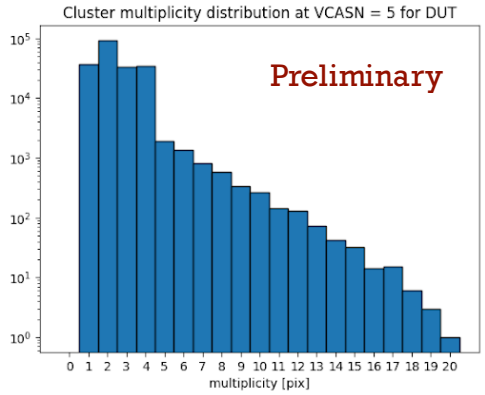



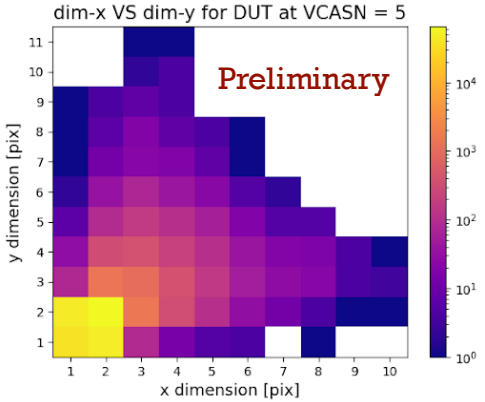

≈96% of clusters within a 2x2 pixel box

# Data analysis: cluster size

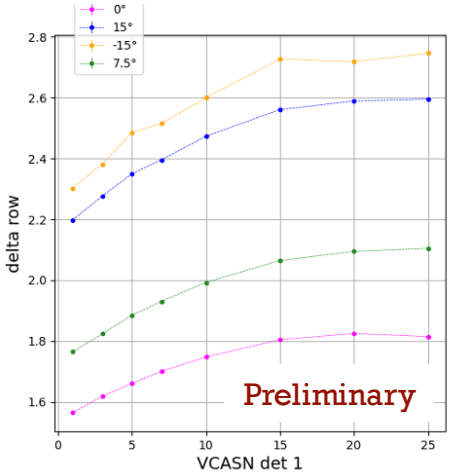
DUT cluster size analysis @VCASN = 5 (~ 600 e-)

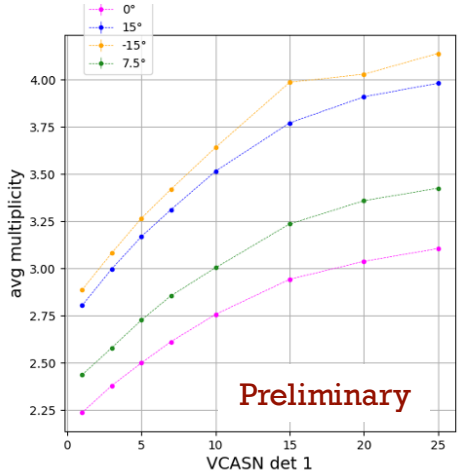



≈96% of clusters within a 2x2 pixel box

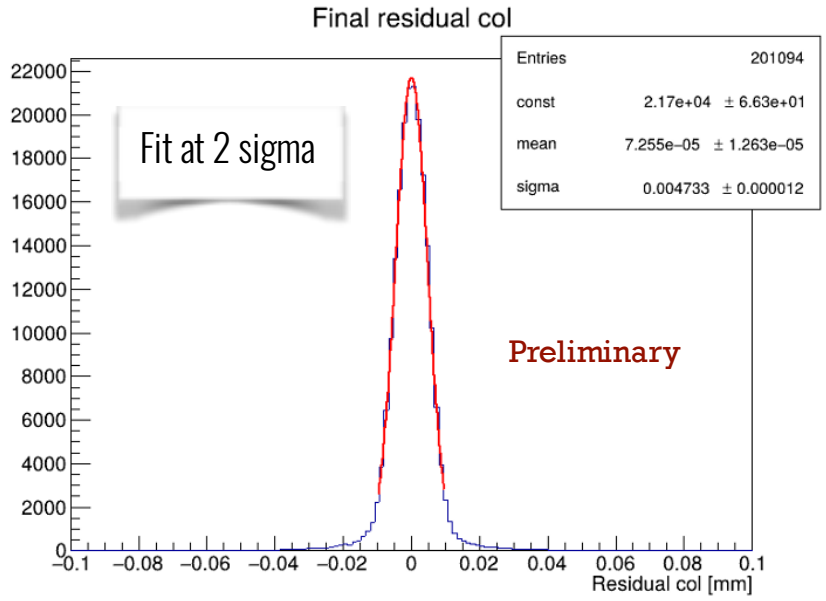


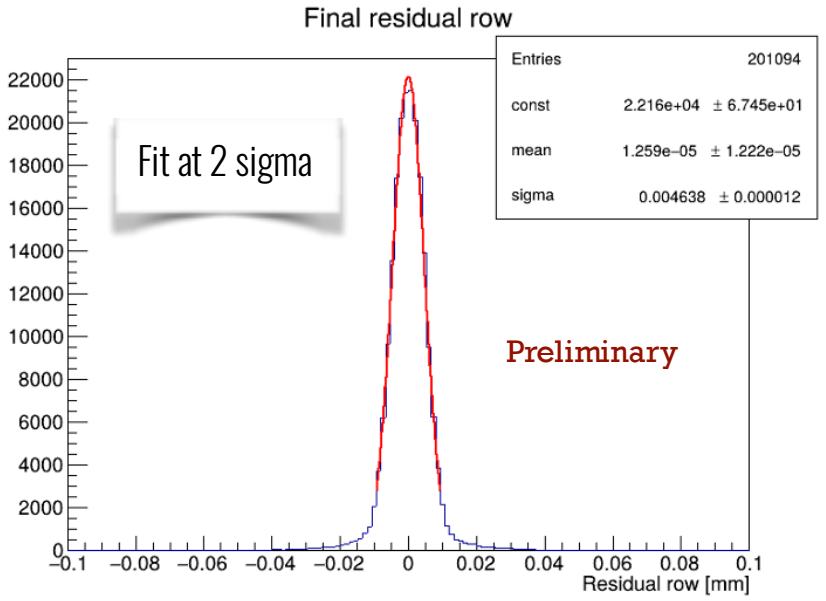




Cluster size (DUT) as a function of discriminator thresholds and incidence track angle

# Data analysis: spatial resolution

- Residuals plots @VCASN = 5 (~ 600 e-): contributions from tracking still included
- angle of tilt = 0°

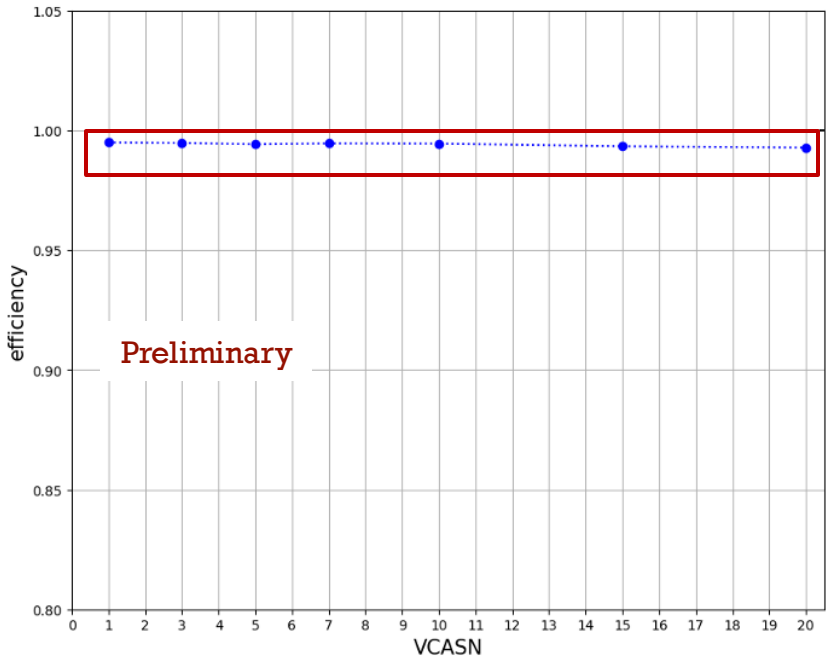


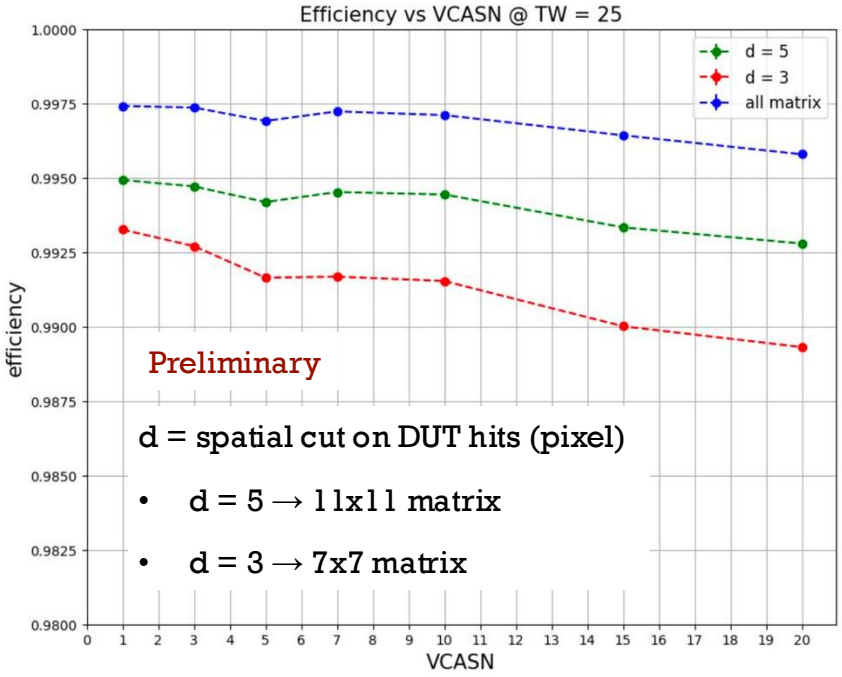

Residuals better than 4.7 $\mu m$

# Data analysis: efficiency

Efficiency plot VS Threshold (from 800e- down to 300 e-)




zoom




Average efficiency of 99.41 ± 0.01 %

Spatial cut = 5 pixels

# Summary of MD3 performance

- Active area of 1.28 x 1.28 $cm^2$
  - 200$\mu m$ thick sensor qualified on beam
  - 50$\mu m$ thick sensor available: to be qualified on beam soon
- Readout rate of 100MHz/$cm^2$ achievable with power consumption < 30 mW/$cm^2$
- Preliminary result from test beam
  - Single point spatial resolution better than 4$\mu m$
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- The MD3's low thickness and low power are important points to get low material budget in front of the tracks
- The small chip area requires the use of overlap regions, which must be carefully quantified