IMPERIAL

Progress with the 1S-module

Introduction & Status

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Progress with 1S-module

Aims of Project

Produce a design for tracking stages that are suitable for:

- Beam Telescopes
- Fixed Target experiments
- R&D activities

To leverage/piggyback on new technologies and designs developed for the CMS upgrade:

- Silicon Sensors
- ASICs
- Backend hardware (Serenity)

To use as much as possible COTS hardware to:

- Avoid exotic technologies such as HDI flex PCBs
- Reduce cost
- Simplify system support requirements
- Make design iterable at 'normal' costs...

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A Quick look at the CERN 2S module

Double sensor arrangement for resolving bends

- Little benefit in many applications
- Introduces additional material into beam path

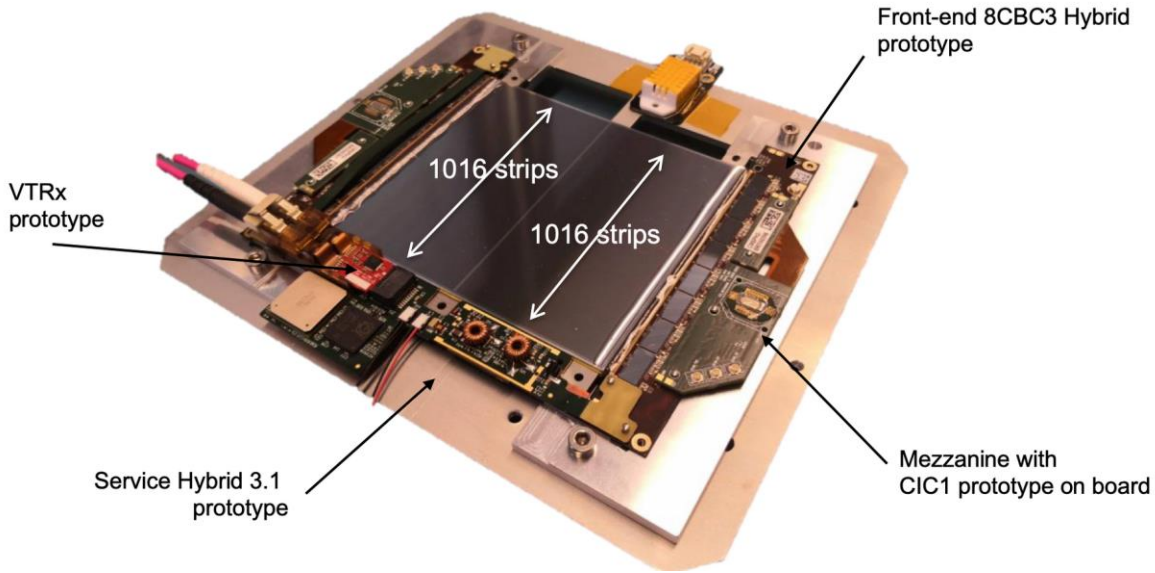
Front-end & Service Hybrid Board

- High B Field, High radiation tolerance design
- Custom devices:
  - CBC3 & CIC
  - LPGBT & VTRx
  - Power Hybrids

All needed to work in CMS constraints, but come with many overheads.

2S Devices are scarce

- Availability will be a consequence of module surplus



https://cds.cern.ch/record/2703569/plots

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Introducing the 1S module

Our design consists of

A single CMS Silicon strip sensor:

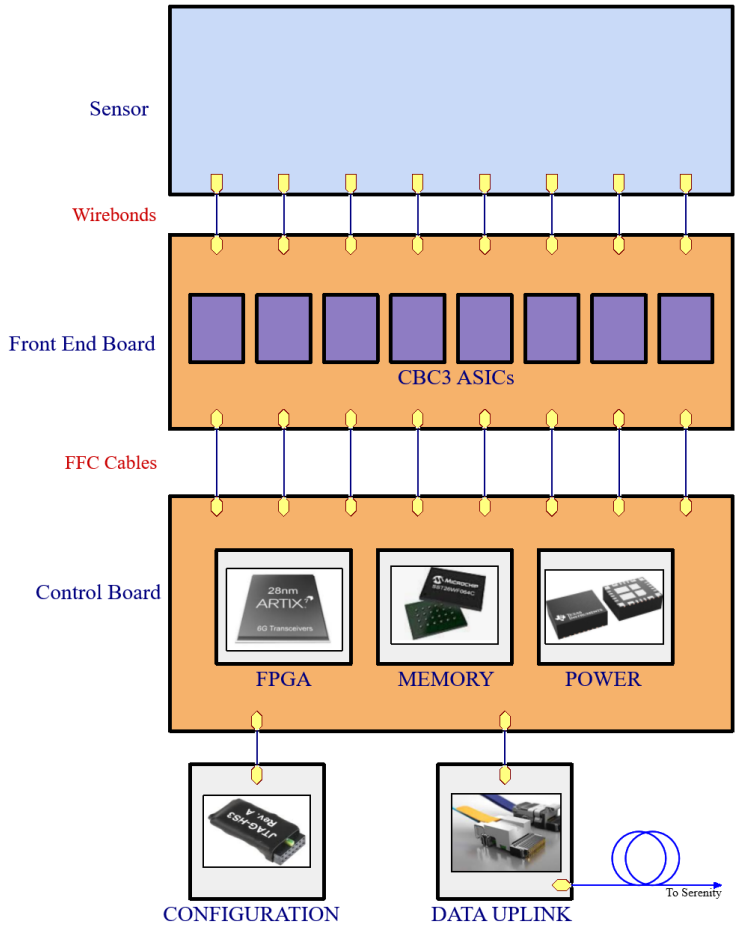
- 1016 channels @ 90 um

2 Front end boards:

- 8 x CBC ASICs
- ~1k wire bond pads to sensor
- Sensor bias filtering and distribution
- Connectors to control board

Control board:

- FPGA
- Power conversion
- Bias control
- Fibre interface to DAQ



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Front End Board

Features:

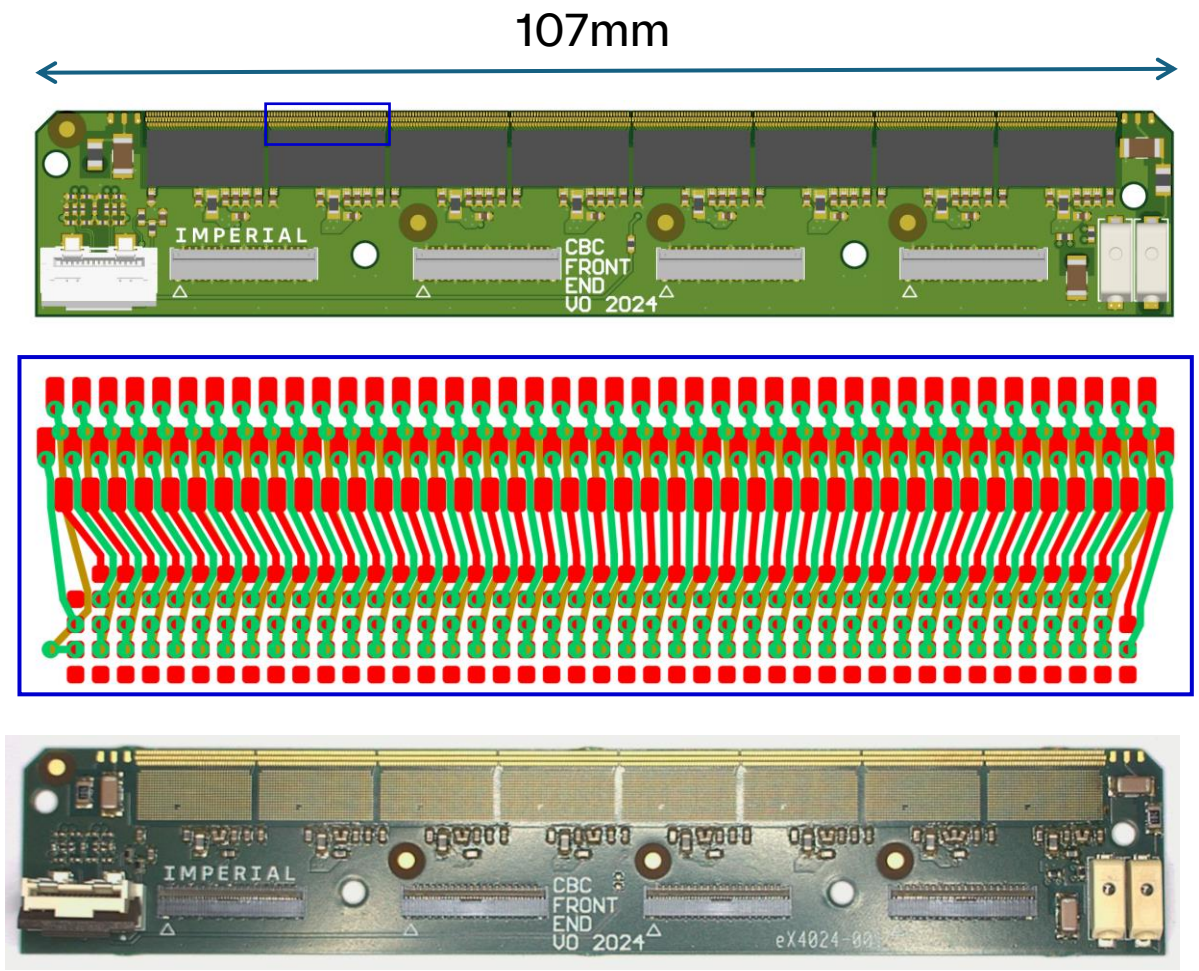
- ~1000 Wire bond pads for sensor connections
- Sites for 8 CBC3 ASICs
- Connectors for data, clock, power
- Bias distribution

Strategy here is maximum simplicity:

- Complexity (and design risk) is offloaded to other board
- This also means we have smaller and cheaper PCB

Board Specs:

- 8 Layer HDI
- 80um track and gap
- 160um uVias
- Total via count = 12K or 5.8/mm^2!
- Cost per bare board is 340 EUR or 17¢/mm^2



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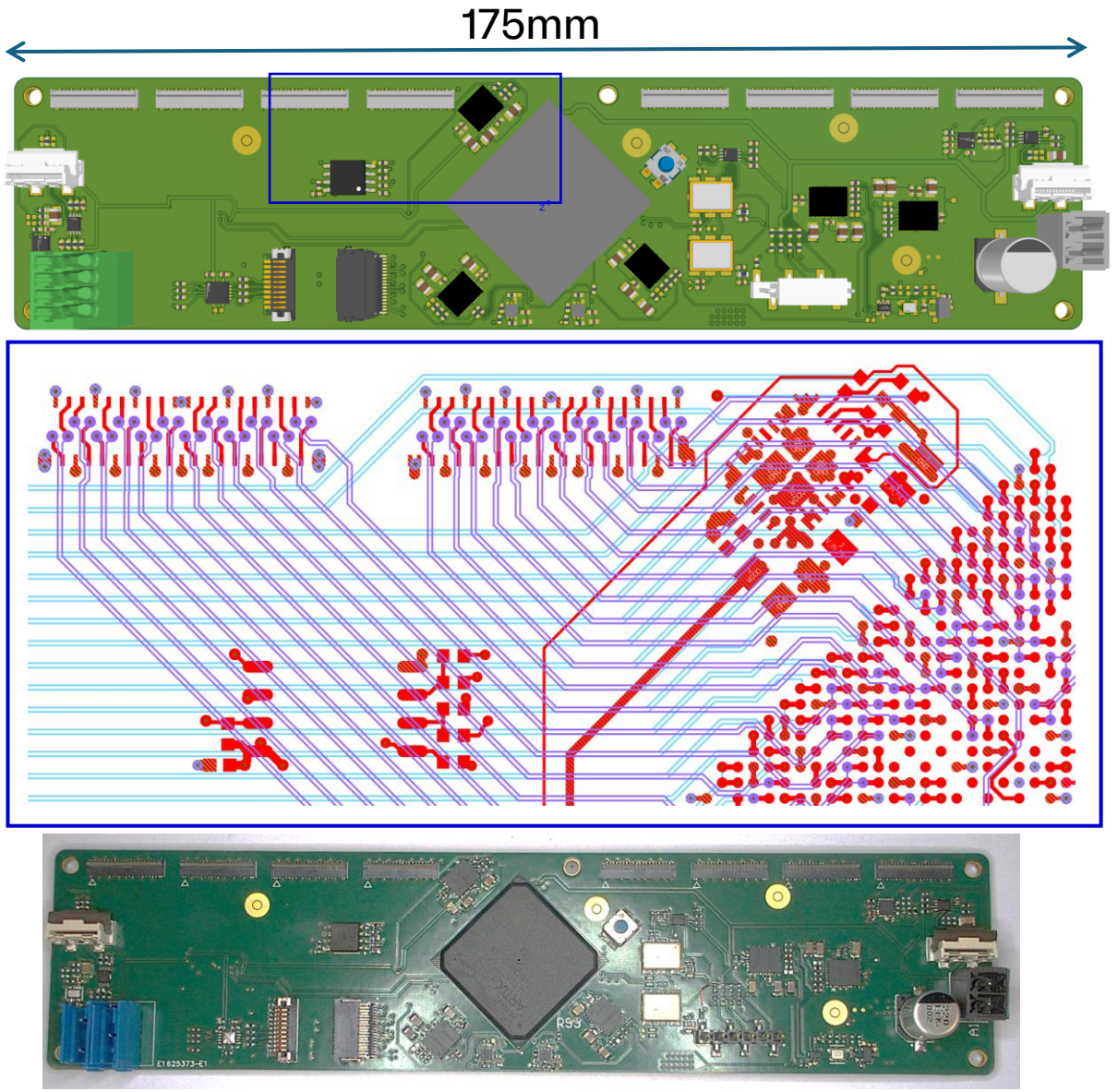
Control Board

Features:

- AMD Artix XC7A100T FPGA (484 balls)
- Connections to 2 Frontend boards:
  - 16 CBC3 ASICs
  - 96 links at 320Mb/s = total 30Gb/s
- 4 channel Firefly transceiver site: 25Gb/s to Serenity
- On board HV bias regulator

Board Specs:

- 8 Layer standard tech
- 125 um track/gap
- Via count 1,300
- Cost per board 80 EUR or 1.4 ¢/mm^2 (more than 10x cheaper than front end boards!)



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Mechanical Support

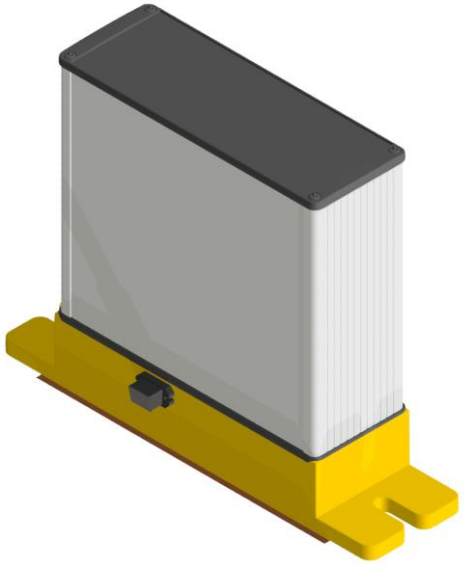
loosely defined as we lack the time resources.

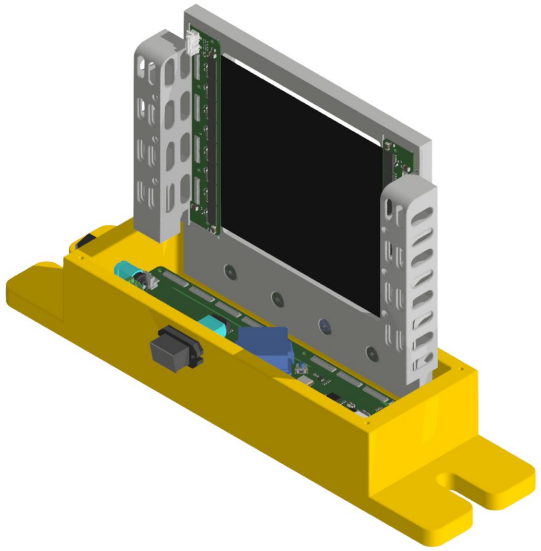
Consequently, working towards a functional electronics demonstration.

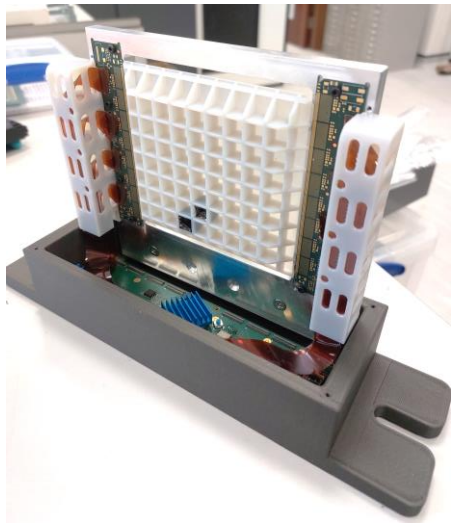
- Acceptable that future mechanical constraints require electronics revision

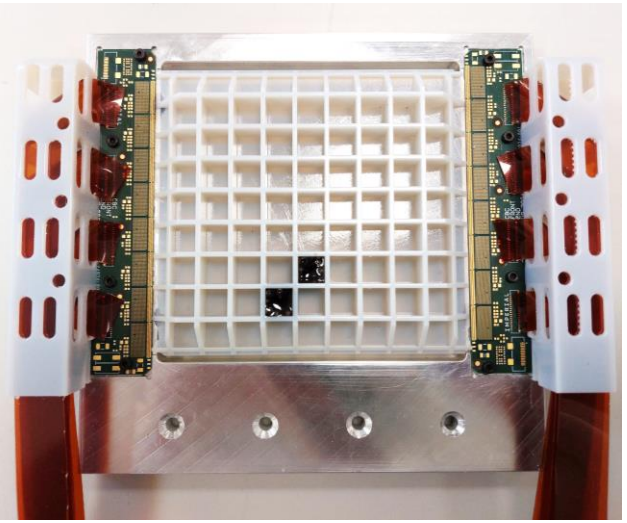
A simple mechanical support system does exist:

- Suitable to demo electronics in a test beam
- Mix of 3d printed and machined alu plate
- Little consideration to:
  - Thermal management
  - Dimensional Stability
  - Alignment









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Device Assembly

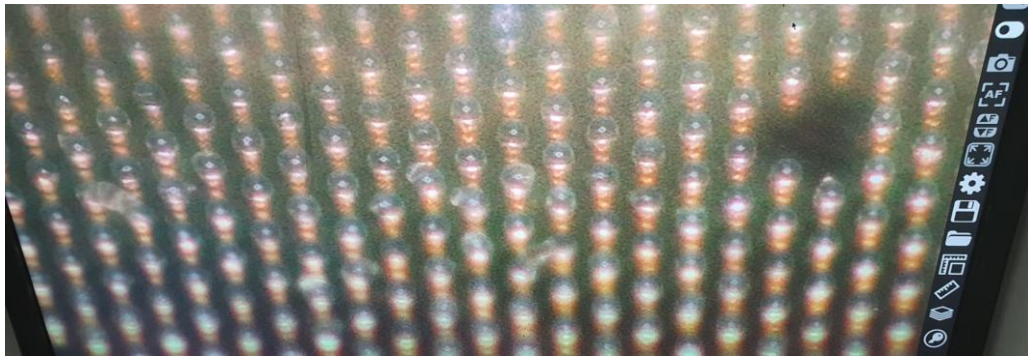
Assembly facilities at IC

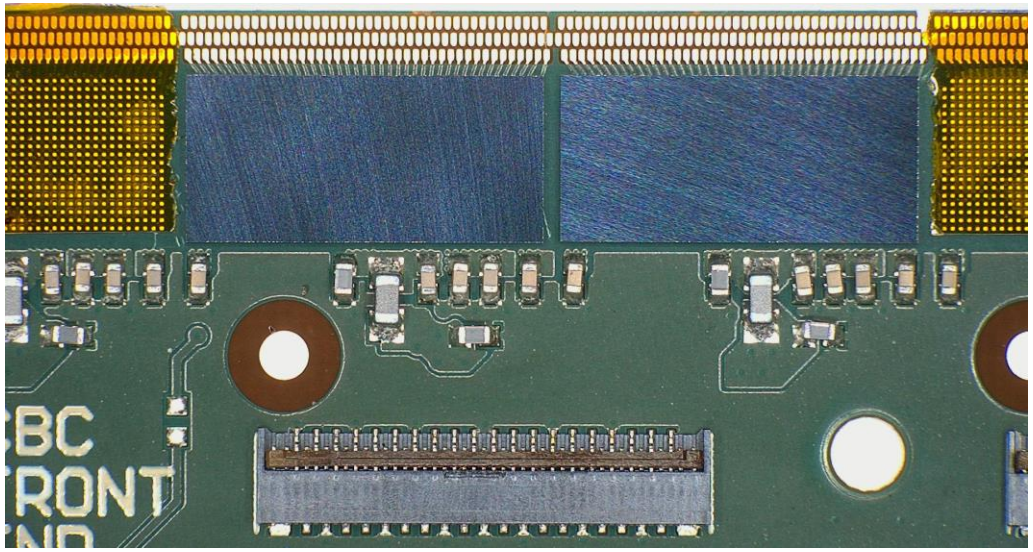
- Automated pick and place
- Reflow machines
- Rework/Precision placement machines.
- Manual wire bonder

New processes to learn – assembly of CBC3 ASICs a 250um pitch bump bonded flip chip:

- Chip dipping technique to deposit ~50um film of flux on each solder ball.
- Tuning flux viscosity
- Precision alignment

Objective: to achieve sufficient yield to assemble one or two complete modules.





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Current Status

We have 5x assembled Control boards

Done:

- All passed smoke tests
- 4 with all power rails functional
- 4 with FPGA visible and programmable
- 4 with some transceiver links functional

To do:

- Develop firmware
- Interface with front end board
- Interface with Serenity
- Read test pulses

We have 5x assembled Front End Boards

(mostly Minus ASICs)

Done:

- One board has 2 ASICs assembled and has passed smoke tests. (significant!)

To Do:

- Fully populate 8 ASICs on 4 boards
- Interface to Control Board
- Attach Sensor to mechanical support
- Wire bonds made to sensor

Many of these tasks need firmware and hardware support!

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Collaboration

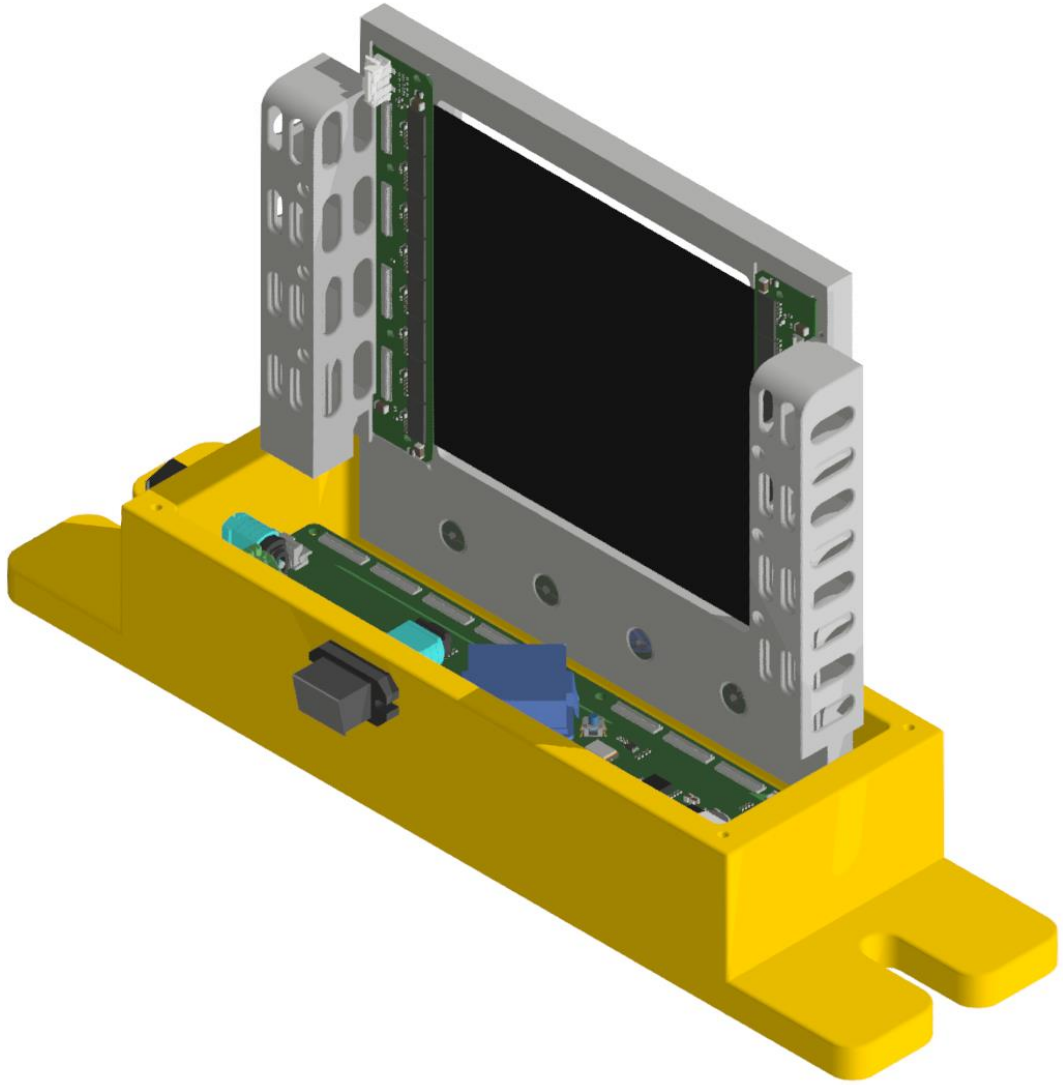
We are seeking collaboration!

We looking for partners with skills/facilities:

- Cleanroom module assembly
- Bump bond flip chip assembly hardware and expertise
- Large scale Wire Bonding
- Mechanical design expertise
- Module level testing

Finally, the system is modular. With limited effort we can revise for different:

- Sensors
- ASICs
- Backend hardware



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