RD50-MPW4 evaluation and joint Mighty Tracker & UT design

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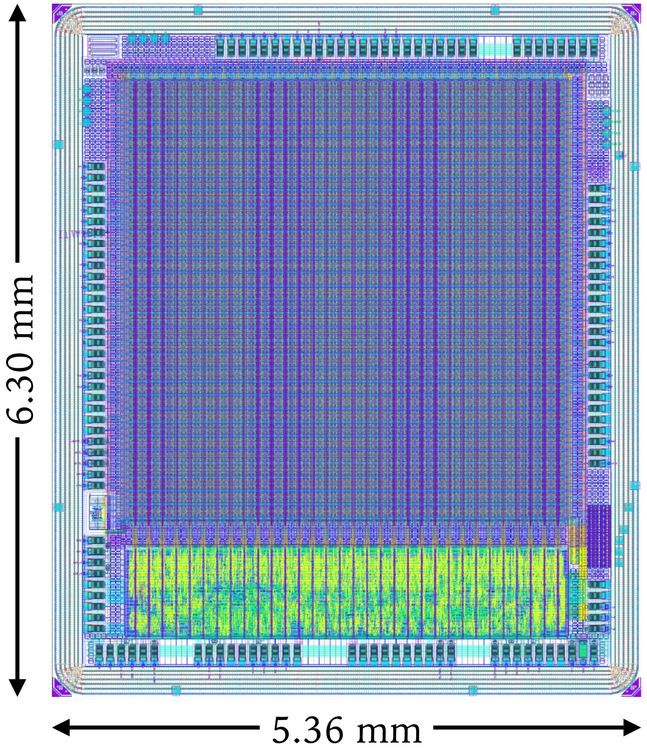
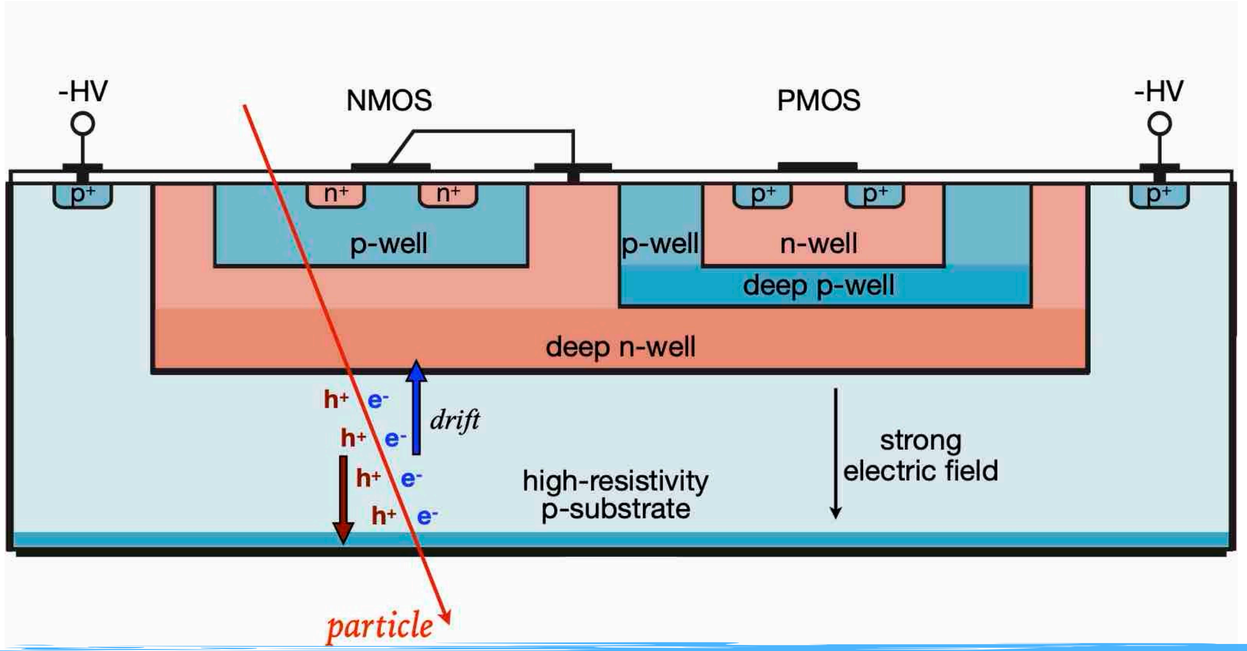
4th Mighty Tracker Workshop
Liverpool, 2-4 July 2024

Sensor cross-section

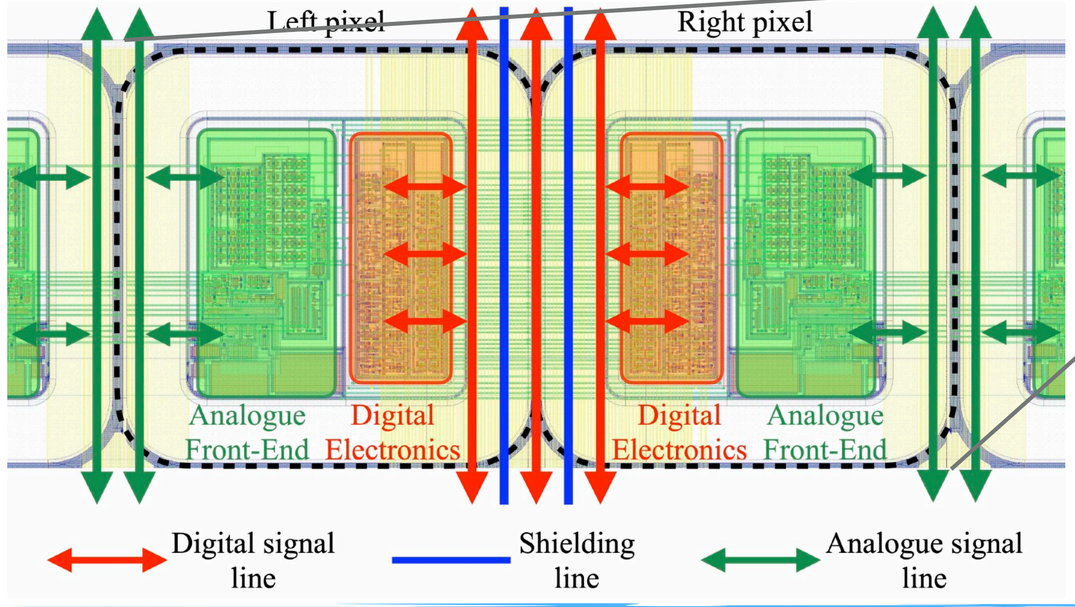
- RD50-MPW4 was developed by the RD50 CMOS working group.
- Large charge collection electrode.
- Fabricated on 3 kΩ·cm wafers and thinned to 280 μm, using 150 nm HV-CMOS process from LFoundry.
- 1 wafer with topside biasing only, 2 wafers were back-side processed for higher breakdown voltage and hence higher radiation tolerance.
- High voltages to the top side or back side with backside processing.

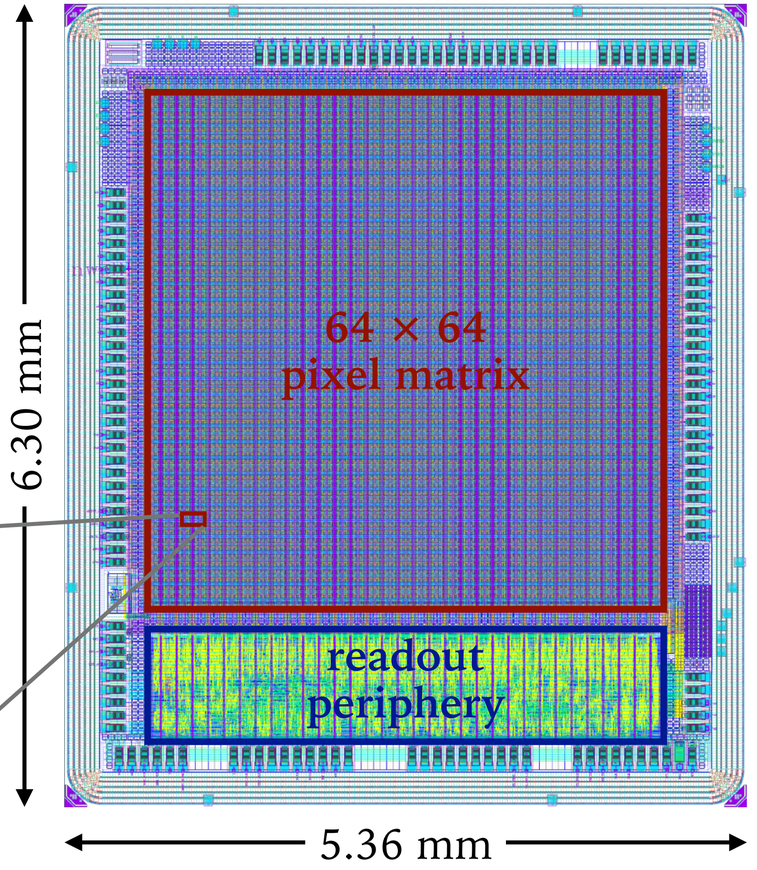




Design of RD50-MPW4

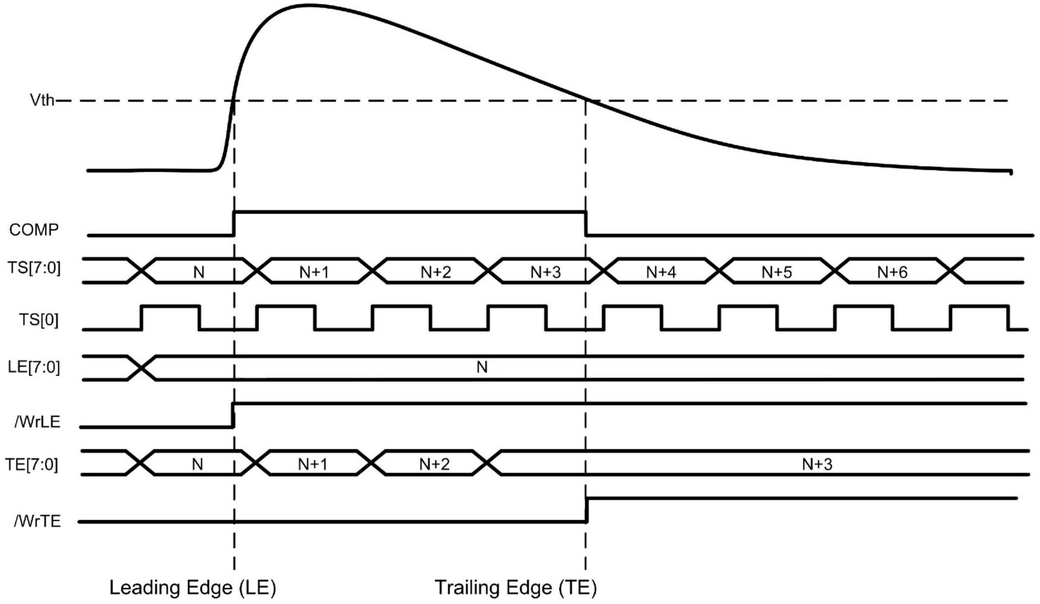
- RD50-MPW4 is mainly composed of a 64 × 64 pixel matrix and a digital readout periphery.
  - pixel matrix has a double-column architecture with FE-I3 style readout (trigger-less);
  - digital periphery implements I2C protocol for slow control configuration and a 640 Mb/s LVDS serial link for hit data transmission.
- Each pixel (62 μm × 62 μm) has analog and digital readout electronics.

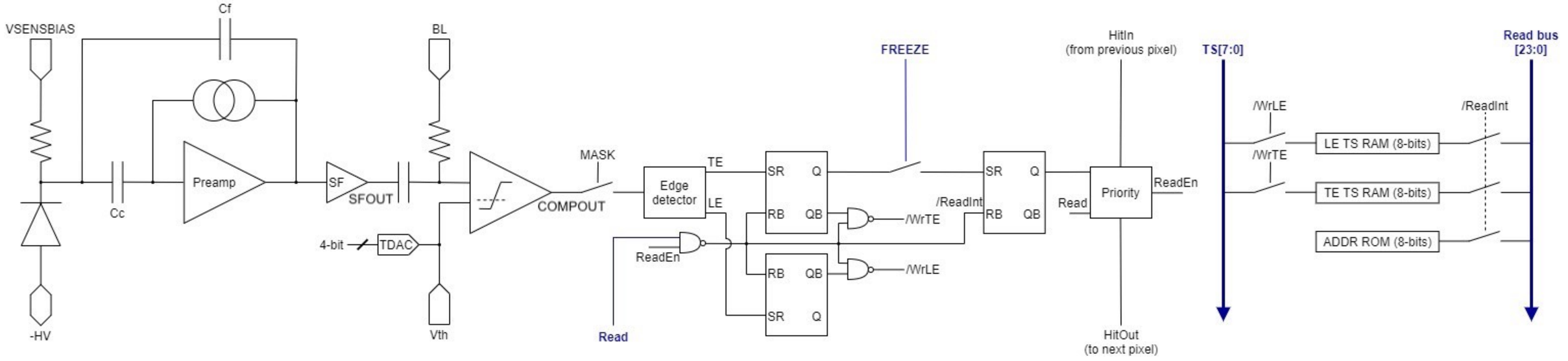




In-pixel readout circuits

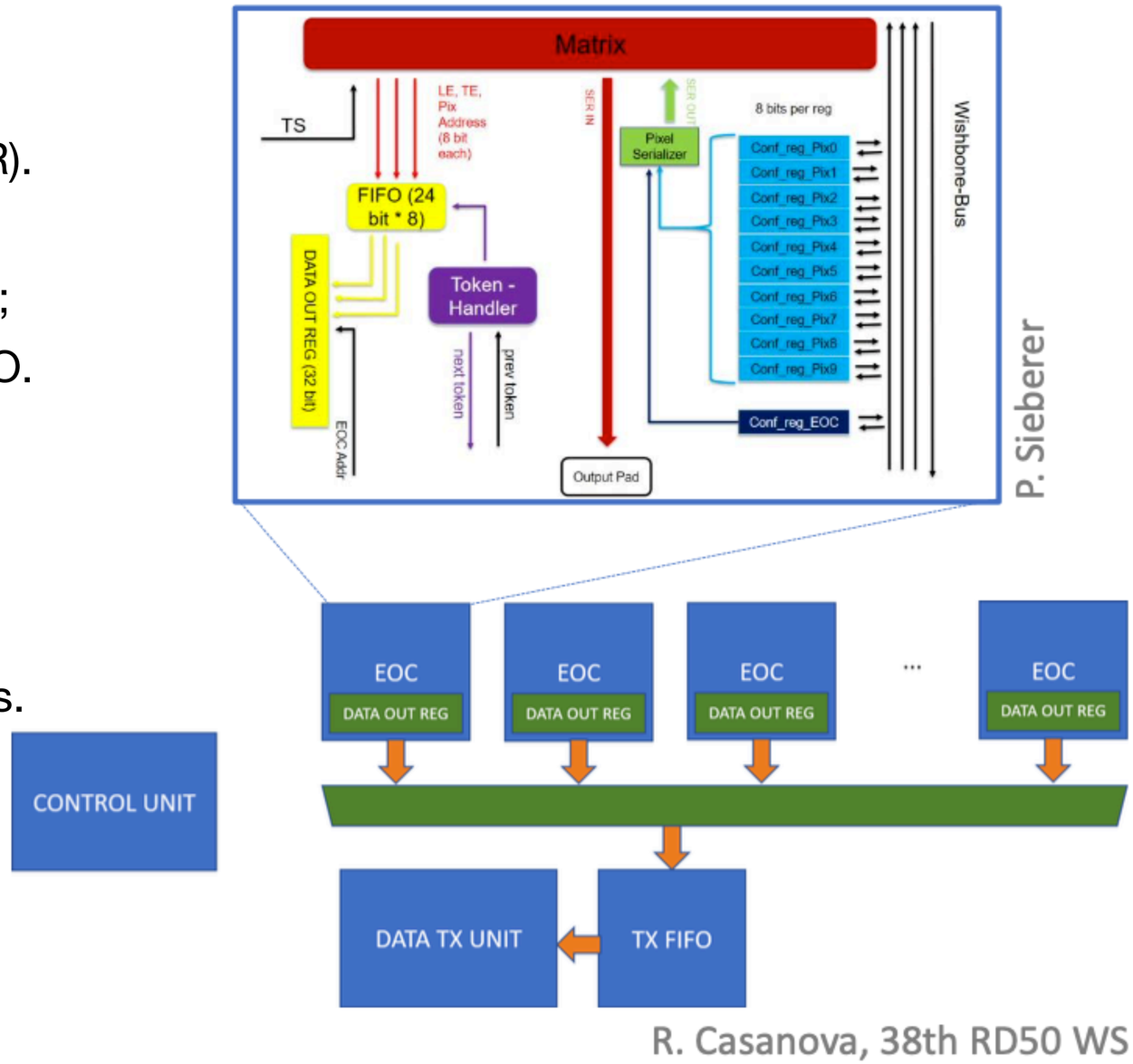
- Each pixel has a 4-bit trimming DAC to compensate threshold voltage variations of its comparator.
- Each double-column provides 24 bits of hit data:
  - time stamps of leading edge (8-bit) and trailing edge (8-bit);
  - 8-bit pixel address in its column.
- The time stamp generator is an 8-bit gray counter operating at 40MHz.



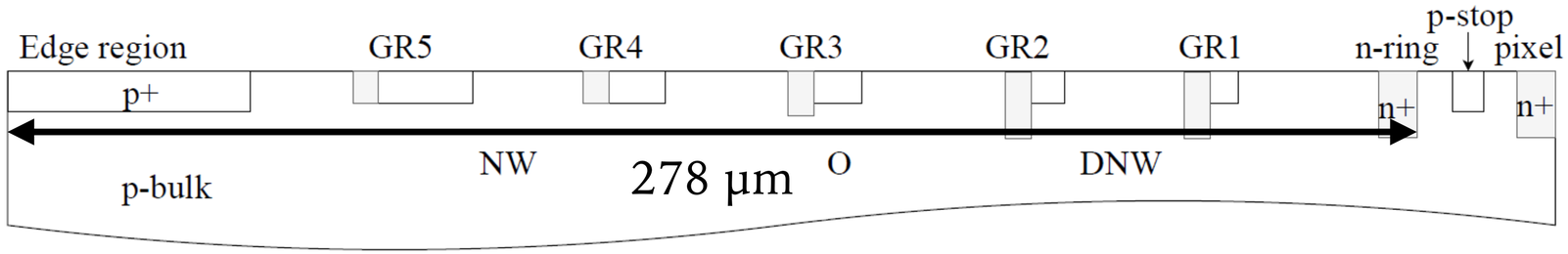


Digital periphery

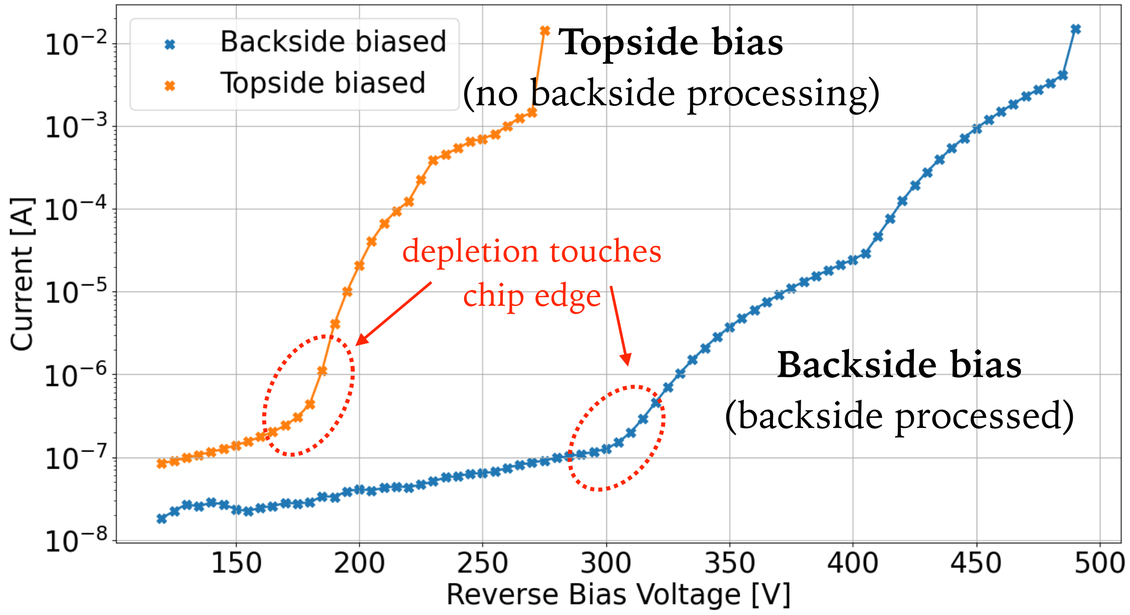
- End of Column (EOC) architecture:
  - Each double column has one EOC;
  - EOC has a FIFO to store hit data (LE, TE and ADDR).
- Readout process:
  - Token mechanism to determine which EOC to read;
  - Hit data from EOC are stored in a transmission FIFO.
  - Data TX unit with LVDS port @640 Mb/s.
- Slow control:
  - Based on I2C protocol for external communication using internal Wishbone bus.
- Needs to be re-designed to meet LHCb specifications.



Results - IV



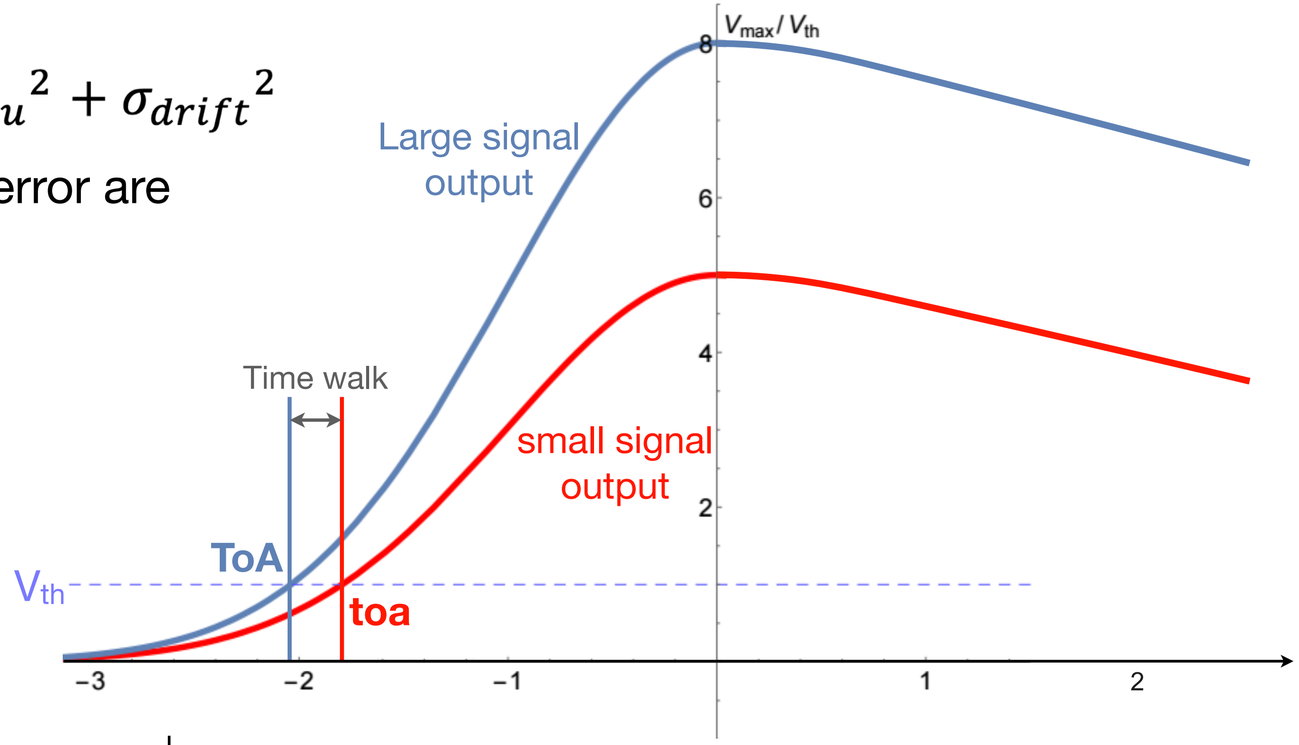
- Improve breakdown voltage with a new chip ring structure.
- High voltage applied from top side or back side:
  - Topside bias (no backside processing): ring leakage jumps to mA at ~200 V;
  - Backside bias (after backside processing): ring leakage jumps at ~400 V.
- The backside processed chip can still be biased to very high voltages.

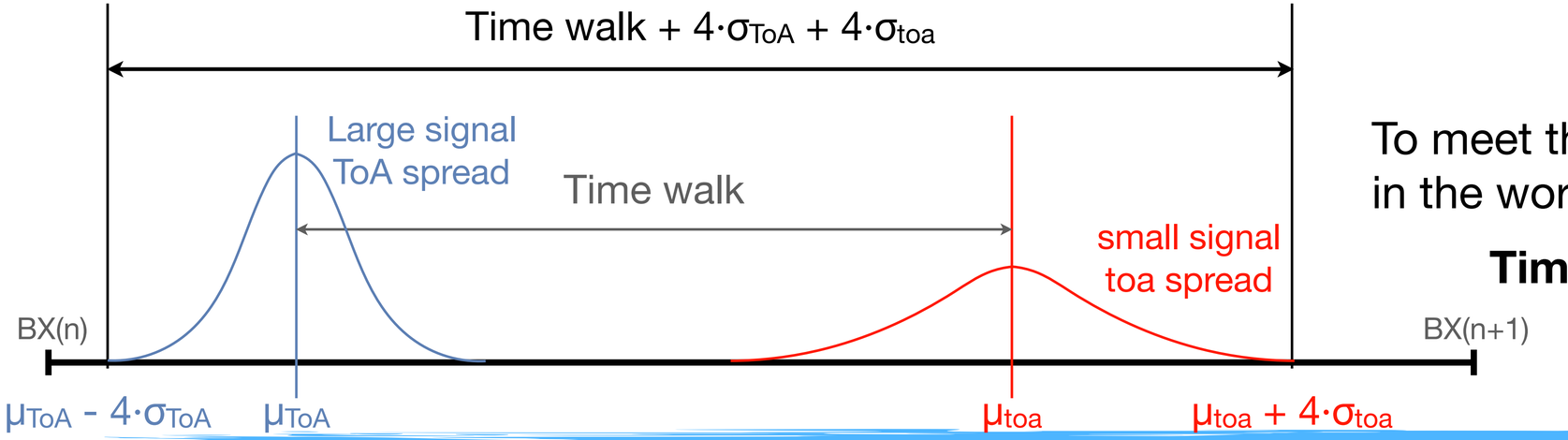


Time resolution requirement

time resolution: $\sigma_t{}^2 \sim \sigma_{jitter}{}^2 + \sigma_{walk}{}^2 + \sigma_{Landau}{}^2 + \sigma_{drift}{}^2$

The main contributions to the time measurements error are jitter (σ_{ToA}) and time walk.





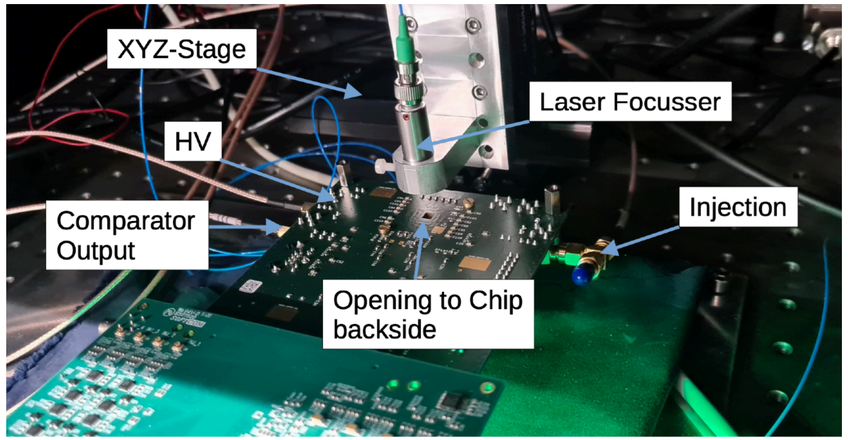
To meet the in-time hit detection requirement, in the worst case:

Time walk + 4·σ_{ToA} + 4·σ_{toa} < 25 ns

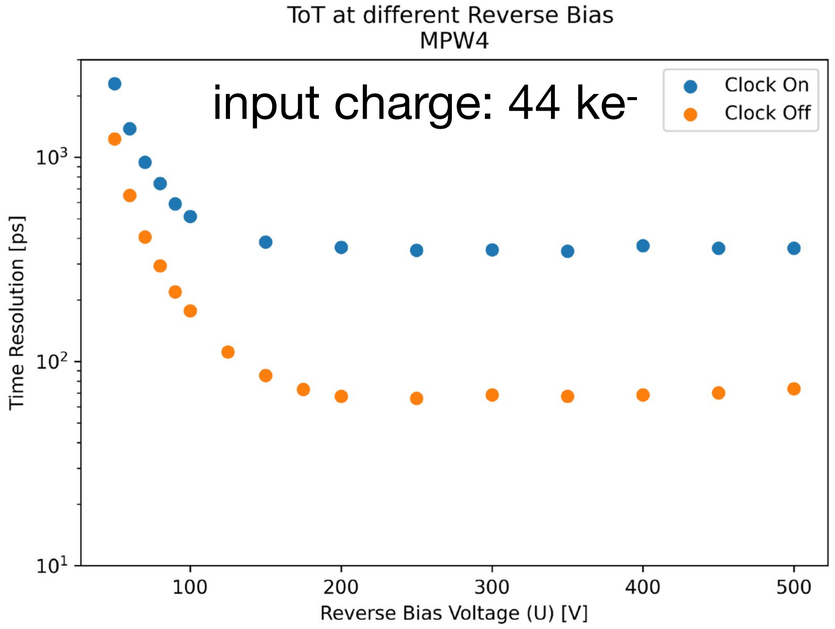
Results - Timing performance

- Timing performance measured by Nikhef using laser.
- Clock introduces noise into pixels and worsens time resolution.
- Better time resolution (σ_{ToA}) with higher bias voltage and larger input charge.
- With V_{th} = 50 mV:
  - Time walk ≈ 10 ns
  - σ_{ToA} ≈ 0.5 ns
  - σ_{toa} ≈ 2.5 ns (small signal 1 ke$^-$)

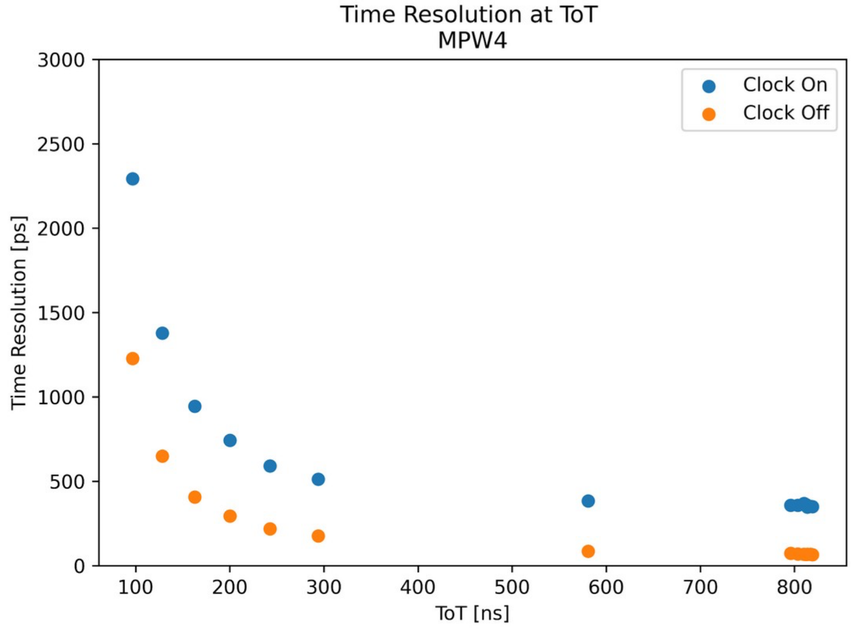
Time walk + 4·σ_{ToA} + 4·σ_{toa} ≈ 22 ns



σ_{ToA}

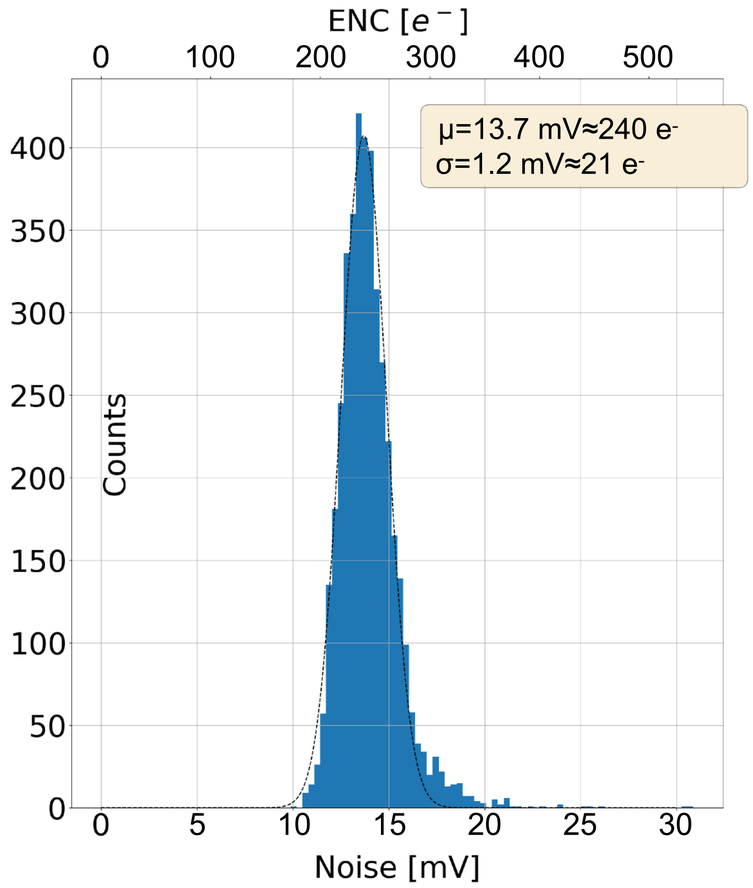


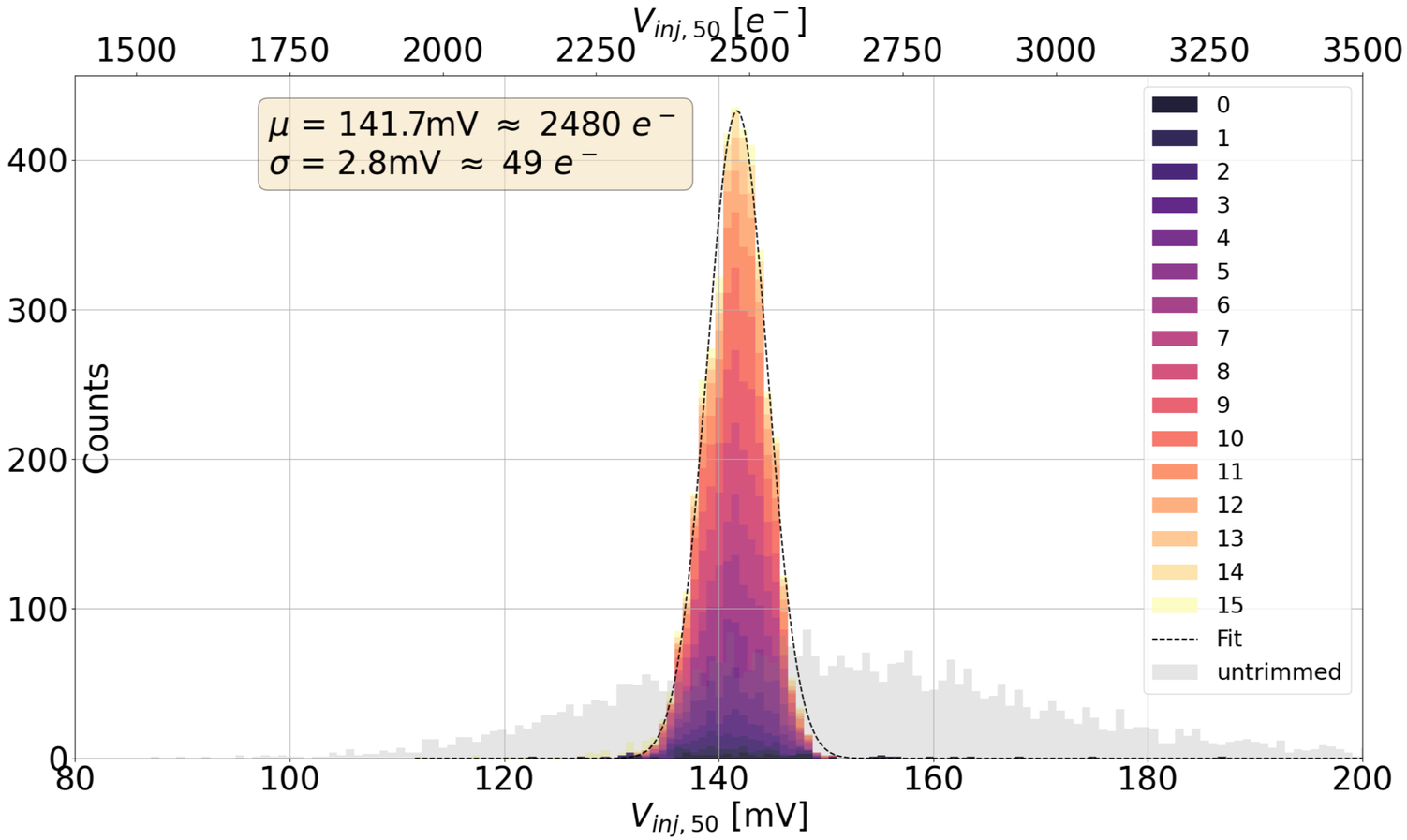
σ_{ToA}



Results - Lab measurement

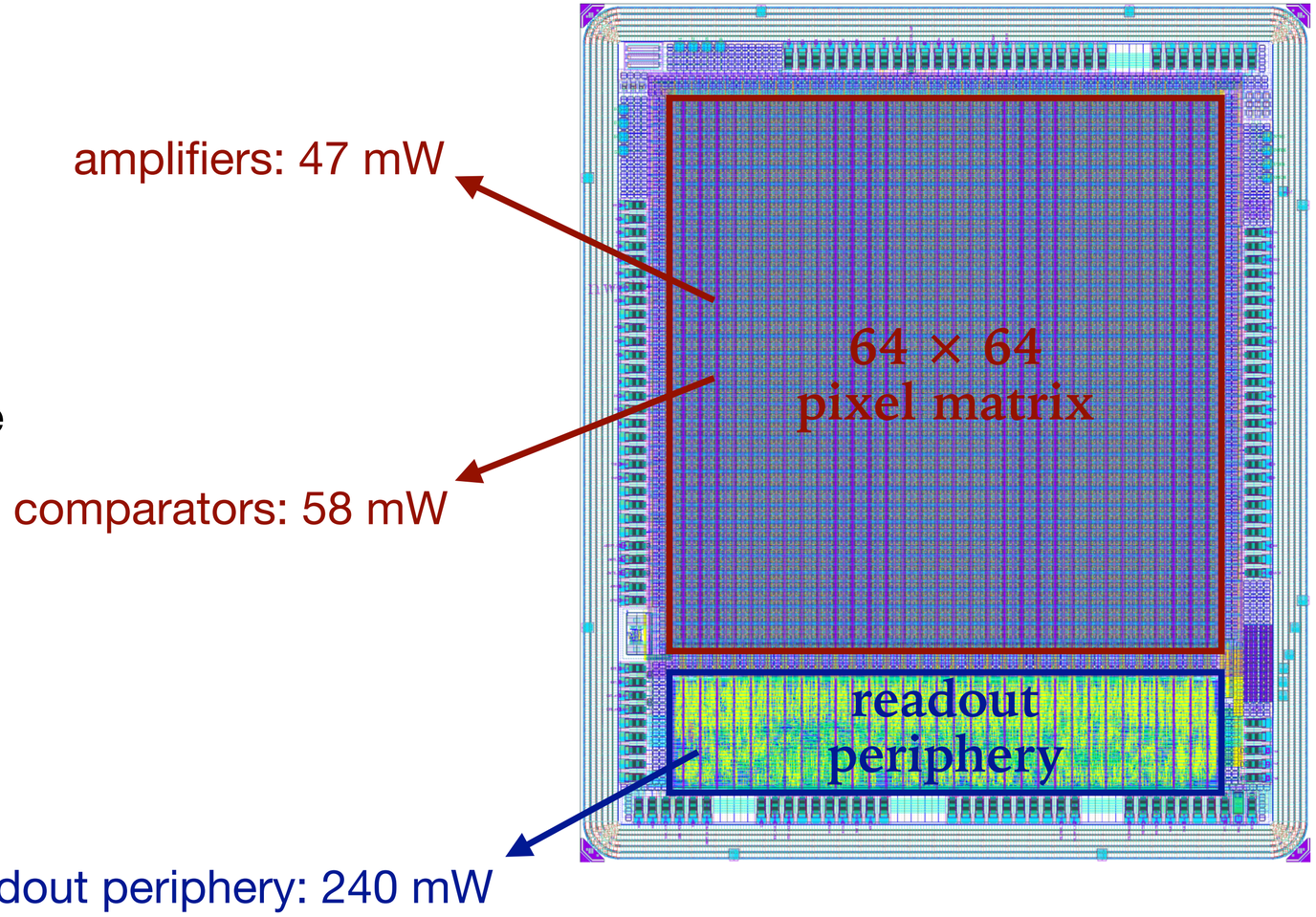
- Pixel noise ~ 240 e-.
- Trimming DAC reduces threshold dispersion over the pixel matrix.
- A low threshold voltage of 50 mV can be used.





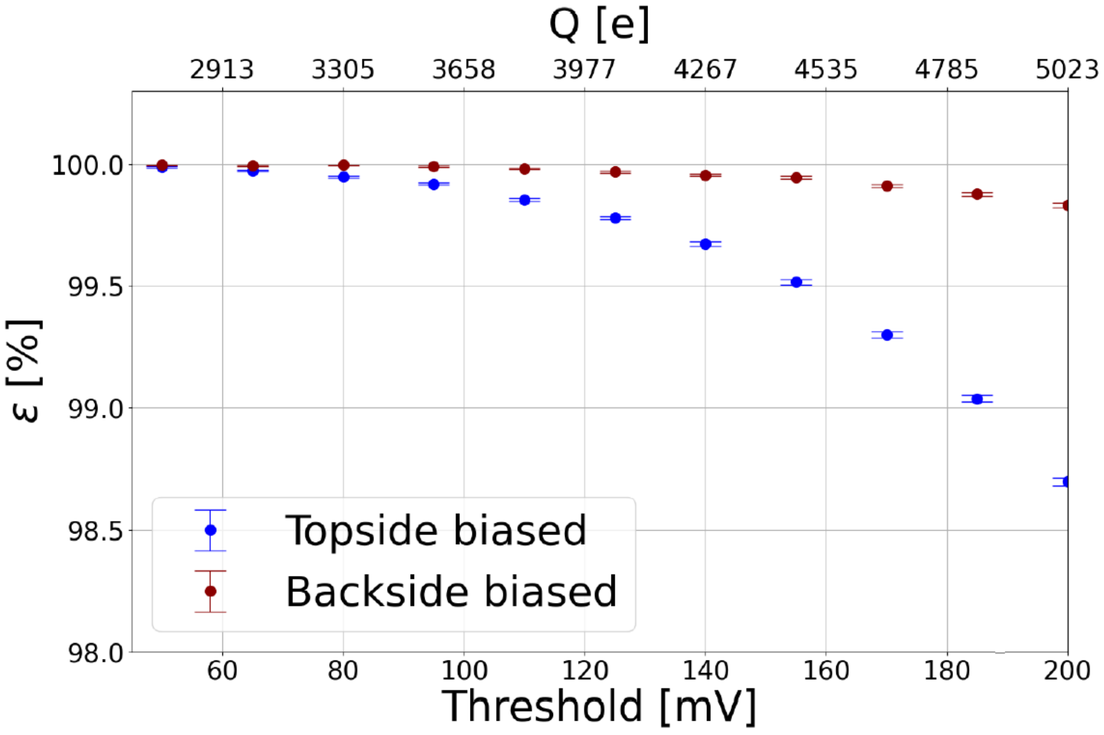
Results - Power consumption

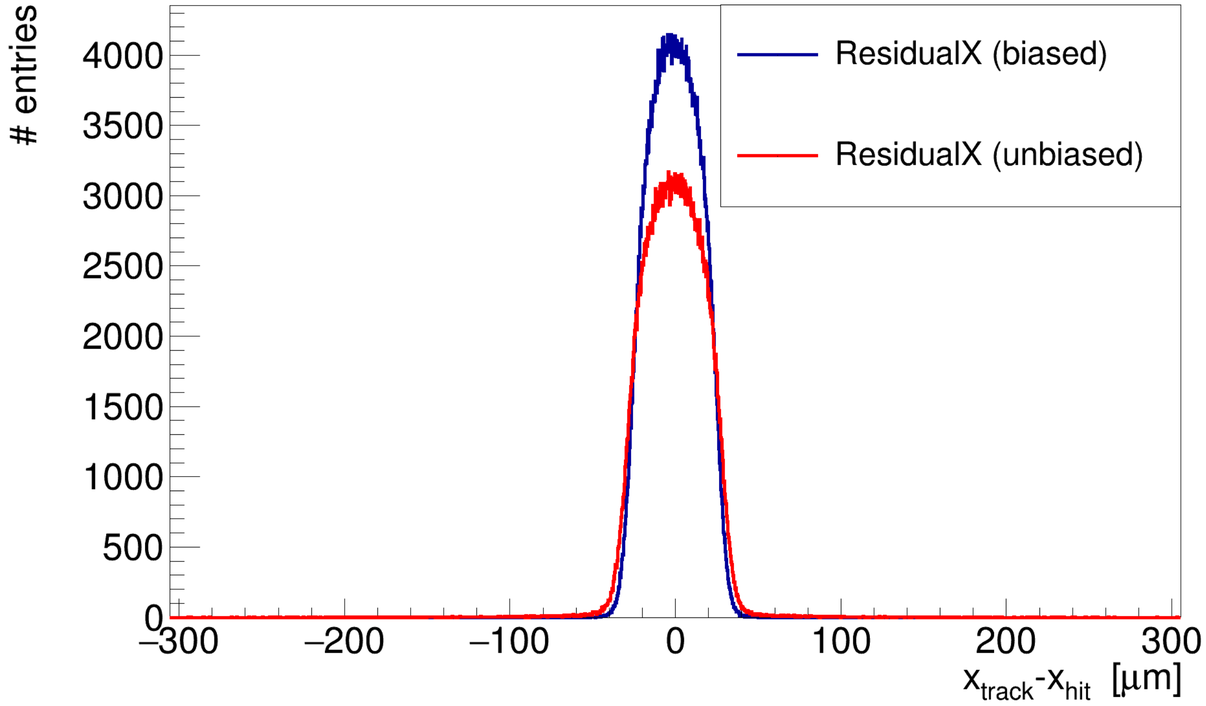
- Power budget of LHCb MightyPix: 150 mW/cm^2.
- Measure the power consumption of different power domains.
- Pixel matrix consumes ~600 mW/cm^2.
  - larger pixel size (considering 100 μm);
  - improve pixel design for lower power consumption.
- Digital periphery will be modified based on the LF-MightyPix chip.



Results - Testbeam

- Testbeam at DESY in April with non-irradiated samples, data analysis ongoing.
- High efficiency > 99.99% achieved.
- Spatial resolution $\sigma_x \approx 17.8$ µm, matches the expected value (pixel pitch 62 µm $/\sqrt{12} \approx 17.9$ µm).

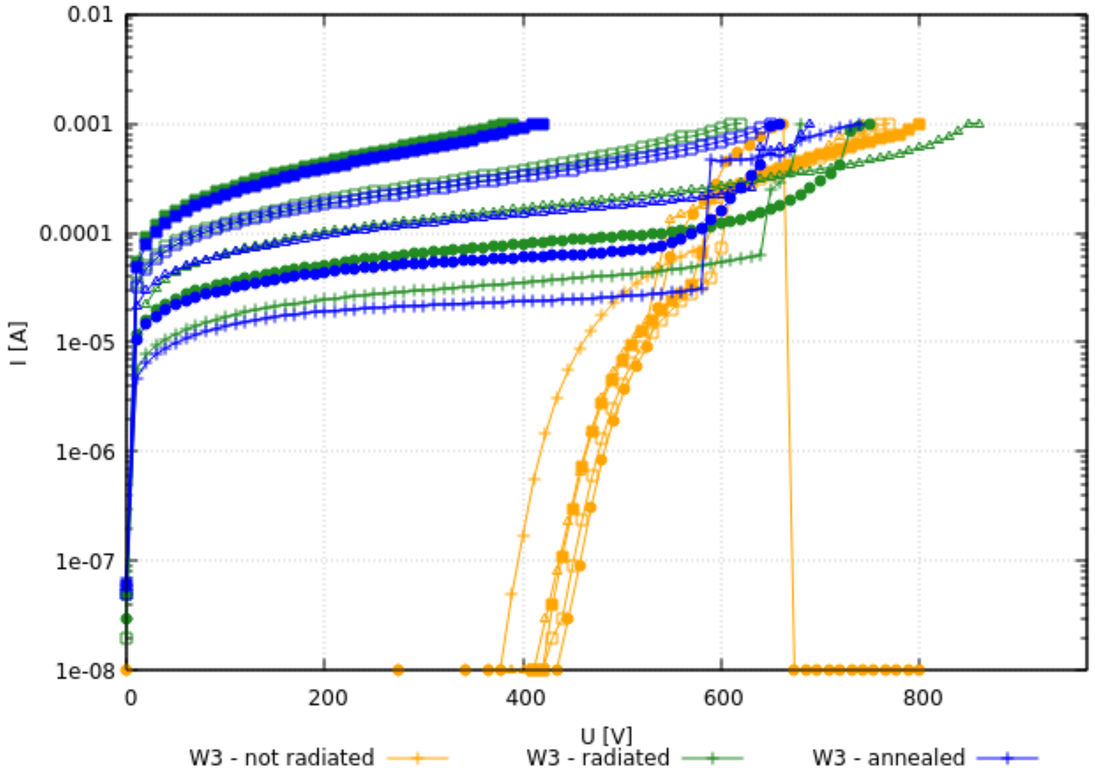




Irradiation campaign

- samples have been neutron irradiated in Ljubljana: 1e14, 3e14, 1e15, 3e15, 1e16, 3e16 n_{eq}/cm^2.
- IV measurements at room temperature show leakage current rise after irradiation.
- Irradiated samples can still be biased to high voltages.
- Samples are being measured in laboratory now.

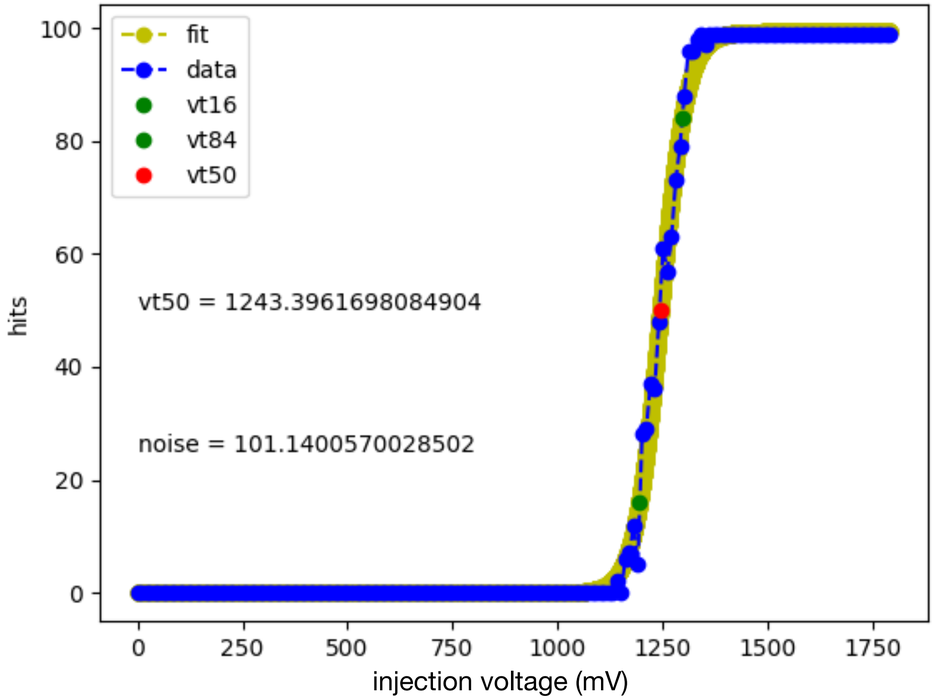
- Chips in the plots are backside processed and irradiated to 1e14, 3e14, 1e15, 3e15 and 1e16 n_{eq}/cm^2.
- Chip ring current measured at room temperature about **10 °C**.
- Annealing for 80 min at 60 °C.



Irradiated samples

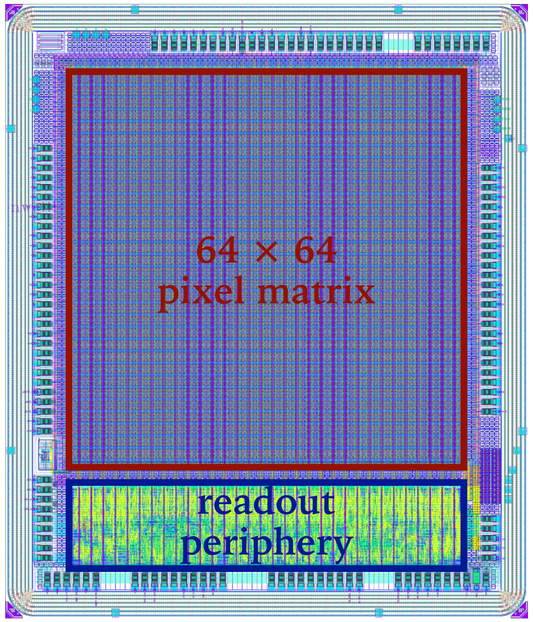
- Has just started testing a 3e15 n_{eq}/cm^2 irradiated sample (not backside processed).
- S-curve measurements show the readout electronics are functioning.
- More measurements using radioactive sources and in test beam.
- Beam test on irradiated samples at DESY in late September.

- measured at room temperature
- biased at 100 V
- 50 mV threshold voltage
- 100 injections for each voltage
- ENC ~ 850 e^-



RD50-MPW4 summary

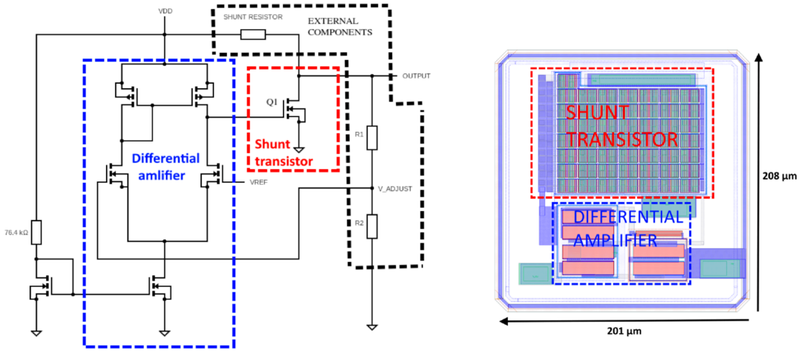
- RD50-MPW4 a successful HV-CMOS prototype.
- High breakdown voltage for high irradiation tolerance:
  - just started testing 3e15 n_{eq}/cm^2 sample, readout electronics still functioning;
  - more measurements on irradiated samples to be followed in lab and test beam.
- To be improved for LHCb:
  - better timing performance;
  - lower power consumption;
  - make the digital readout periphery compatible with LHCb (lpGBT protocol, meet the TFC and ECS requirements), enable daisy chain, 4 fast data links;
  - use radiation hard electronics (circular transistors, triple-redundancy digital circuits);
  - reduce I/O pads to only one side of the chip.

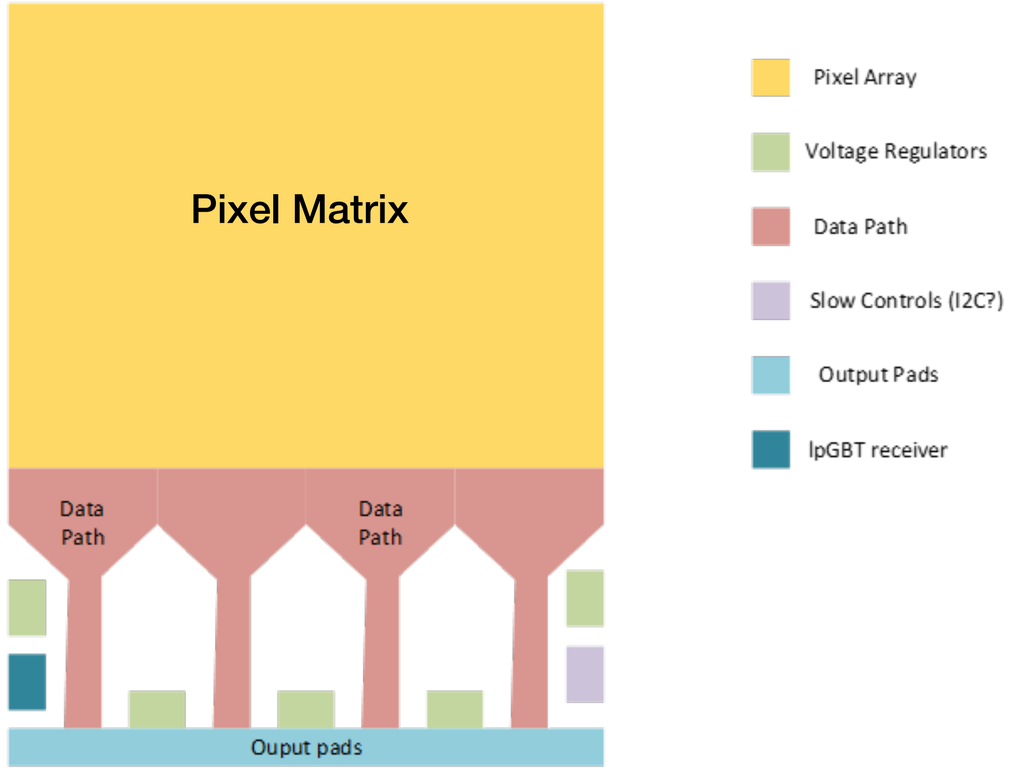


New design for LHCb: RadPix

- **RadPix** (in collaboration with RAL).
- Same pixel matrix structure from RD50-MPW4.
- Lower power consumption:
  - larger pixel size (considering 100 μm);
  - improved pixel design.
- Digital periphery compatible with LHCb requirements (re-use from LF-MightyPix).
- Add voltage regulation to enable serial powering.
- Use a slow control faster than the I2C used in RD50-MPW4.
- Use a thinner chip ring to reduce dead area.

Shunt regulator design





Preliminary RadPix block diagram