RadPix: Brainstorming

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Requirements – From physics (discussion in progress)

- **RadPix must have (for Mighty Tracker):**

Parameter	Value
Chip size [cm × cm]	~ 2 × 2
Sensor thickness [µm]	200
Pixel size [µm × µm]	< 100 × 300
Time resolution [ns]	3 (must be within 25 ns window)
Inactive area [%]	< 5
Power consumption [W/cm^2]	0.15
Data transmission [Gbits/s]	4 links × 1.28 Gbit/s, multiplexed to 2 and 1 links
Data rate [MHz/cm^2]	17
NIEL [1 MeV n_{eq}/cm^2]	3E14 (includes 2 safety factor already)
TID [MRad]	40

Requirements – From physics (discussion in progress)

- **RadPix must have (for UP):**

- Main differences between two detectors (all other values I think are not an issue)

Key numbers :

Characteristics	Specification
Hit rate in hot event and region	160 MHz / cm^2 pp * (~52.5 hits / cm^2 / BX for Pb/Pb)
Time resolution	O(1 ns) for BX tagging (> 99% In-Time Eff.)
Space resolution	~ 5 µm
Power consumption	O(100-300 mW/cm^2)
Radiation dose for 350 fb^{-1}	3×10^{15} 1-MeV n_{eq}/cm^2, 240 Mrad

** From FDTR ; the hit density is currently under revision*

Hit rate

Possibility to ignore sensors closest to the beam pipe?

From LHCb upgrade electronics workshop 2024 (Fabrice Guilloux)

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Requirements – Compatibility with LHCb online system

- **RadPix must:**
  - Run with the LHC clock at 40 MHz **(already exists in RD50-MPW chips)**
  - Use the lpGBT protocol for communication **(NEW!)**
    - Maximum input voltage 1.2 V (HV-CMOS chip has VDD = 1.8 V)
    - Protocol compliance (VELO scrambler (8b/10b encoding), clock-data recovery, etc.)
    - I/O standards (LVDS, CML)
    - Clocking requirements (clock tolerance, jitter and synchronisation method between HV-CMOS chip and lpGBT) and latency
    - Data rate (≤10.24 Gbps)
    - …
  - Meet Timing and Fast Control (TFC) + Experiment Control System (ECS) **(NEW!)**
    - TFC controls the entire readout of the LHCb detector. It is essential for ensuring that the entire detector is working in a synchronised manner, with minimal delays between collision events and data collection
    - Full details here

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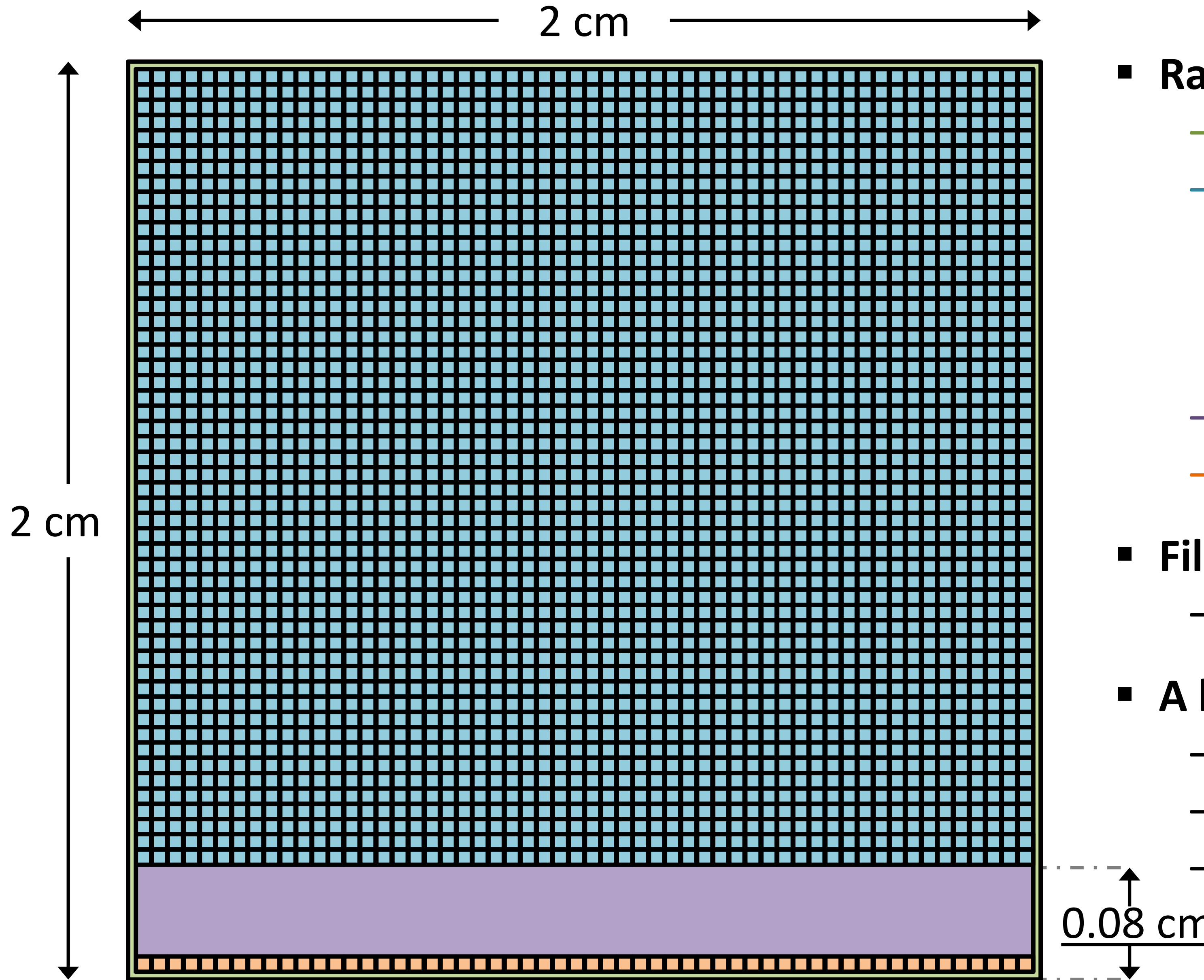
RadPix draft floorplan



- **RadPix contents (assumptions)**
  - Chip ring (width 100 µm)
  - Pixel matrix
    - 100 µm × 100 µm pixels
    - 192 rows × 198 columns
    - Total of 38,016 pixels
  - Digital periphery
  - I/O pads
- **Fill-factor requirement**
  - Dead area <5%
- **A bit of maths**
  - Sensitive area = # pixels × pixel area
  - Sensitive area = 3.8016 cm^2
  - Dead area = 100 × [1 – (sens. area/total area] = **4.96%**

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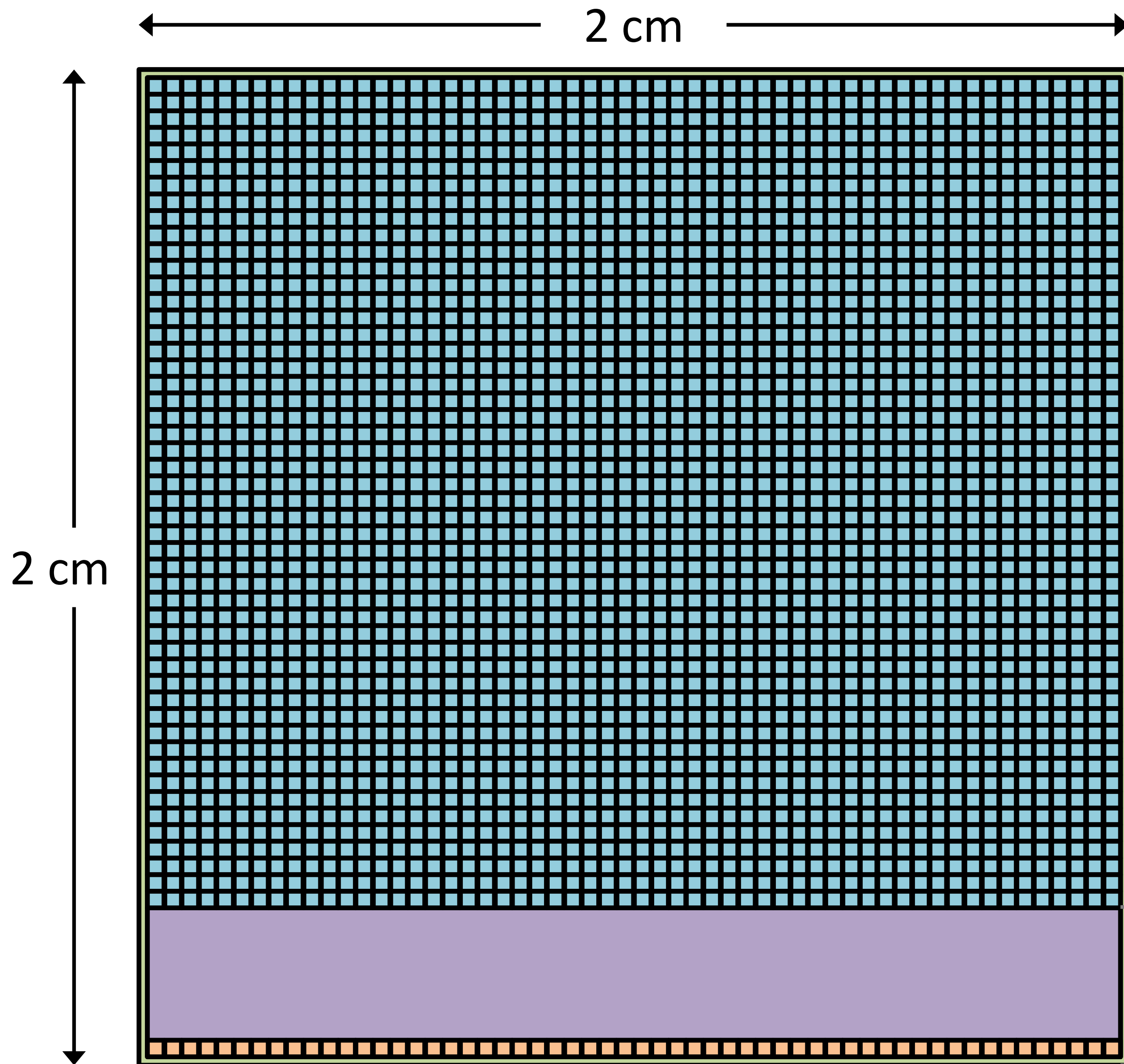
RadPix draft floorplan



- **RadPix contents (assumptions)**
  - Chip ring (width 100 µm)
  - Pixel matrix
    - 100 µm × 100 µm pixels
    - 190 rows × 198 columns
    - Total of 37,620 pixels
  - Digital periphery
  - I/O pads
- **Fill-factor requirement**
  - Dead area <5%
- **A bit of maths**
  - Sensitive area = # pixels × pixel area
  - Sensitive area = 3.762 cm^2
  - Dead area = 100 × [1 – (sens. area/total area] = **5.95%**

Not good enough

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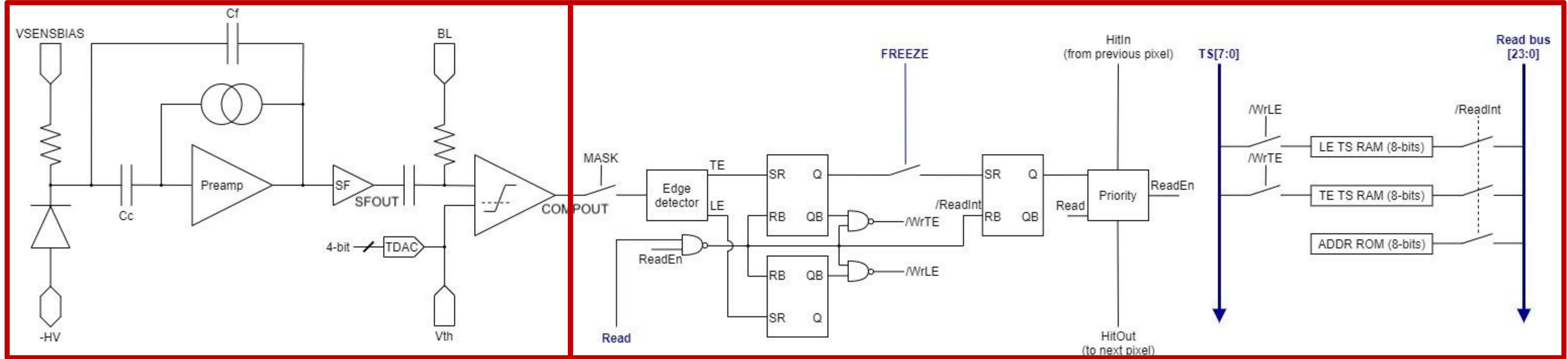
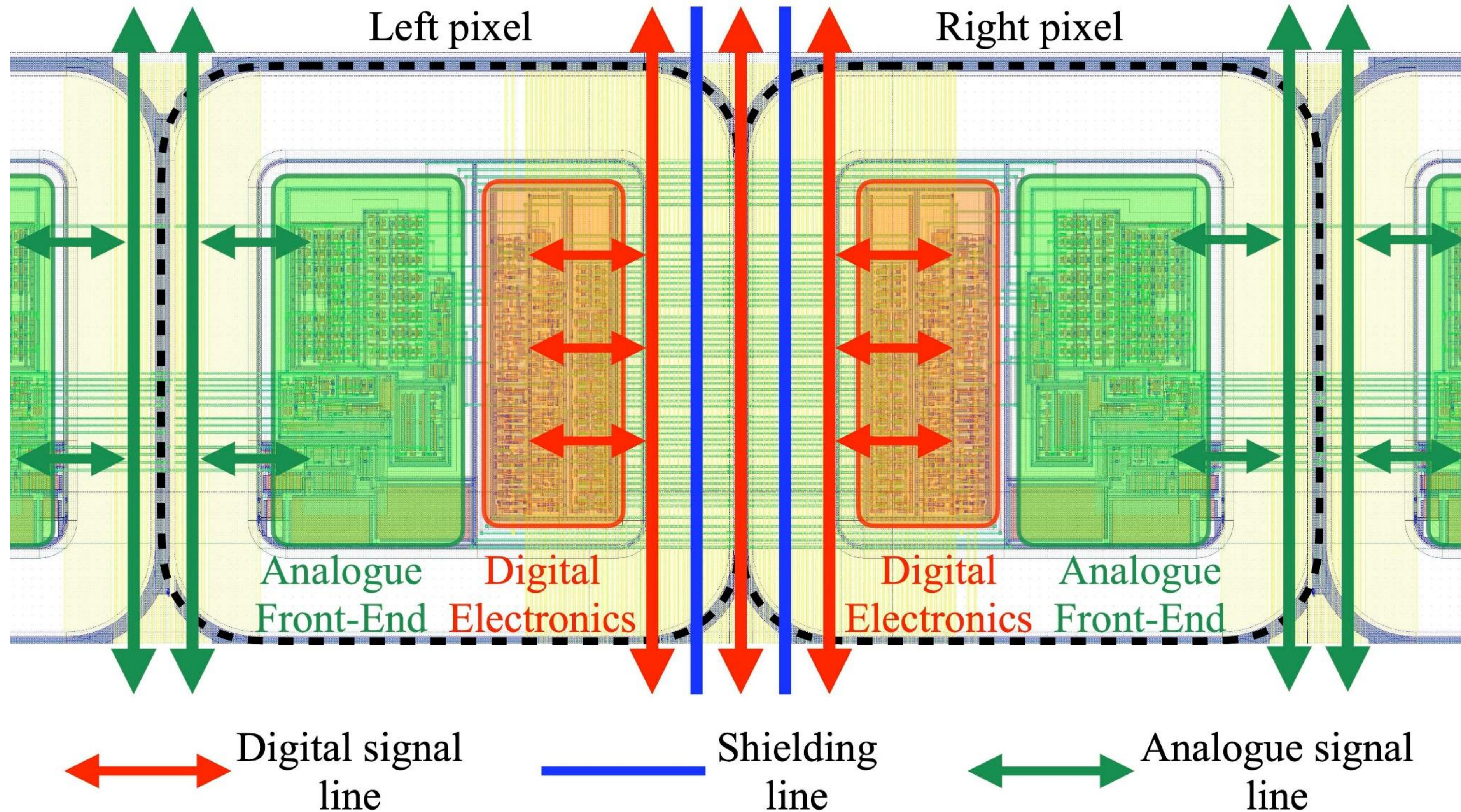
Pixel electronics as in RD50-MPW4

Analogue readout   Digital readout



- **Column drain architecture (FE-I3 style)**
- **Electronics to**
  - Mask noisy pixels (MASK)
  - Possibility to pause digitisation of new hits until readout is complete (FREEZE)
  - 8-bit SRAM shift register for serial configuration
    - Pixel-trimming to compensate for threshold voltage variations (4-bits)
    - Flag to mask noisy pixels (1-bit)
    - Signals to enable/disable calibration circuit (1-bit), SFOUT (1-bit), COMPOUT (1-bit)

RD50-MPW4 pixel layout



Double column scheme to alleviate routing congestion and minimise crosstalk

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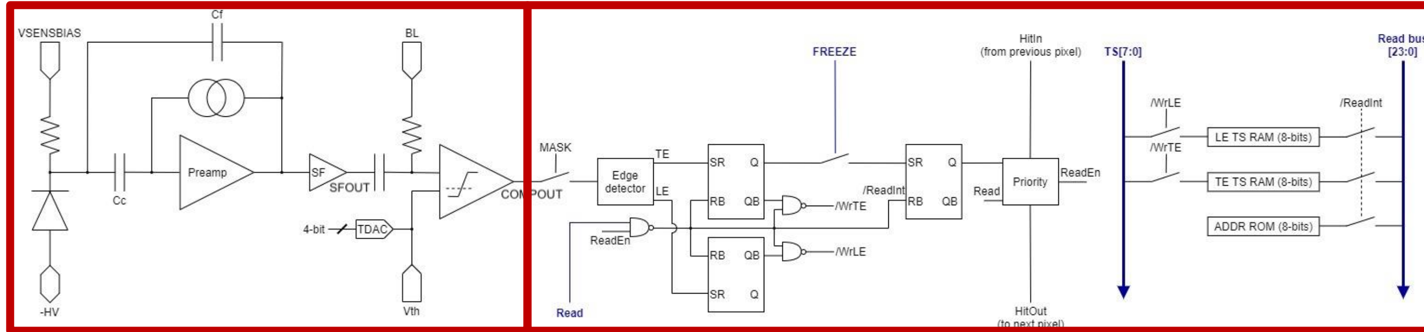
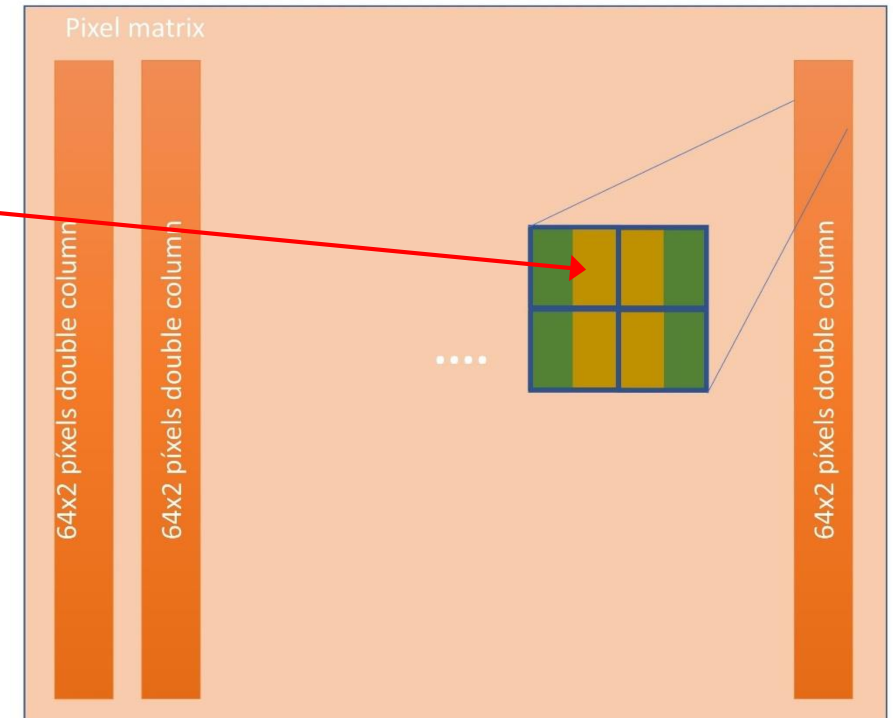
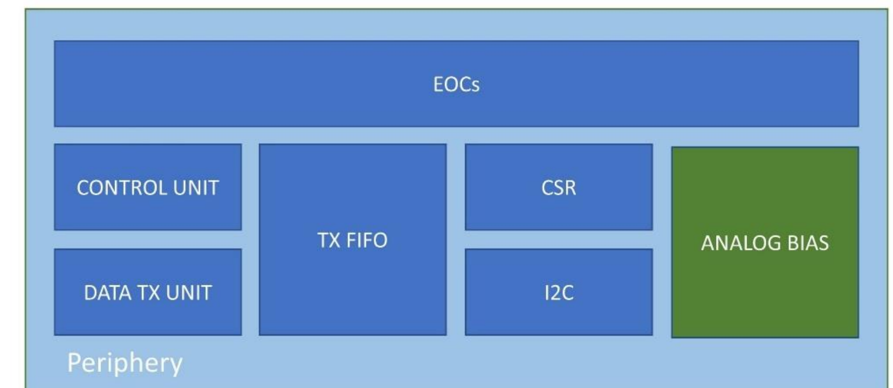
RD50-MPW4 block diagram







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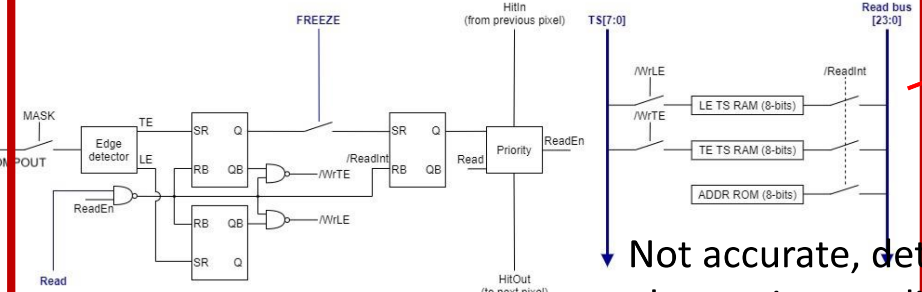
Pixel electronics as in MightyPix and LF-MightyPix

1.8 V
Bias resistance
Base line
Pixel
Comparator
Tout
Threshold
Amplifier
Sensor
C_{inj}
EnInjection
- HV
AmpOut
Offset
VMinus
Data Transfer Line
Injection
RAM
TDAC
WrRAM
Row control
Column control
Hit buffer

29 Columns
Pixels
(320 per col)
Hit buffers
(320 per col)
EoC buffers
(1 per col)
Col0
Col1
...
Col28
Readout Logic

- Edge detector
- Priority system
- ROM and DRAMs to store hit data



Not accurate, details of electronics are different

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Pros. and cons of each option

	Pros	Cons
In-pixel (RD50-MPW)	Reduces dead area Dead area does not scale with matrix size No crosstalk Proven to work (MonoPix)	Larger pixel capacitance (pixel needs larger PSUB) → higher noise Potential clock distribution problems (buffers needed) Potential higher power consumption (for buffers)
In periphery (MightyPix)	Simpler clock distribution Potential lower power consumption Proven to work (ATLASPix)	Pixel location dependent gradients (COMPOUT routing lines have different lengths) → worse timing resolution Potential crosstalk problems Larger dead area (should still be possible to meet <5% requirement), it scales with matrix size Not enough metal layers to route COMPOUT to peripheral digital readout in full-size chip? Limits use of high metal layers for powering

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Data word

- **LHCb uses 32-bit data words (or multiples of 32-bit)**
  - More bits per hits means smaller data rate
- **In RadPix we need:**
  - Row address: 9-bit (2^9 = 512 values, RadPix will have >256 pixels in a double column)
  - Column address: 7-bit (2^7 = 128 values, RadPix will have <100 double columns)
  - Leading edge time-stamp: 8-bit (is this enough? We probably want more?)
  - Trailing edge time-stamp: 8-bit (is this enough? We can probably survive with less?)

  - TOTAL so far = 32-bit

  - *Recommendation to leave a few unused bits for sync pattern + detecting potential errors*

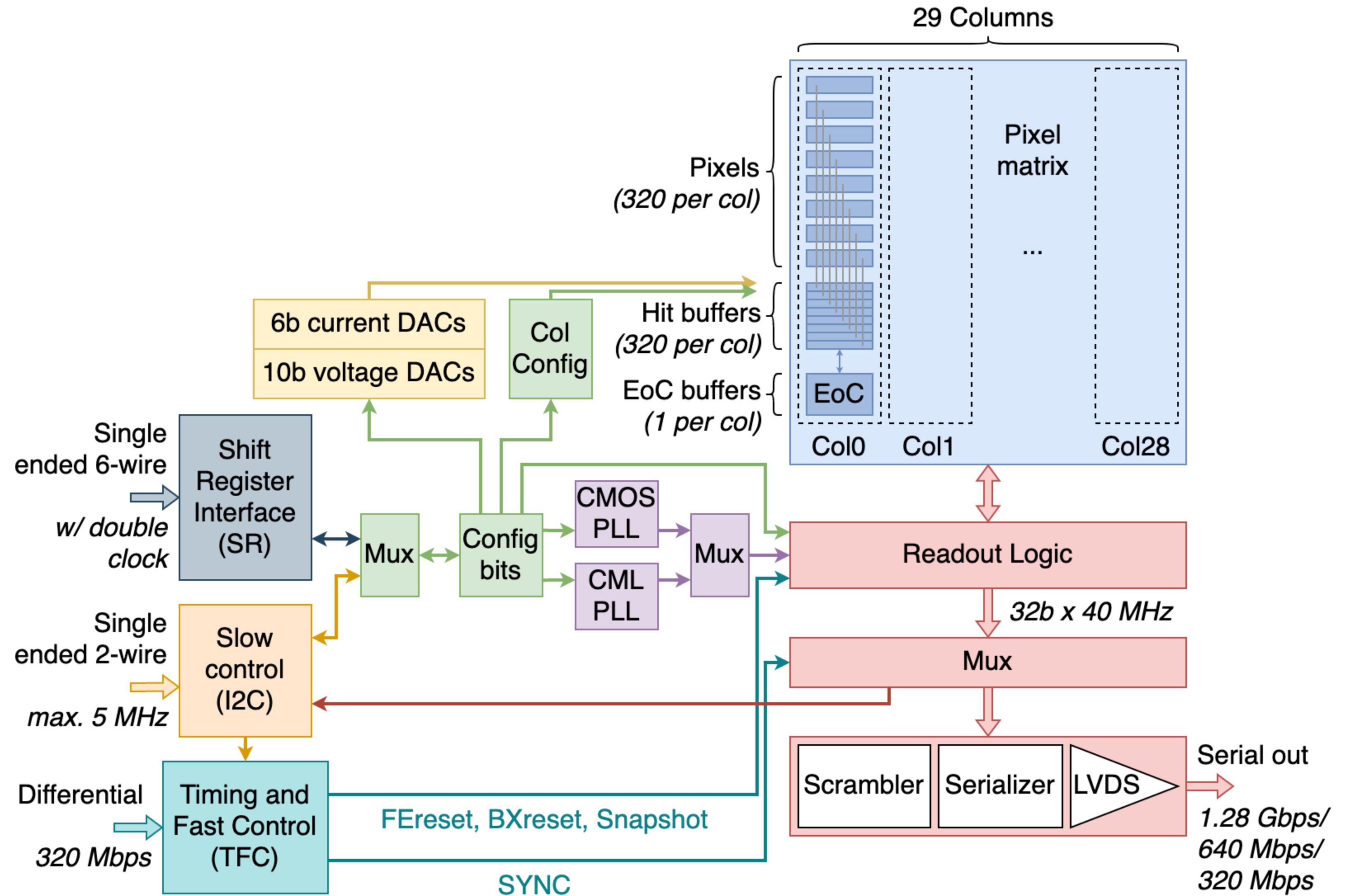
Data rate

- **RadPix sensitive area :**
  - (192 rows × 198 columns) × 100 µm × 100 µm = 3.8016 cm^2
- **Maximum rate sent off chip w/o any losses:**
  - (4 × 1.28 Gbit/s) / (32-bit × 3.8016 cm^2) = 42 MHz/cm^2
  - Good enough for the Mighty Tracker, but not for the UP
  - Depth of FIFOs in the periphery to avoid loosing hits? In other words, how many hits need to store? (num. of 1.28 Gbit/s is four per 2 cm × 2 cm chip)

Voltage regulation

- **RadPix allowed power consumption**
  - 0.150 W/cm^2
  - Chip requires a few different power domains (VDDA, VDDD, VSSA)
- **Mighty Tracker staves**
  - Will have 4-5 chips per serial group
  - How many on a chain not decided yet

MightyPix1 block diagram



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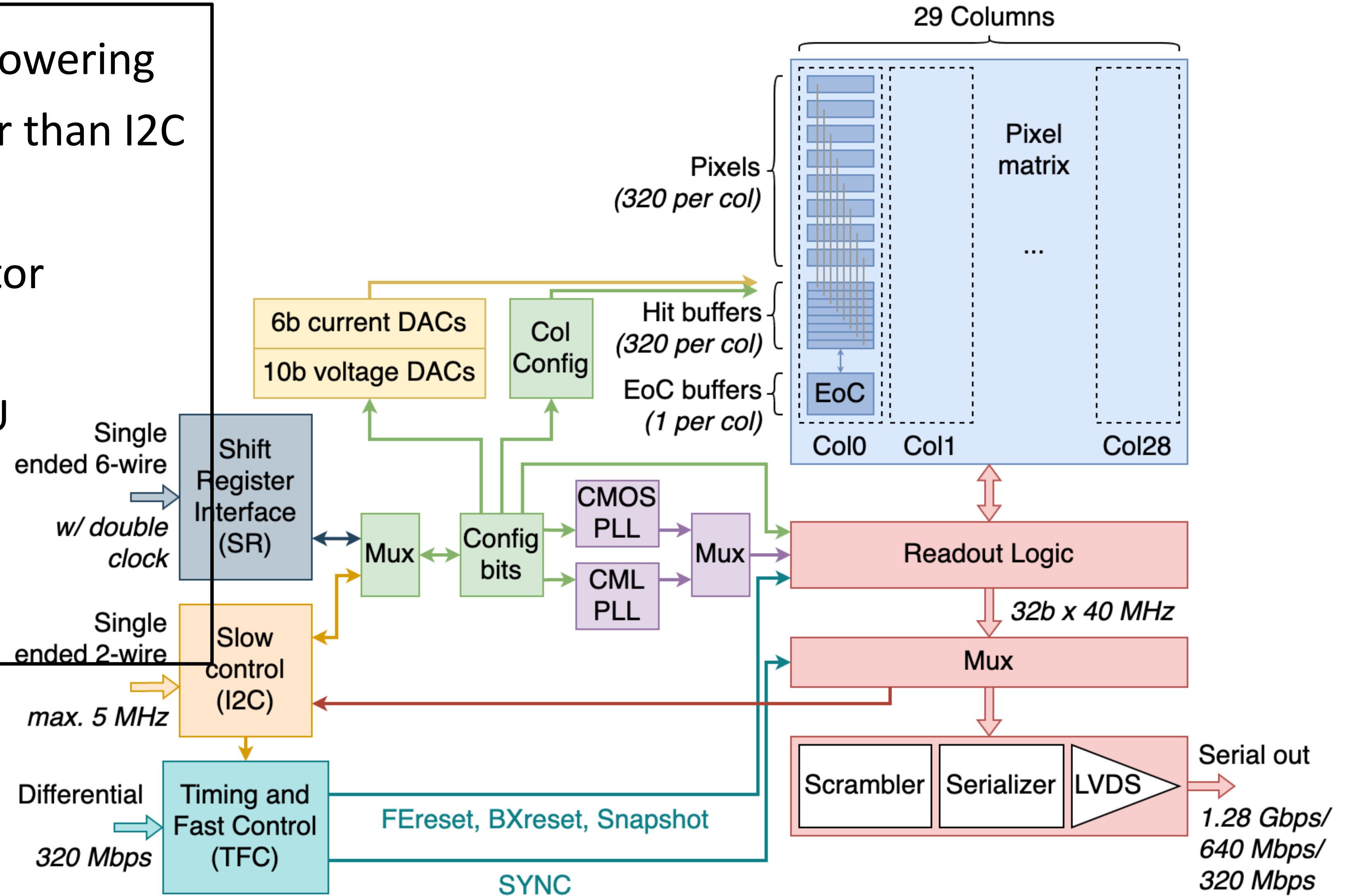
MightyPix1 block diagram – Missing blocks

- Voltage regulation for serial powering
- Differential slow control faster than I2C
- Command decoder
- Daisy chain and data aggregator
- Options for multiplexing links
- Triple redundancy against SEU
- HV switch (?)
- Temperature sensor
- Other things I have missed



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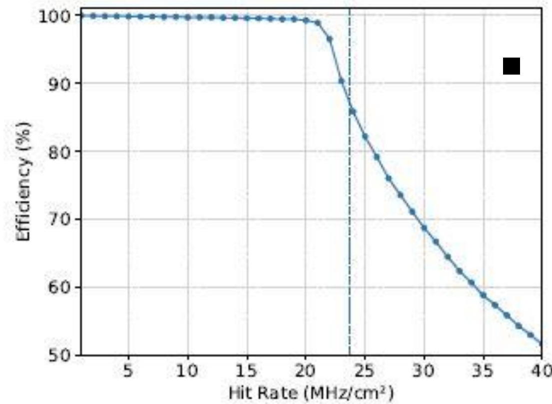
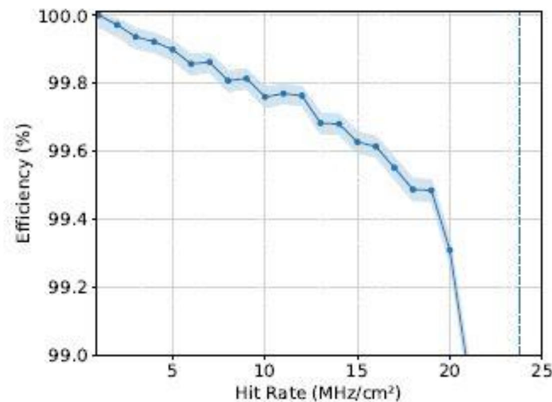
MightyPix1 – Efficiency simulations

https://doi.org/10.1088/1748-0221/19/04/C04045



(a) Simulated MightyPix1 readout efficiency for hit rates up to 40 MHz cm^{-2}.



(b) Simulated MightyPix1 readout efficiency in the over 99 % region.

Figure 6.3.1: (a) The simulated MightyPix1 readout efficiency drops off at a hit rate of 21 MHz cm^{-2}, which is before the readout limit of 23.75 MHz cm^{-2} *(dashed line)*. (b) At hit rates below 21 MHz cm^{-2} the simulated readout efficiency of MightyPix1 is above 99 %. The blue band shows the C-P interval. It is too narrow to be visible in (a).

- **Maximum rate sent off chip w/o any losses:**
  - (1 × 1.28 Gbit/s) / (2 × 32-bit × 0.8422 cm^2) = **23.75 MHz/cm^2**

29 Columns
Pixel matrix
...
Pixels (320 per col)
Hit buffers (320 per col)
EoC buffers (1 per col)
EoC
Col0 Col1 Col28
6b current DACs
10b voltage DACs
Col Config
Single ended 6-wire w/ double clock
Shift Register Interface (SR)
Mux
Config bits
CMOS PLL
CML PLL
Mux
Readout Logic
32b x 40 MHz
Mux
Single ended 2-wire max. 5 MHz
Slow control (I2C)
Differential 320 Mbps
Timing and Fast Control (TFC)
FEreset, BXreset, Snapshot
SYNC
Scrambler
Serializer
LVDS
Serial out
1.28 Gbps/ 640 Mbps/ 320 Mbps

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MightyPix1 – Efficiency simulations

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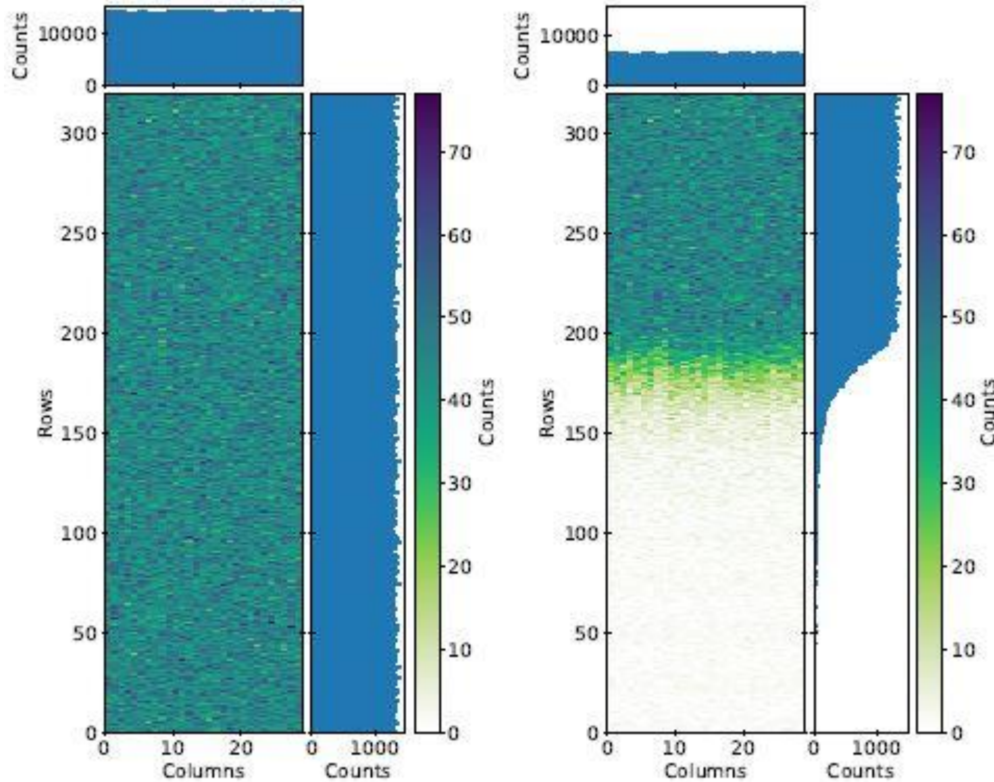

(a) Simulated hits across the MightyPix1 pixel matrix.

(b) Missing hits across the MightyPix1 pixel matrix.

Figure 6.3.5: At a hit rate of 40 MHz cm^{-2} the **(a)** simulated hits are evenly distributed across the MightyPix1 pixel matrix *(heat map)*. All 29 columns *(histogram above)* contain about the same number of hits, as do all of the 320 rows *(histogram to the side)*. The distribution of **(b)** missing hits shows a clear trend at 40 MHz cm^{-2}, with nearly all hits missing in the top half of the pixel matrix rows.

sent off chip w/o any losses:

ɔit/s) / (2 × 32-bit × 0.8422

5 MHz/cm²

29 Columns
Pixels
(320 per col)
Pixel matrix
...
Hit buffers
(320 per col)
EoC buffers
(1 per col)
EoC
Col0
Col1
Col28
6b current DACs
10b voltage DACs
Col Config
Shift Register nterface (SR)
Mux
Config bits
CMOS PLL
CML PLL
Mux
Readout Logic
32b x 40 MHz
Mux
Slow control (I2C)
ming and ıst Control (TFC)
FEreset, BXreset, Snapshot
SYNC
Scrambler
Serializer
LVDS
Serial out
1.28 Gbps/
640 Mbps/
320 Mbps

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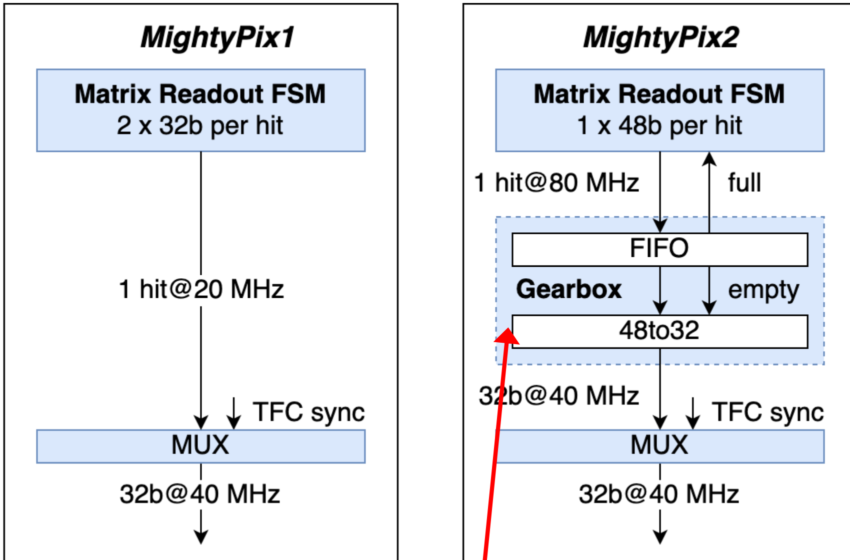
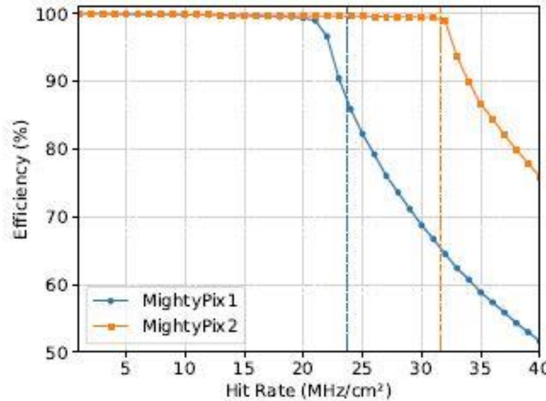
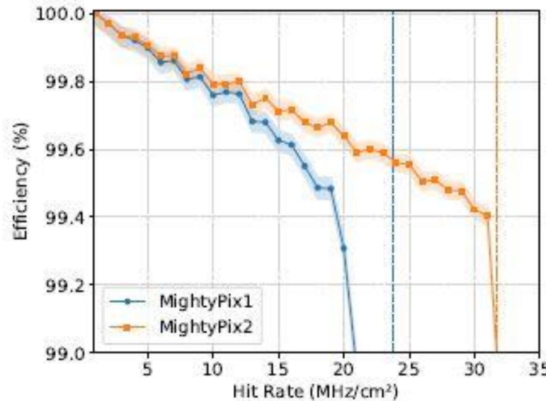
LF-MightyPix, MightyPix2 – Improvement



(FIFO depth 16 hits)

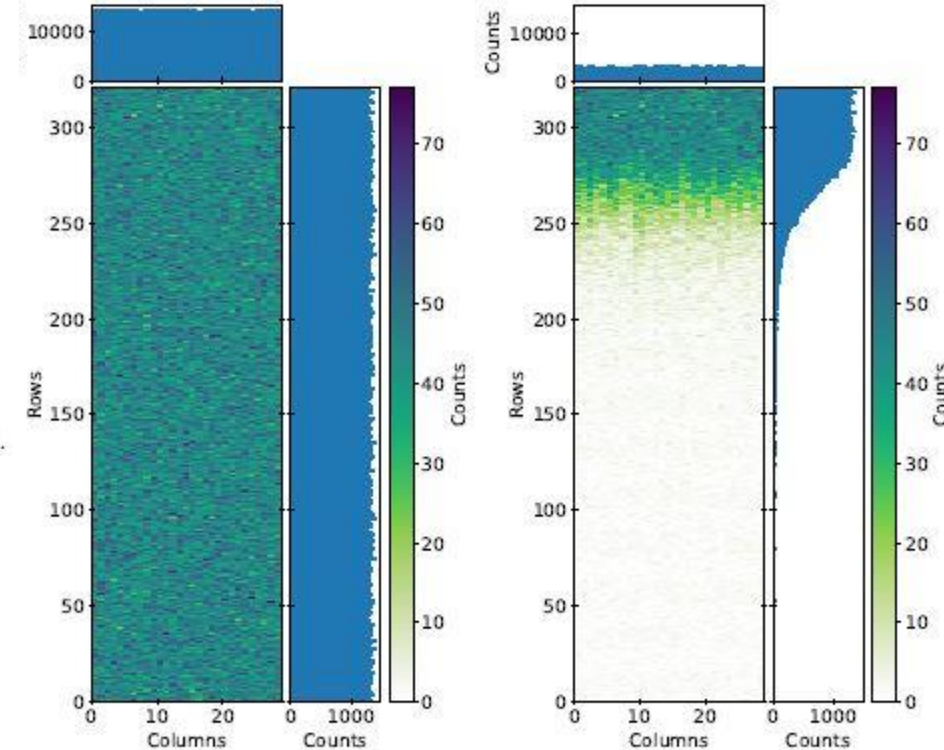


(a) Simulated MightyPix2 readout efficiency for hit rates up to 40 MHz cm^{-2}.



(b) Simulated MightyPix2 readout efficiency in the over 99 % region.

Figure 7.3.1: While the simulated readout efficiency of MightyPix1 *(blue)* drops off before the readout limit of 23.75 MHz cm^{-2} *(blue dashed line)* is reached, the simulated efficiency of the proposed MightyPix2 readout system *(orange)* is over 99 % up to the new readout limit of 31.66 MHz cm^{-2} *(orange dashed line)*. The blue and orange bands show the C-P interval. They are too narrow to be visible in (a).

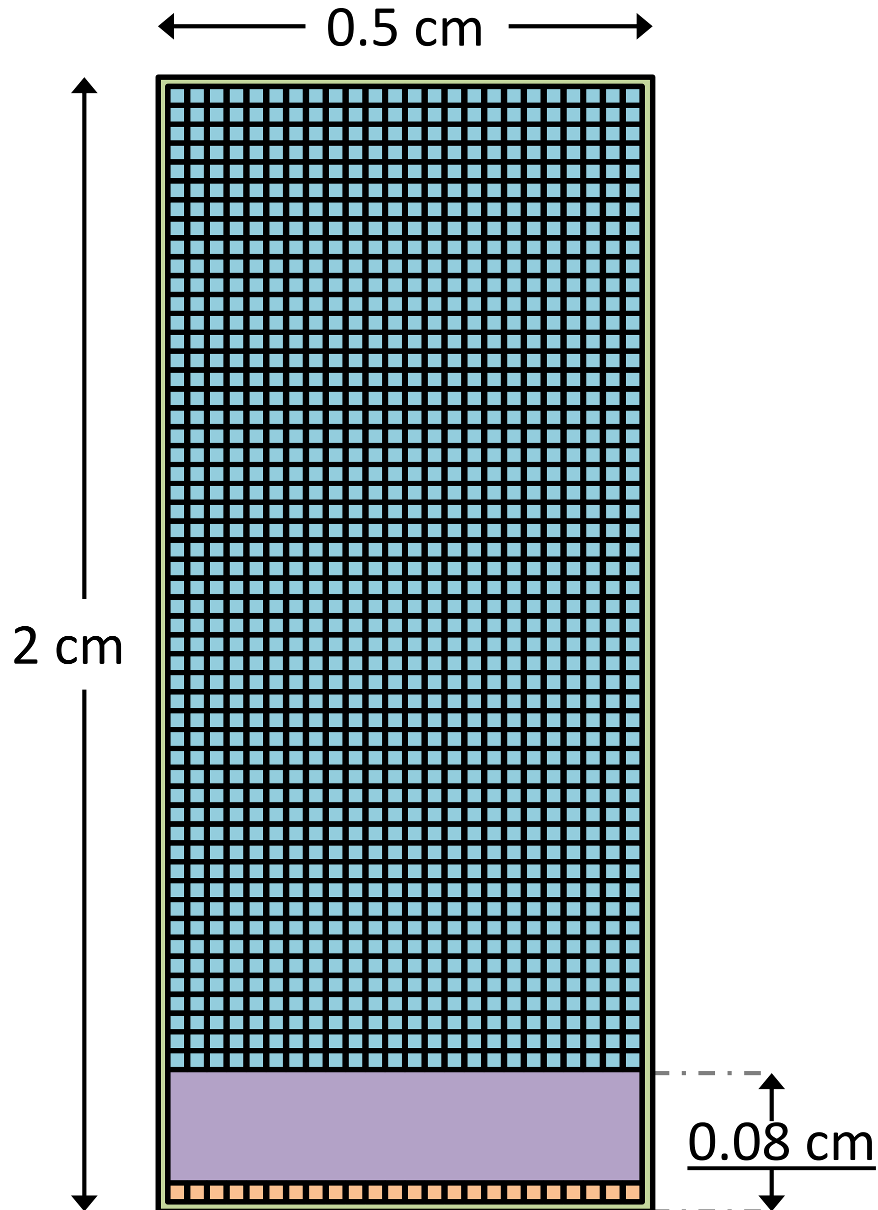


(a) Simulated hits across the pixel matrix.

(b) Missing hits across the pixel matrix.

Figure 7.3.6: (a) At a hit rate of 40 MHz cm^{-2} the simulated hits are evenly distributed across the pixel matrix *(heat map)* for the simulations with the improved readout mechanism for MightyPix2. The hits are evenly distributed across the columns *(histogram above)* and rows *(histogram beside the heat map)*. (b) The missing hits are evenly distributed across the columns but nearly all of them occurred in the top quarter rows.

RadPix1 draft floorplan



- **RadPix contents (assumptions)**
  - Chip ring (width 100 µm)
  - Pixel matrix
    - 100 µm × 100 µm pixels
    - 192 rows × 198/4 columns
    - Total of 9,504 pixels
  - Digital periphery
  - I/O pads
- **Fill-factor requirement**
  - Dead area <5%
- **A bit of maths**
  - Sensitive area = # pixels × pixel area
  - Sensitive area = 0.9504 cm^2
  - Dead area = 100 × [1 – (sens. area/total area] = **4.96%**

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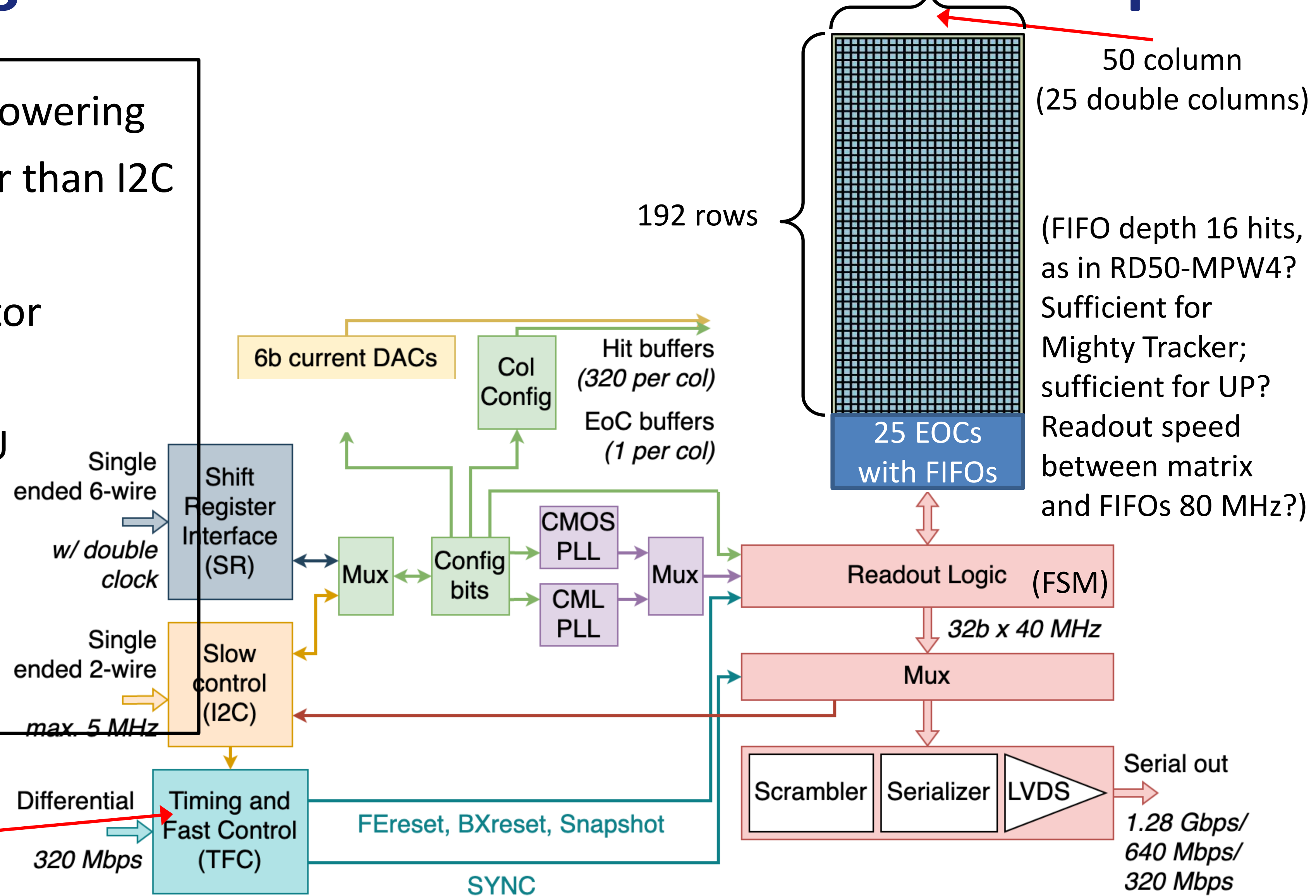
RadPix1 block diagram – What do we include in the chip?

- Voltage regulation for serial powering
- Differential slow control faster than I2C
- Command decoder
- Daisy chain and data aggregator
- Options for multiplexing links
- Triple redundancy against SEU
- HV switch (?)
- Temperature sensor (copy structure from MuPix?)
- Other things I have missed

- Ask VELO group for Verilog?



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RadPix submission plan

- **RadPix1 (0.5 cm × 2 cm):**
  - Submission spring 2025
  - Delivery of fabricated samples November 2025
- **RadPix2 (2 cm × 2 cm):**
  - Submission …
  - Delivery of fabricated samples …

RadPix submission plan

- **MLM3 (potentially):**
  - Maximum MLM 1×3 area is 25 mm x 9 mm
  - Submission date spring 2025

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Back up slides

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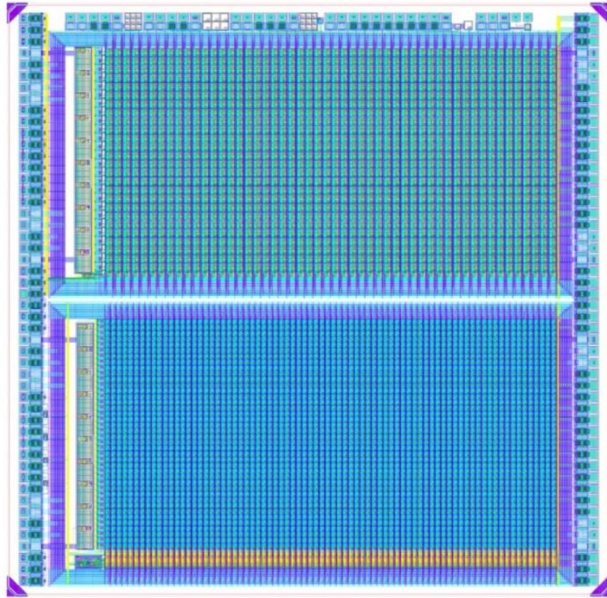
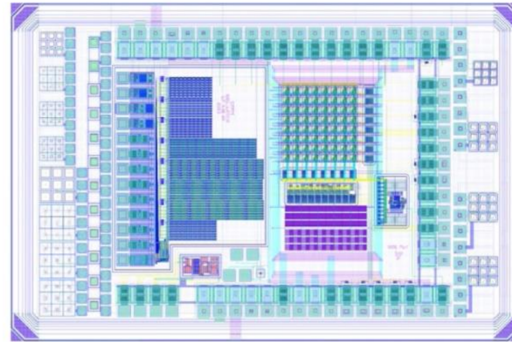
RD50-MPW chip series

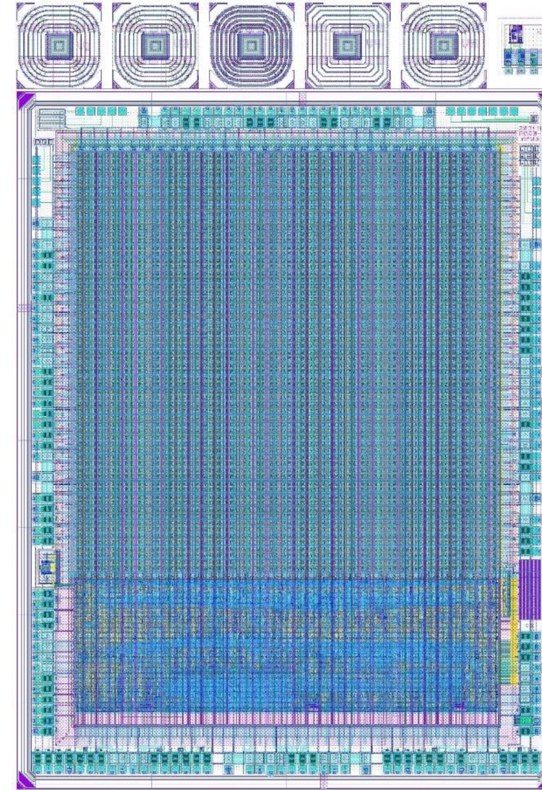
RD50-MPW1



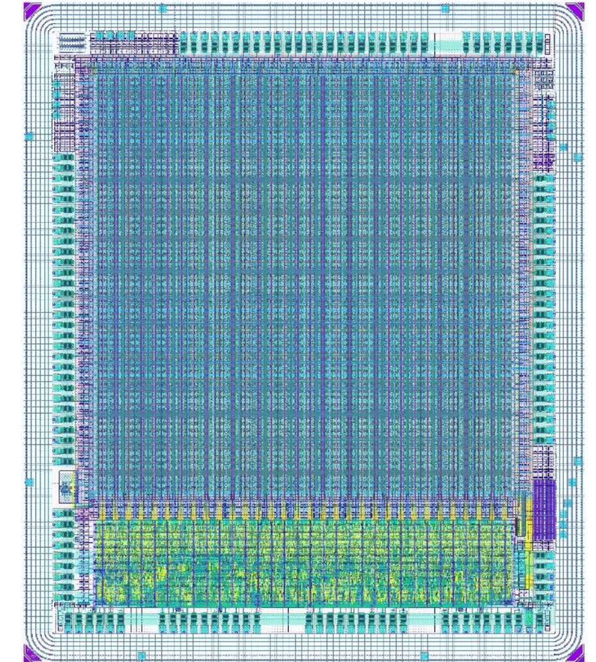
RD50-MPW2



RD50-MPW3



RD50-MPW4



RD50-MPWx chip series – Overview

- Are TX FIFOs really needed (in LHCb)?

Parameter	RD50-MPW1	RD50-MPW2	RD50-MPW3	RD50-MPW4
Device size [mm x mm]	5 x 5[(1)]	3.2 x 2.1	5.1 x 6.6	5.4 x 6.3
Pixel matrix size	40 x 78	8 x 8	64 x 64	64 x 64
Pixel size [µm x µm]	50 x 50	60 x 60	62 x 62	62 x 62
P-n spacing [µm]	3	8	8	8
In-pixel electronics	Analogue Digital	Analogue	Analogue Digital	Analogue Digital
Output data	Pixel address Time-stamp	Binary	Pixel address Time-stamp	Pixel address Time-stamp
Digital periphery	78 EOCs 2 LVDs lines	8 EOCs	32 EOCs, with 32-events 24-bit FIFOs 128-events 32-bit TX FIFOs I2C Wishbone bus 1 LVDs line	32 EOCs, with 16-events 24-bit FIFOs 64-events 32-bit TX FIFOs I2C Wishbone bus 1 LVDs line

(1)Half of the chip has a pixel matrix for applications beyond physics

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RD50-MPWx chip series – Overview

Parameter	RD50-MPW1	RD50-MPW2	RD50-MPW3	RD50-MPW4
Chip guard ring frame	None	1 n-ring 6 p-rings	1 n-ring 6 p-rings	1 n-ring 5 n-/p-rings
Substrate biasing	Through p-stop contacts	Through p-stop contacts	Through p-stop contacts	Through chip edge or backside
Substrate resistivity [kΩ·cm]	0.5 – 1.1 1.9	Standard 0.2 – 0.5 1.9 3	Standard 1.9 3	Standard 3
Device thickness [μm]	280	280	280	280
V_{BD} [V]	56	120	120	500(2)
I_{LEAK} [μA/pixel]	1	1E-4	1E-6	1E-6(2)
Depletion depth [μm]	118	110	Not tested	Fully depleted(2)
ENC [mV]	50	2	< 140, > 50	50(2)
Efficiency [%]	Not tested	Not tested	> 98	> 99(2)

(2)Anticipated values for RD50-MPW4

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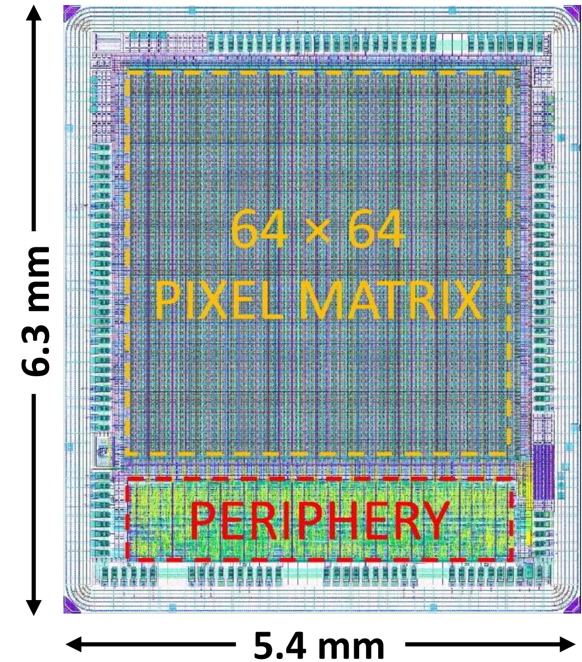
RD50-MPW4

- **Chip contents**
  - Matrix of depleted CMOS pixels with FE-I3 style readout
    - 64 x 64 pixels
    - 62 µm x 62 µm pixel area
    - Analogue and digital readout embedded in the sensing area
    - Double column scheme to alleviate routing congestion and minimise crosstalk
  - Digital periphery
    - 32 EOCs, with *16-events* 24-bit FIFOs
    - *64-events* 32-bit TX FIFOs
    - I2C protocol, Wishbone bus and one 640 MHz LVDS link
  - *Advanced chip rings*
  - Tests structures (e-TCT, DLTS)
- **Fabrication**
  - *Chip fabricated on 3 kΩ·cm wafers* (150 nm HV-CMOS LFoundry)
  - *One wafer with topside biasing only, two wafers allow backside biasing as well*



Delivered in January '24 (topside biased) and February '24 (backside biased)

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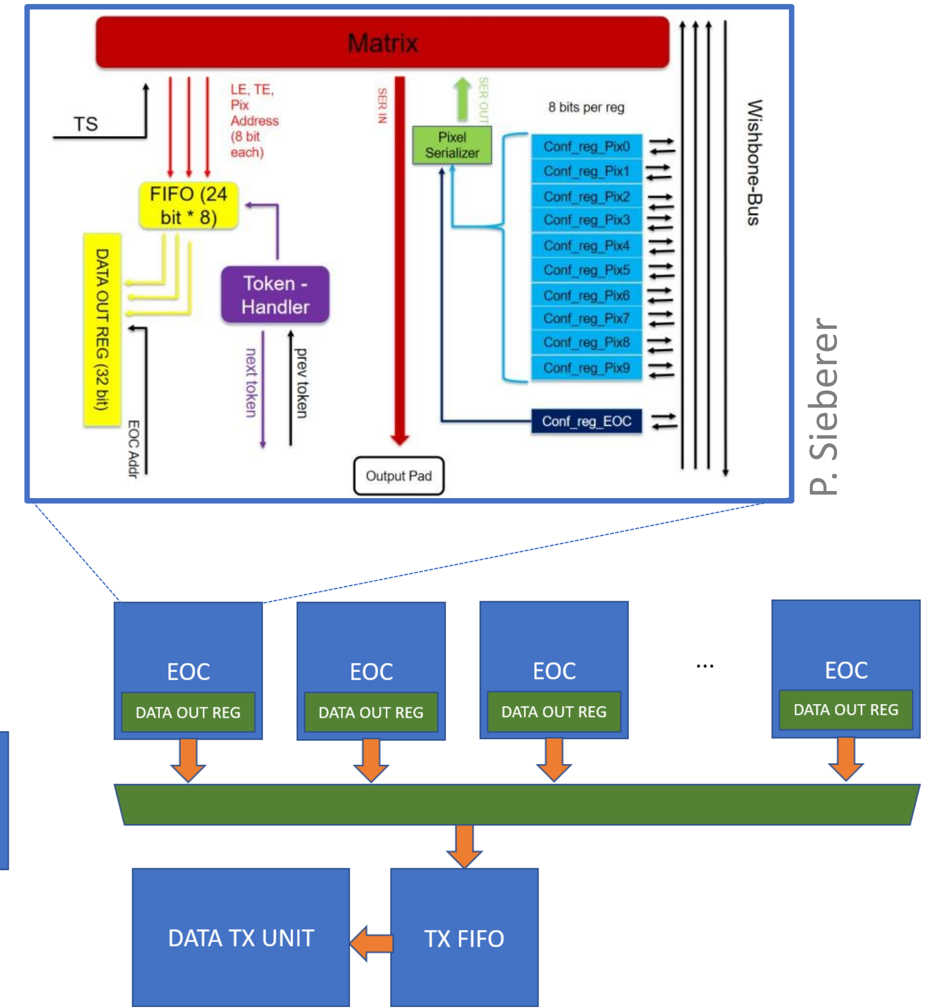
Digital periphery

- **End-Of-Column (EOC) architecture**
  - FIFO stores hit data (LE TS, TE TS and ADDR)
  - FSM reads double column
  - Token mechanism to determine which EOC is read out
- **Readout**
  - Pixel is read out immediately after hit (if FIFO is not full)
  - CU reads EOCs sequentially
  - Data stored temporarily in TX FIFO
  - Data TX unit with LVDS port @ 640 Mbps
- **Slow control**
  - Based on I2C protocol for external communication using internal Wishbone bus

CONTROL UNIT



R. Casanova, 38th RD50 WS

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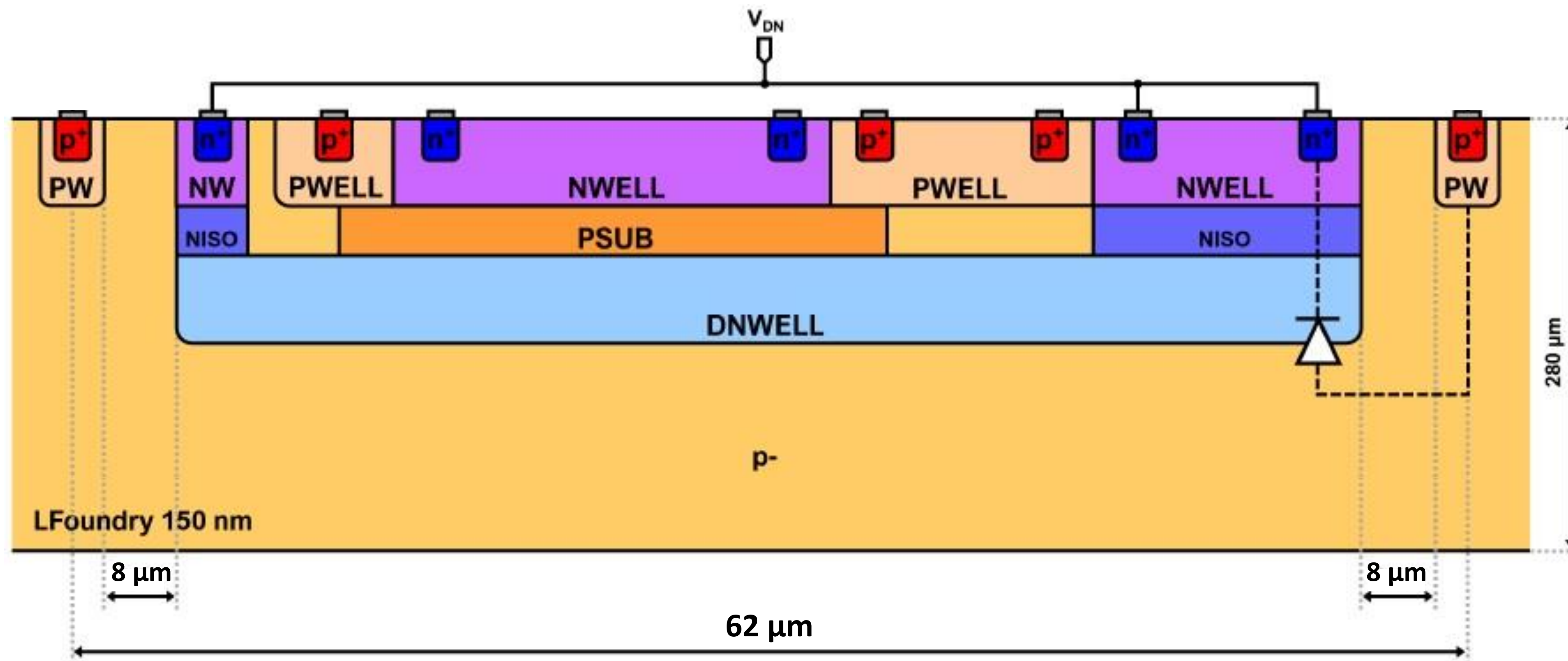
Process and sensor cross-section

- **150 nm HV-CMOS LFoundry**
  - P-substrate/DNWELL sensing junction
  - Pixel readout electronics embedded inside DNWELL
  - CMOS electronics in sensing diode & isolated from DNWELL with PSUB



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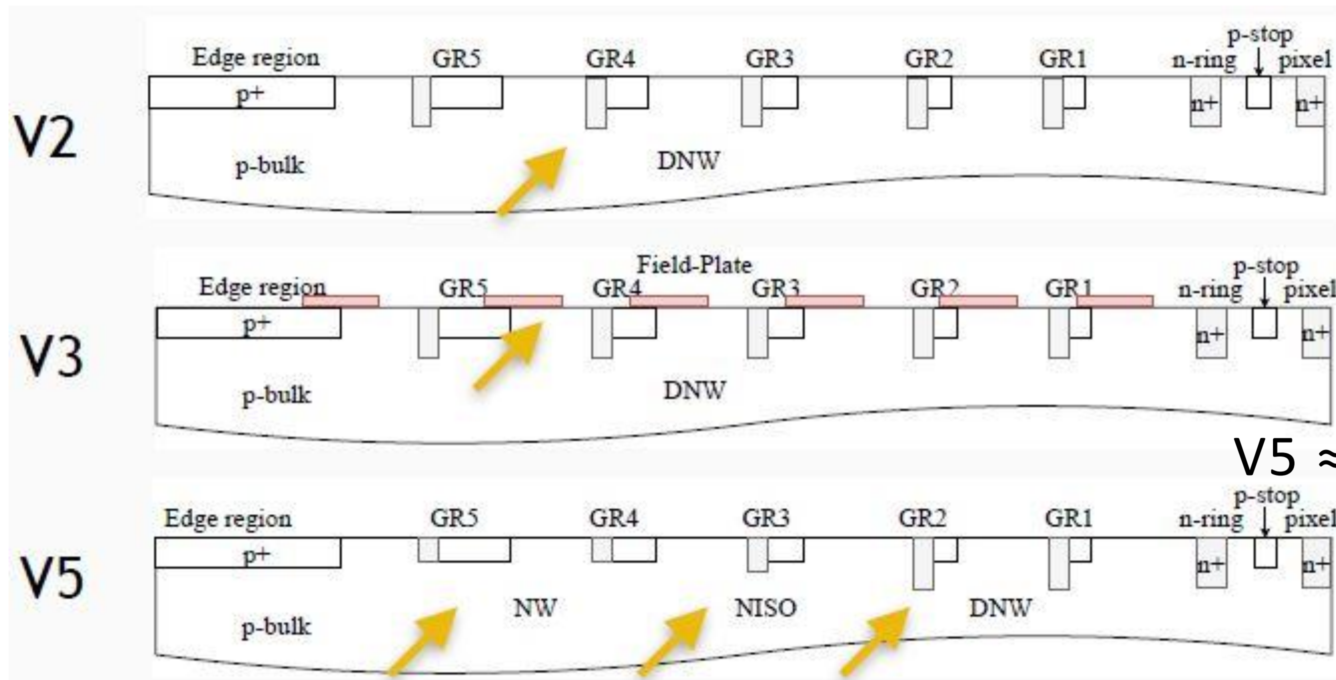
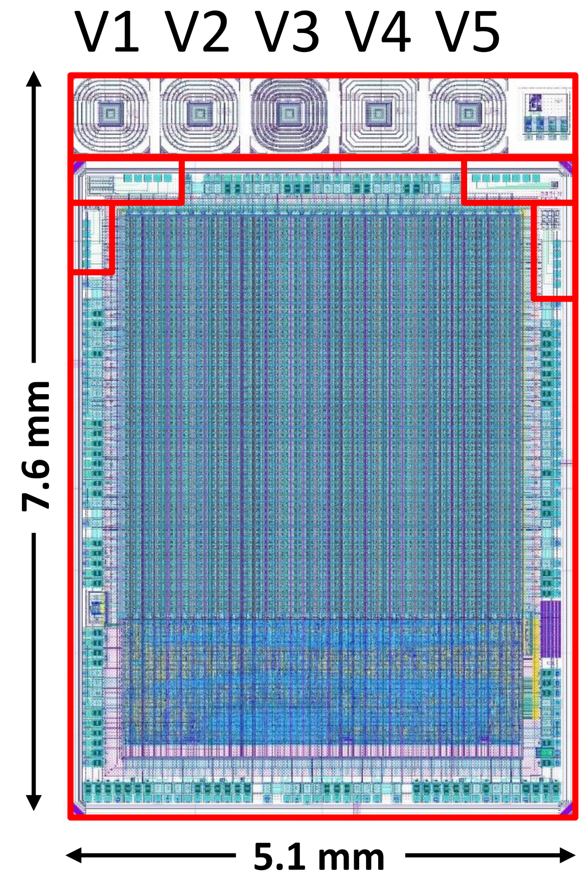
Towards RD50-MPW4 – Rings in RD50-MPW3

- **Guard ring types**
  - V1 old design: n+p GR, large space between n-ring and GR1
  - V2 based on V1: deep n-well replaces standard n-well at GR
  - V3 based on V2: large overhang
  - V4 based on V1: chamfer corner
  - V5 based on V1 & V2: reduced n-well depth from inner to outer GR





V5 ≈V2 > V3 ≈V1 > V4

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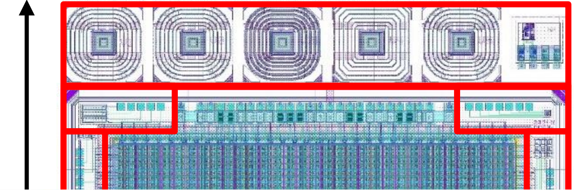
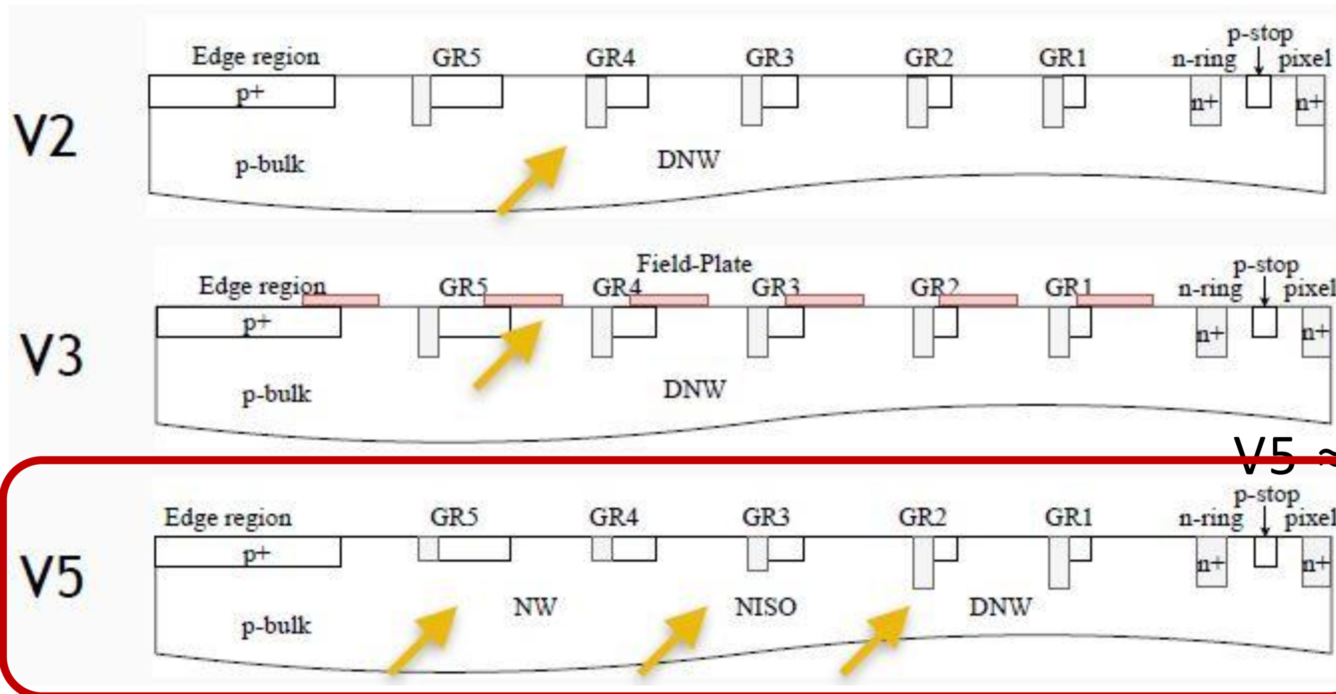
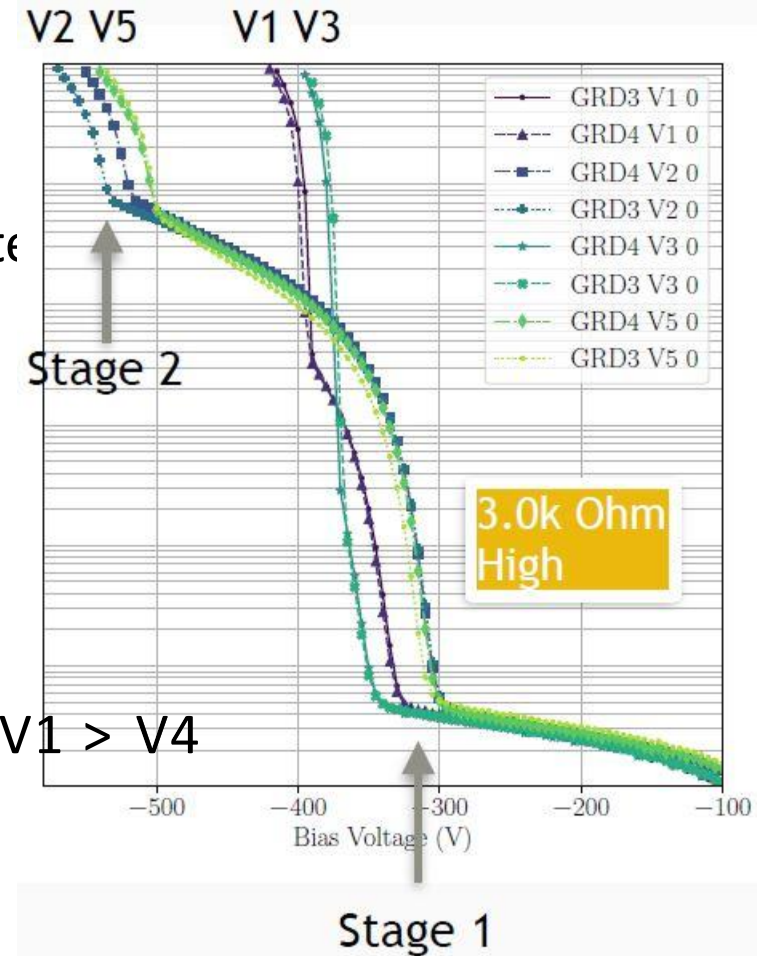
Towards RD50-MPW4 – Rings in RD50-MPW3

- **Guard ring types**
  - V1 old design: n+p GR, large space between n-ring and GR1
  - V2 based on V1: deep n-well replaces standard n-well at GR
  - V3 based on V2: large overhang
  - V4 based on V1: chamfer corner
  - V5 based on V1 & V2: reduced n-well depth from inner to oute

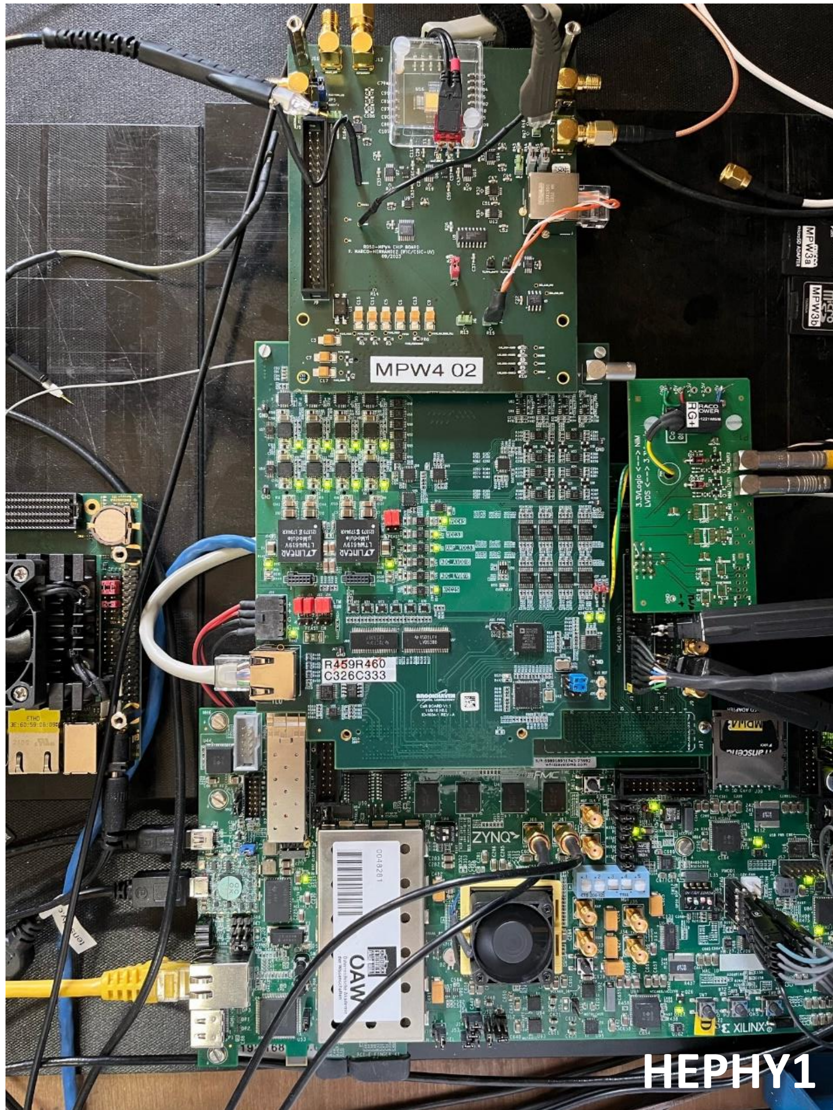


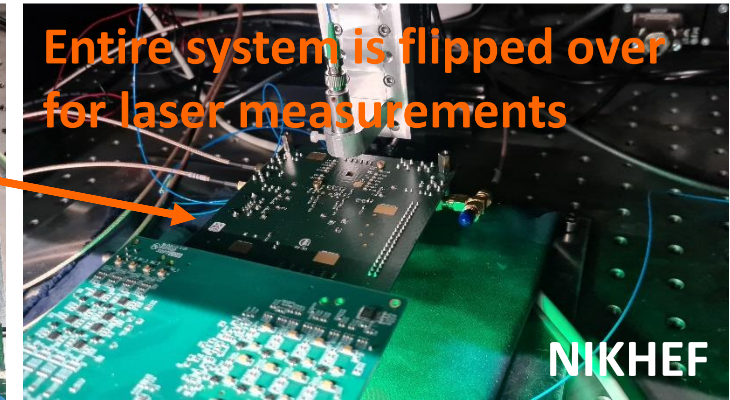




V5 ≈V2 > V3 ≈V1 > V4

RD50-MPW4 – DAQ based on Caribou



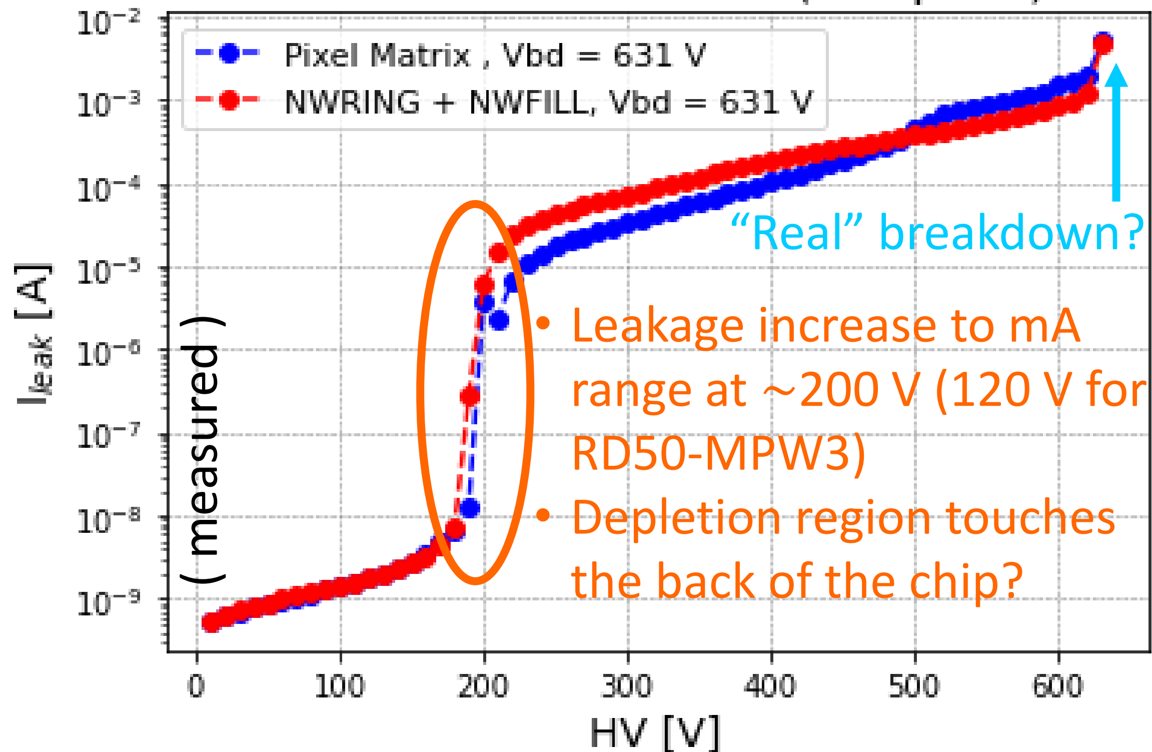


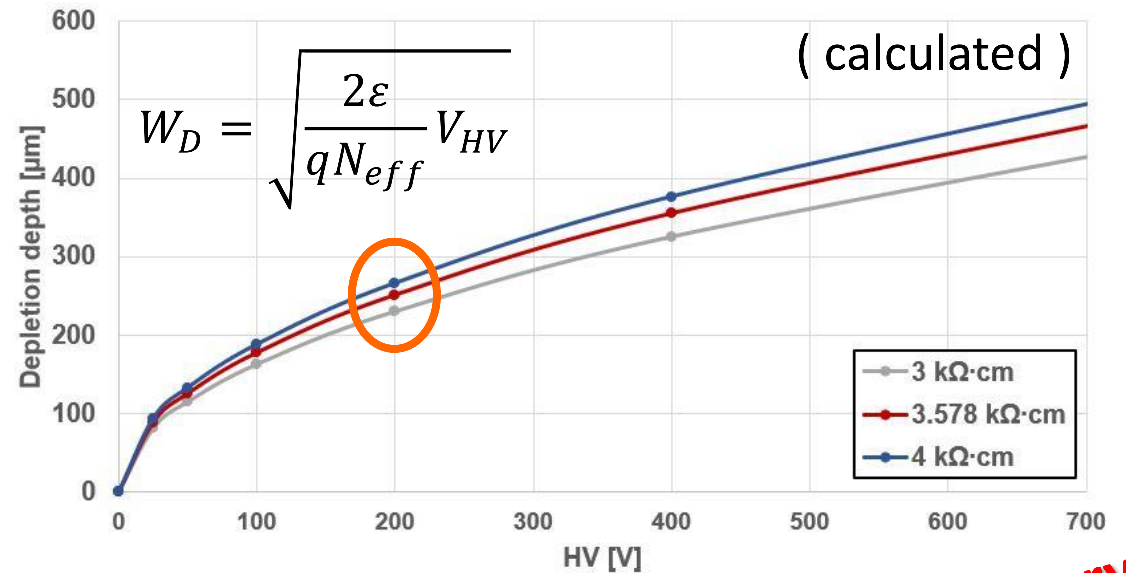
- **Xilinx Zynq-7000 SoC board**
  - ZC706 (ZC702 possible too)
- **Control and Readout (CaR) board**
  - Provides common services
- **Custom chip board**
  - Provides chip specific features

(and more sites currently getting ready)

RD50-MPW4 – I-V measurements, topside biased

- **First set of samples without backside processing were received first (W8)**
  - Substrate biased to high voltage from top side
  - Thinned to 280 µm
  - Probe station with needles, in darkness and at room T





Preliminary

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RD50-MPW4 – Evaluation plan

- **Laboratory measurements**
  - **I-V measurements**
    - Study V_BD, I_LEAK and their dependence with temperature
  - **Edge TCT measurements**
    - Study dependence of depletion depth with V_HV
  - **Active pixel matrix**
    - Identify optimised DAC settings for matrix bias block
    - Trade-off between pixel performance and power consumption
    - Pixels calibration and parameter extraction (gain, noise)
    - Charge collection efficiency
- **Test beam @ DESY in April (TB22)**
- **Irradiation campaign**
  - NIEL → N-fluence: 1E14, 3E14, 1E15, 3E15, 1E16, 3E16 n_{eq}/cm^2
  - TID → Evaluate pixel performance up to meaningful dose
- **Evaluate unirradiated and irradiated samples, topside and backside biased samples**

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