LHCb Upgrade II

Eva Vilella

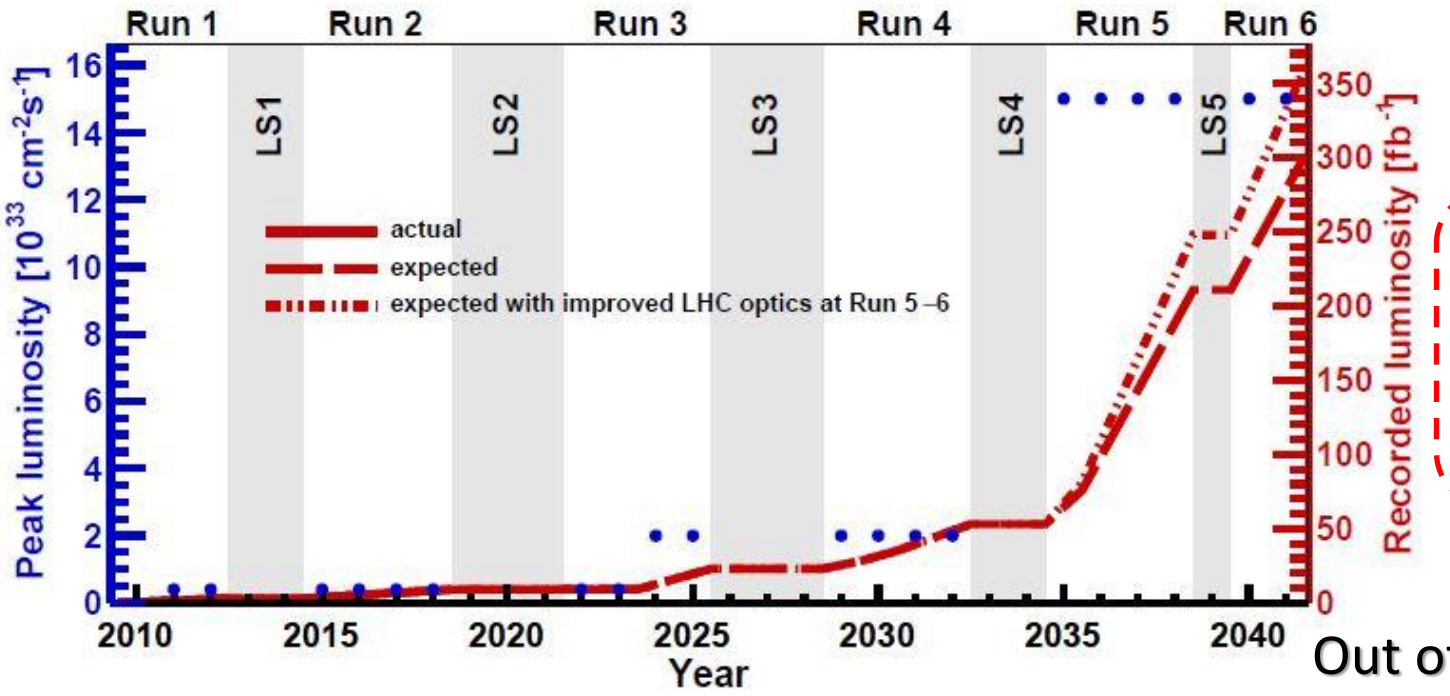
on behalf of Ashley, Ayushi, Chenfan, Karol, Kieran, Kurt, Sam, Tara

Important and recent reviews and workshop:

- Mighty-Tracker Pixel: Electronics architecture review, 4 Mar 2025, link
- MightyPix2 design review, 6 Mar 2025, link
- 5th Mighty-Tracker Workshop, 10-13 Mar 2025 @ CERN, link

LHC schedule

Instantaneous luminosity increase by ~ one order of magnitude compared to Upgrade I



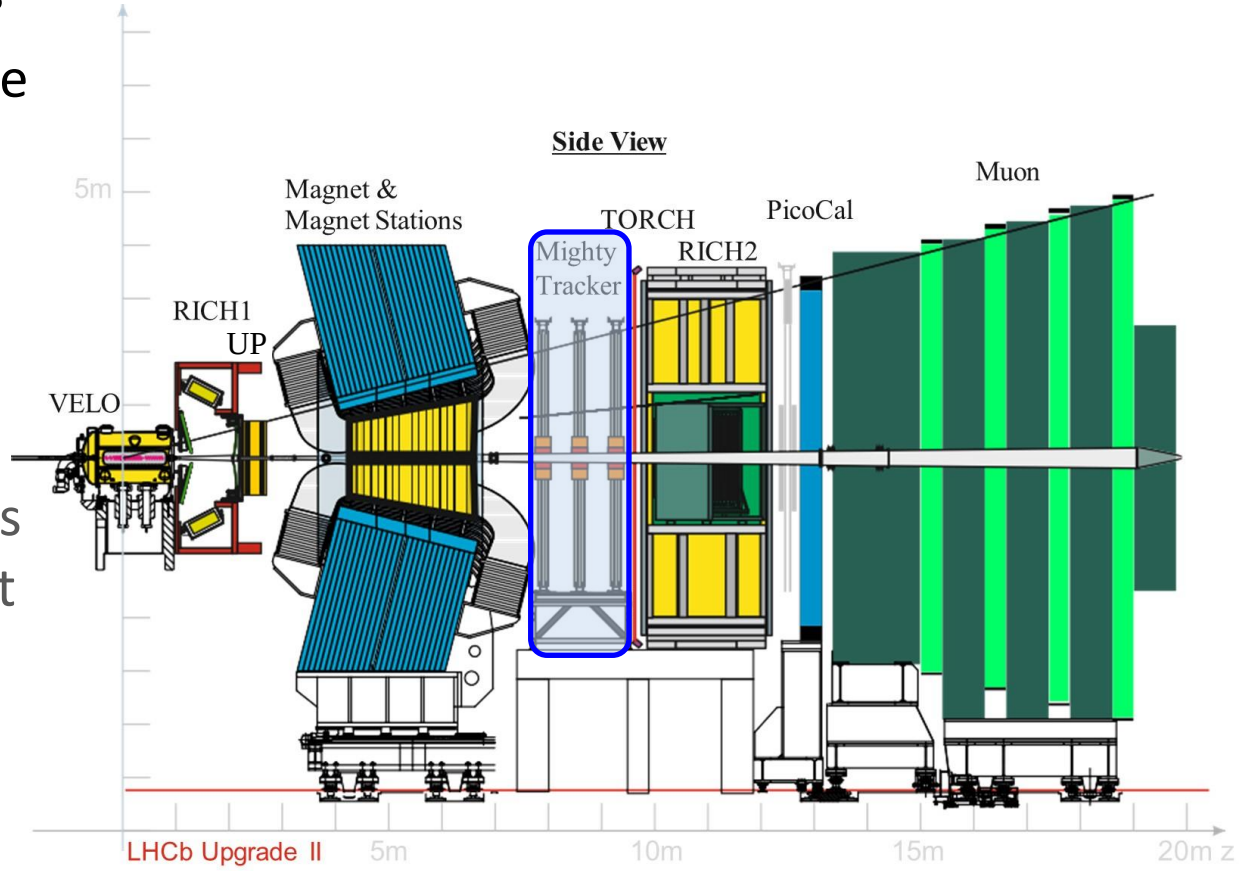
To accumulate a sample of 300 fb^{-1} of high energy pp collision data

Out of date!

- **Run 5 and Run 6** → Much increased instantaneous (peak) and integrated (recorded) luminosity
  - Unprecedented and unique discovery potential (precision searches for new physics in the flavour sector, direct searches for dark sector particles and QCD studies)
- To handle the much-increased particle flux and radiation level → **A second major upgrade is necessary** (detector technology with improved granularity and radiation tolerance)

LHCb Upgrade II

- Maximum peak luminosity of 1.5×10^{34} cm^{-2}s^{-1}
- Key features for successful physics programme
  - Efficient tracking of charged particles
  - Correct association of secondary heavy flavour decays to their primary vertices
  - Excellent particle ID
- Same footprint as existing spectrometer
  - Tracking system = VELO + tracking stations upstream and downstream of the magnet (UP + **Mighty-Tracker**)
  - PID system = RICH1 + RICH2 detectors upstream and downstream
  - Electromagnetic calorimeter (PicoCal)
  - Muon stations
  - Time-of-Flight detector (TORCH)

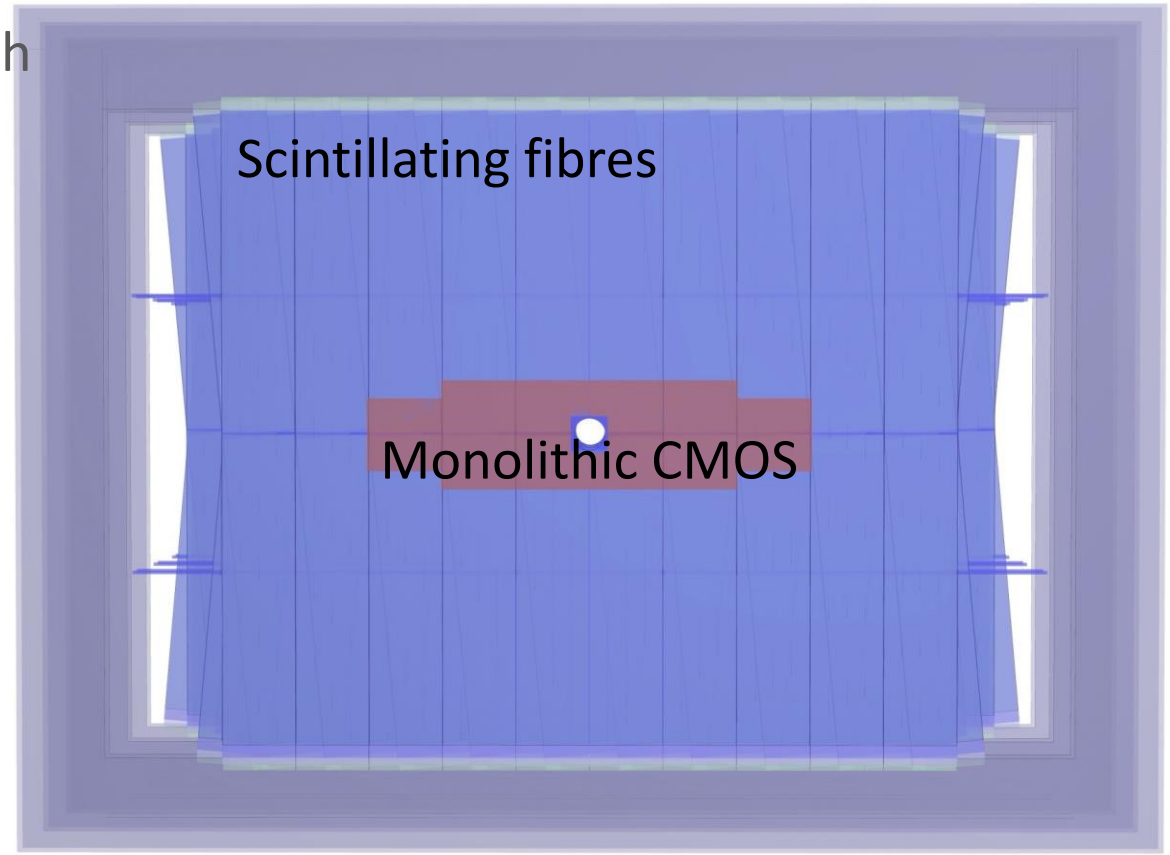


The LHCb Upgrade II (layout view)

Mighty-Tracker

- **New hybrid detector** for LHCb Upgrade II
  - To cope with high particle density and high radiation damage, and to minimise incorrect matching of upstream and downstream track segments
- **Mighty-Pixel: Inner Mighty Tracker region**
  - High granularity
  - High radiation tolerance

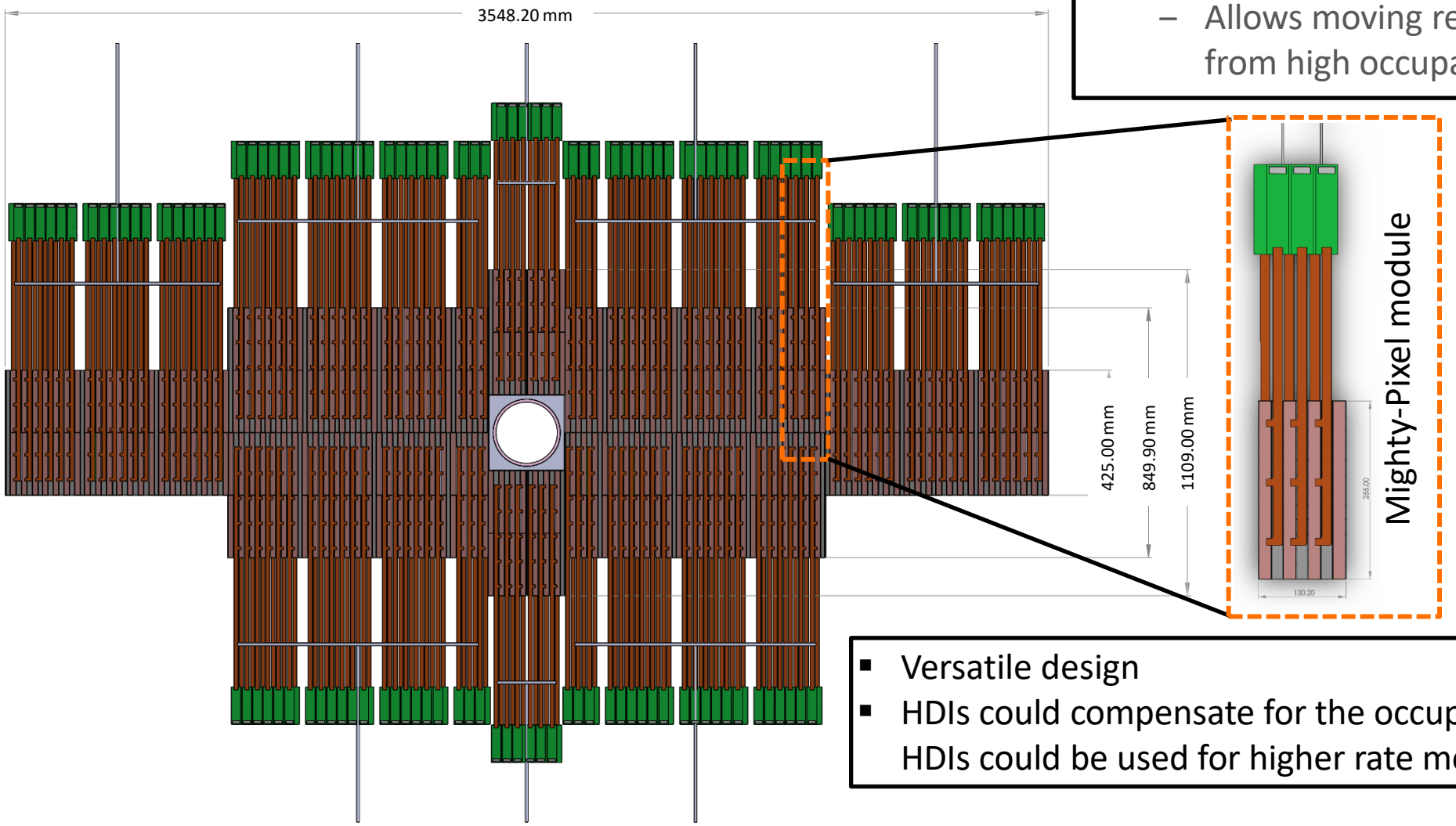
  → **Monolithic CMOS (~9 m²)**
- **Mighty-SciFi: Outer Mighty Tracker region**
  - **Scintillator fibres**, as in Run 3, but with significant improvements
- Installation at tracking stations T1 to T3 (six layers)



The Mighty Tracker – Scoping document baseline design (from Tai-Hua Lin)

Mighty-Pixel – Layer layout

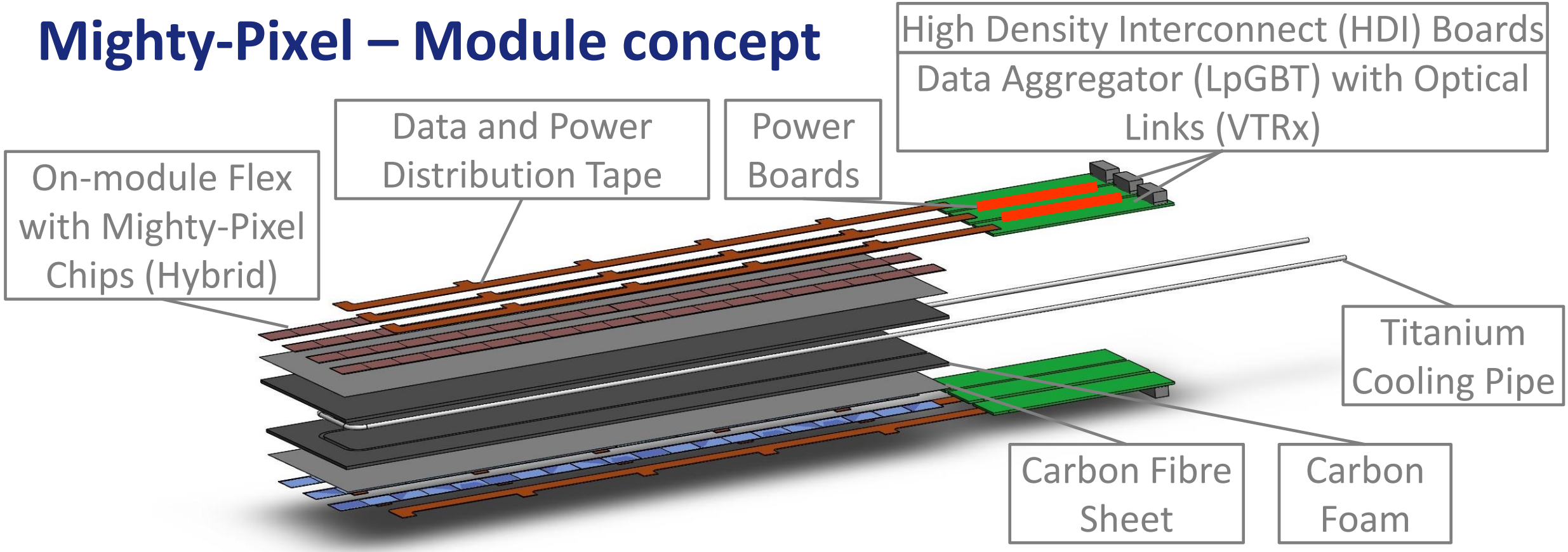
- Stave topology
  - Elongated support structure
  - Allows moving readout electronics away from high occupancy region



The pixels cover the hit rate region that the fibers cannot withstand

- Versatile design
- HDIs could compensate for the occupancy difference (more HDIs could be used for higher rate modules)

Mighty-Pixel – Module concept



- Double-sided staves, with Mighty-Pixel chips on the front and back, to avoid acceptance gaps
- **Hybrids:** Flex circuits with Mighty-Pixel chips attached
  - In thin build Cu-Polyimide technology, with controlled impedance for the many 1.28 Gbps data links
  - About 5,000 hybrids are needed (including yield)
- **Power boards:** For powering the HDI boards + optional HV switch for Mighty-Pixel chips
  - About 2,000 hybrids are needed

Chip specifications

Pixel sensor specifications for the LHCb Mighty-Pixel tracker and the Upstream tracker, S. Bachmann *et al.*, EDMS document 3207186 v.1.0

Mighty-Pixel

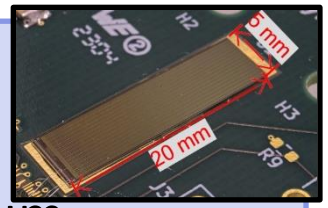
Parameter	MP Specification
Pixel size (bending plane)	$\leqq 100\,\mu m$
Pixel size (non bending plane)	$\leqq 200\,\mu m$
Substrate thickness	$<200\,\mu m$
Pixel orientation	x
Max. Particle Rate	$17\ MHz/cm^2$
Max. Hit Rate	$34\times10^6\ s^{-1}cm^{-2}$
Max. length of data word	32
Overall efficiency	>96%
In-time efficiency	>99% within 25 ns
Noise rate (End of life)	$\leq 400kHz/\,cm^2$
Transmission rate	4 links of 1.28Gbit/s each
NIEL	$3\times10^{14}n_{eq}/cm^2$
TID	40 MRad
Power Consumption	$\leq 150\ mW/\,cm^2$

→ unique BXID

+ compatibility with: back-end electronics, general LHCb readout architecture, Timing and Fast Control (TFC) and Experiment Control System (ECS) of the LHCb experiment.

MightyPix (180 nm)

MightyPix2 – Architecture and User Manual, R. Leys *et al.*, link



MightyPix1

- Chip size: 0.5 cm × 2 cm
- Pixel size: 165 µm × 50 µm
- 2 × 32-bit hit data words
  - Pixel address
  - Time-of-Arrival (ToA)
  - Time-over-Threshold (ToT)
  - Time-to-Digital Converter (TDC)
- Periphery
  - 1 data link (max. 1.28 Gbit/s)
  - Slow control (I2C protocol)
  - Timing and Fast Control (TFC)
  - lpGBT frame compatible

MightyPix2

- Chip size: 2 cm × 1.66 cm (TBC, aim for large size)
- Pixel size: 84 µm × 84 µm (identical to P2Pix)
- 2 output modes
  - Long: 41-bit hit data word
  - Short: 30-bit hit data word (high-rate mode, 4 data links with 5-bit column address)
- Periphery
  - 4 data links (max. 1.28 Gbit/s)
  - Slow control (serial powering & ECS compatible)
  - Timing and Fast Control (TFC)
  - Gearbox + asynchronous FIFO for improved rate
  - Serial powering, temperature diode

MightyPix3

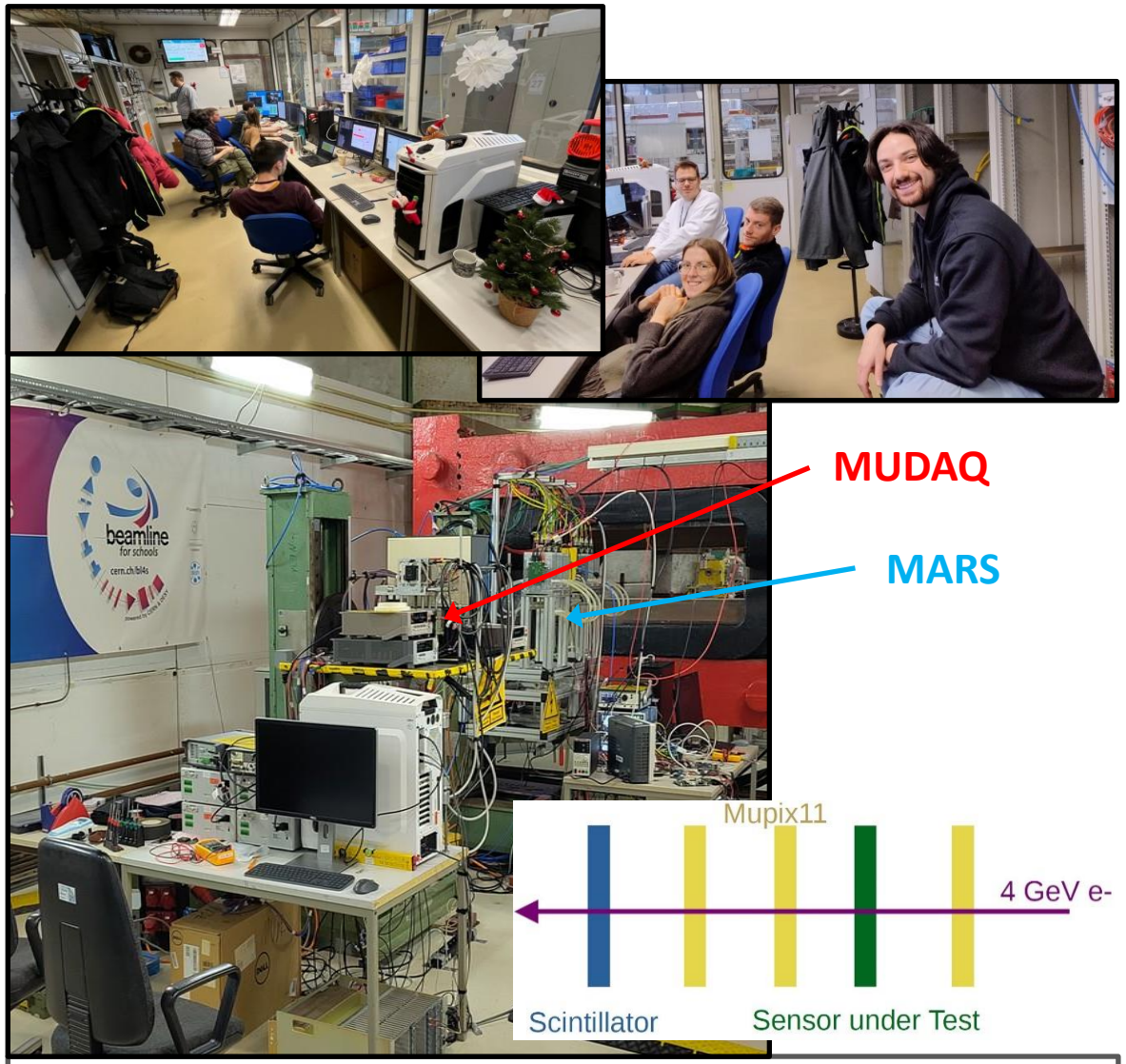
2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028

MightyPix test beam

- **Goal:** Validate radiation tolerance of 180 nm HV-CMOS technology for the Mighty-Tracker
- MightyPix1 is not suitable for an irradiation campaign
  - Unstable configuration due to design bug
- Use TelePix2 as a proxy for performance measurements

	MightyPix1	TelePix2
Size [cm × cm]	0.5 × 2	2 × 1
Pixel size [µm × µm]	165 × 50	165 × 25
Breakdown [V]	–210	–150
Amplifier	CMOS	CMOS
Comparator	CMOS	CMOS

- Two weeks of DESY test beam in December 2024
  - 4 GeV electrons
  - Hit rate: 30 – 40 kHz/(2 cm × 2 cm)

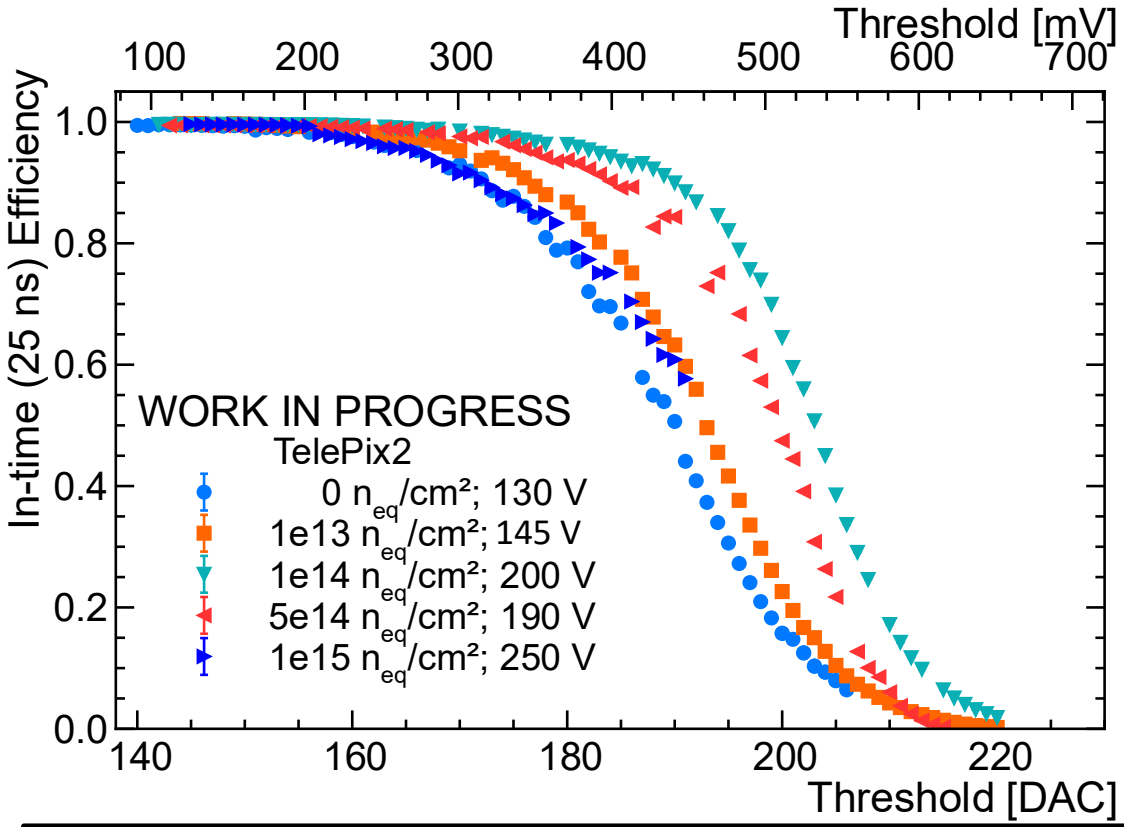


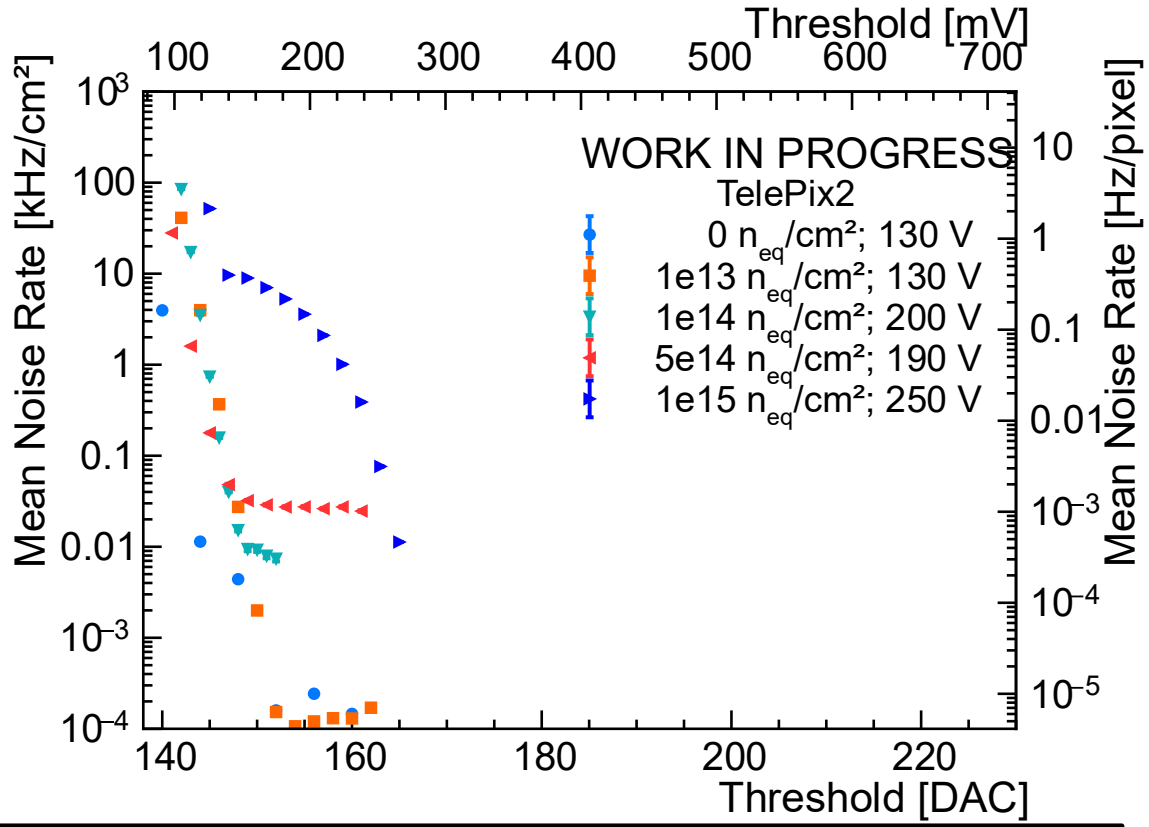
TelePix2: Full scale fast region of interest trigger and timing for the EUDET-style telescopes at the DESY II Test Beam Facility, L. Huth *et al.*, arXiv:2503.08177

In-time efficiency at high HV

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

Source: Lucas Dittmann

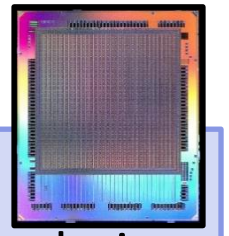




- No timing correction or threshold tuning required
- For all fluence ➔ Noise rate < 400 kHz/cm^2 & In-time efficiency > 99%
- Even for 1 × 10^{15} n$_{eq}$/cm^2 all fluence ➔ Time resolution < 2.4 ns

TelePix2 has
120 × 400 pixels

RadPix (150 nm)



RadPix status and design plans, C. Zhang *et al.*, 5th Mighty Tracker Workshop

RD50-MPW4

- R&D prototype to push boundaries of HV-CMOS technology
- 10^{15} n_{eq}/cm^2 radiation tolerance (tested); further tests in 2025 with samples irradiated to higher fluence (10^{16} n_{eq}/cm^2)

Enhancing Radiation Hardness and Granularity in HV-CMOS: The RD50-MPW4 Sensor, B. Pilsl *et al.*, VCI2025

RD50-MPW4: A thin backside-biased HV-CMOS pixel chip, E. Vilella *et al.*, JINST

RadPix1

- Chip size: 0.5 cm × 2 cm (TBC)
- Pixel size: 80 µm × 80 µm
  - Power consumption optimisation (< 9.6 µW/pixel to meet 150 mW/cm² requirement, with 99% in-time efficiency)
- 1 × 35-bit hit data word (in progress)
- Periphery
  - 1 data link (max. 1.28 Gbit/s)
  - Slow control (I2C protocol for convenience)
  - Timing and Fast Control (TFC)
  - Gearbox
  - Serial powering, Power-on-Reset

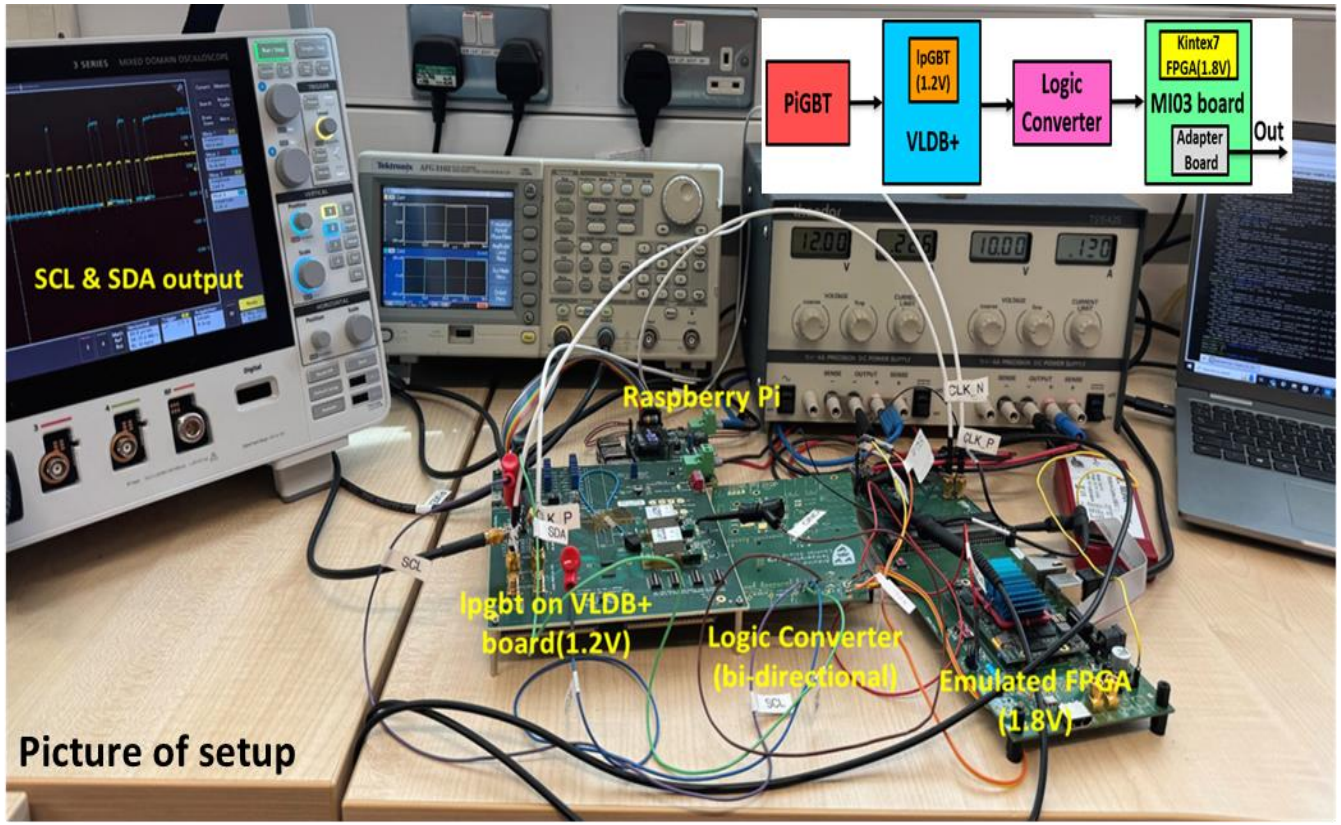
See Chenfan's talk for RadPix design work

RadPix2

2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028

FPGA emulation

- **Idea:** To use an FPGA to emulate digital features of the chip using a Kintex 7 Mercury FPGA.

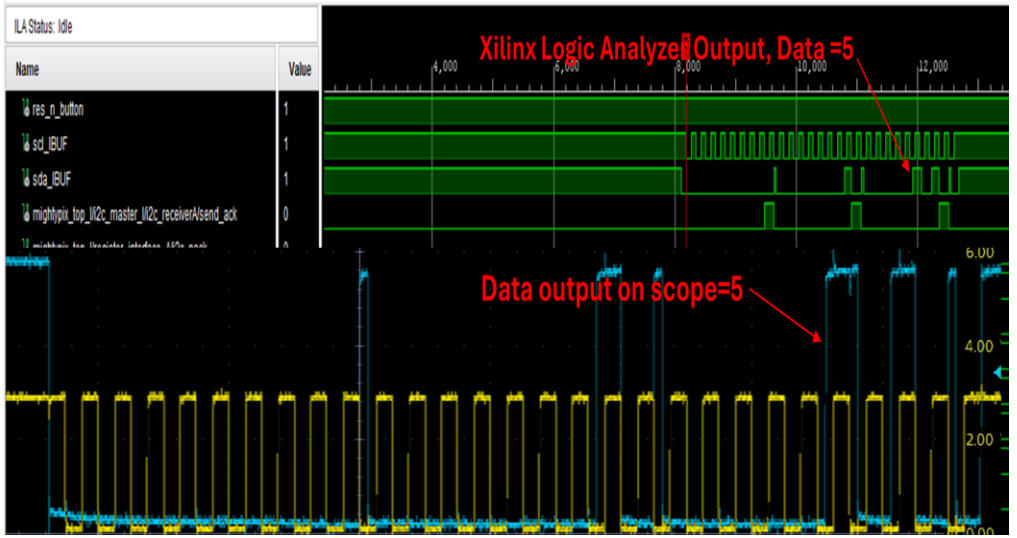


- ✓ To ***verify behavior of the chip*** in LHCb environment with LHCb protocols via lpGBT (low power gigabit transceiver) using VLDB board.
- ✓ To ***initiate the communication*** between lpGBT and chip emulator over I2C for sending and receiving data.
- ✓ To ***configure the emulated chip*** using I2C interface.

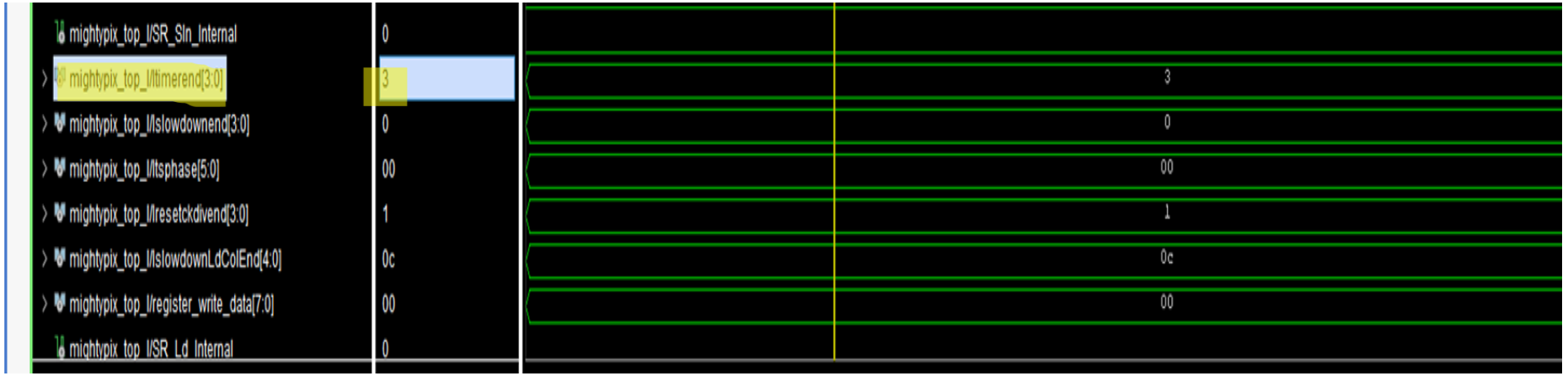
- A 40 MHz clock provided by the lpGBT as an input clock to the FPGA chip emulator.
- Logic converter added for voltage compatibility between FPGA and lpGBT.

FPGA emulation

- Successfully managed to talk to FPGA emulator over I2C and read back data from internal registers.
- Successfully transferred digital config bits from lpGBT to set the internal shift registers to configure the chip.
- Developing the setup with MightyPix design and will extend it for RadPix design.

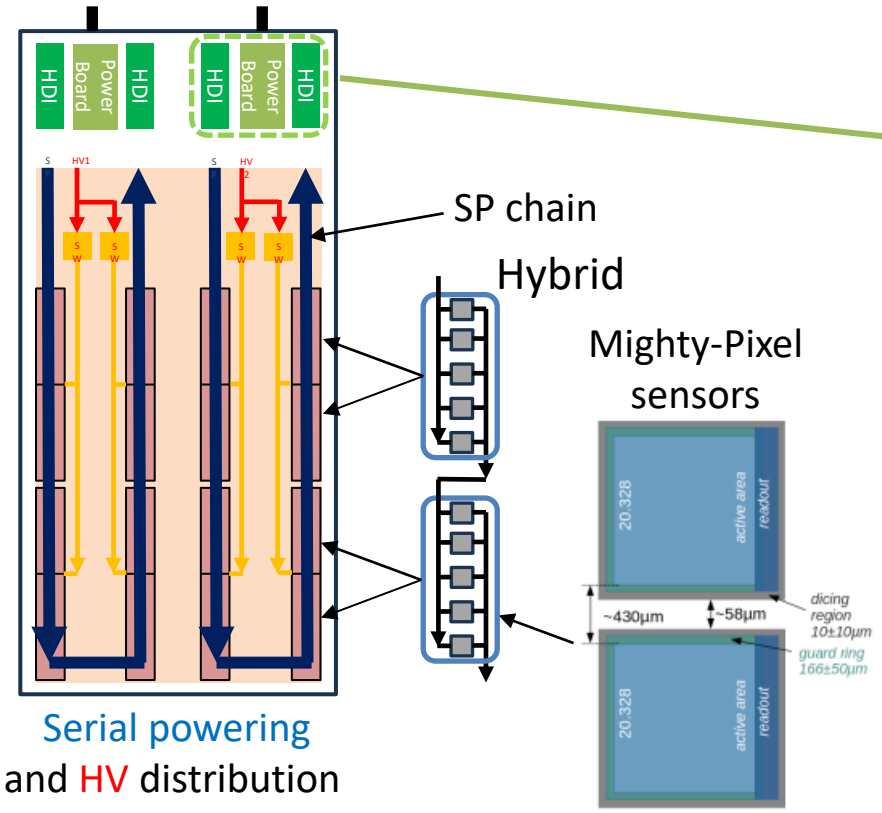


Communication from lpGBT to Mighty-FPGA.

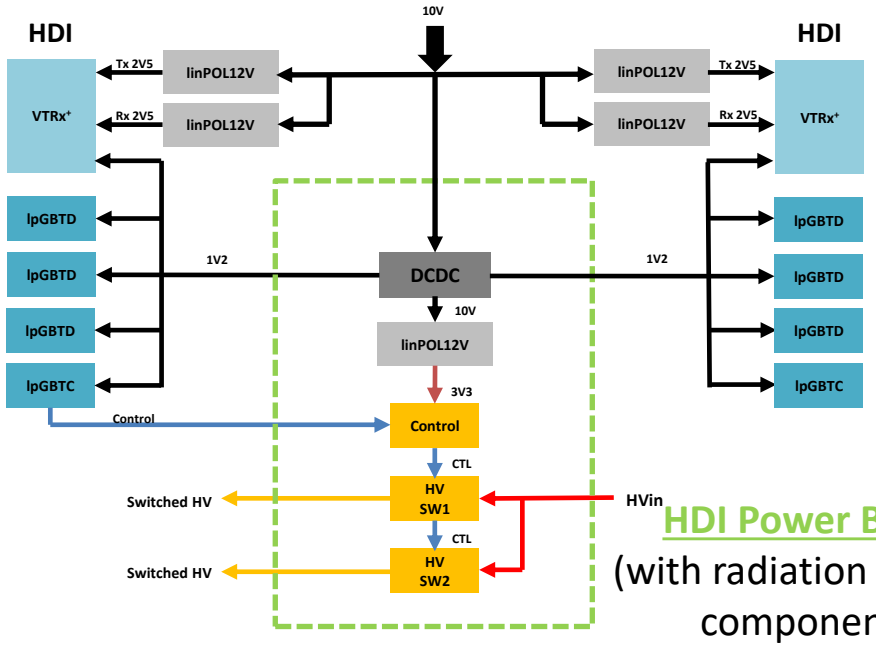


Setting the shift registers to configure the digital part of the emulated sensor chip.

Module: Serial powering chain and HV distribution



Serial powering and HV distribution across hybrids



HDI Power Board (with radiation tolerant components)

- Hybrids come loaded with 5 Mighty-Pixel chips
  - Precision mounted with ~60 µm gap between sensors

- Buck DCDC converter and linear voltage regulators
  - CERN bPOL12V and linPOL12V devices
- GaNFET devices used as SW controllable HV switches
  - Providing segmentation of HV on a hybrid
  - And failure protection from anomalous sensors

Mighty-Tracker organisation

WP1 Simulation and performance
Lucia Grillo (Glasgow), Christoph (HD), Matt Needham (Edinburgh)

WP2 Fibres
Guido Haefeli (Lausanne)
Thomas Kirn (Aachen)

WP2.1 Fibres
WP2.2 SiPM
Esteban Curras (Lausanne)
WP2.3 SiPM Cooling and coldbox
Joanna Liberadzka-Porret (Lausanne)
Thorsten Siedenburg (Aachen)
WP2.4 ASIC
Albert Comerma (Barcelone)
WP2.5 Electronics, controls and monitoring
Ulisses Carneiro (Rio)

WP3 Pixels
Eva Vilella (Liverpool)
Klaas Padeken (Bonn)

WP3.1 MightyPix chip
Eva Vilella (Liverpool)
Toko Hirono (KIT),
WP3.2 Evaluation of the MightyPix chip
Atanu Modak (RAL)
Sebastian Bachmann (Heidelberg)
WP3.3 Electronics, controls and monitoring
Dirk Wiedner (Dortmund)
Mike Perry (Manchester)
WP3.4 MightyPix modules
Oscar Augusto De Aguiar Francisco (Manchester)

WP4 Back-end Readout
Dirk Wiedner (Dortmund)
Karol Hennessy (Liverpool)

WP5 Mechanics, integration and services
Michael McCann (Imperial)

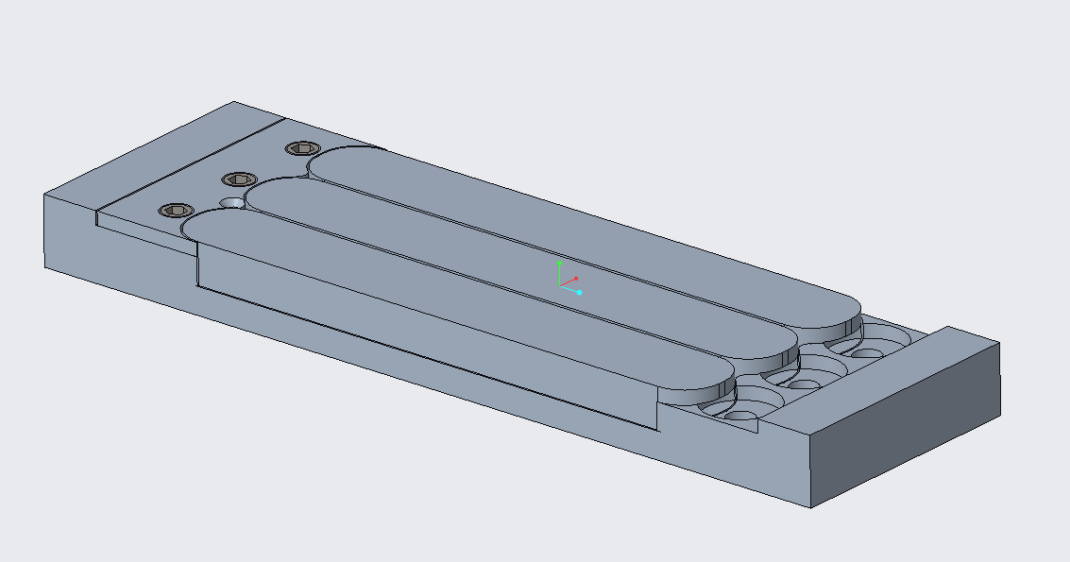
WP5.1 Modules for Fibre and Pixels enclosure
Trevor Savidge (Imperial)
WP5.2 Global mechanics design
Blake Leverington (Heidelberg)
WP5.3 Services
Alexander Bitadze (Manchester)
WP5.4 Safety and DSS system

Project Engineers WP3 – WP5
Alexander Bitadze (Manchester)

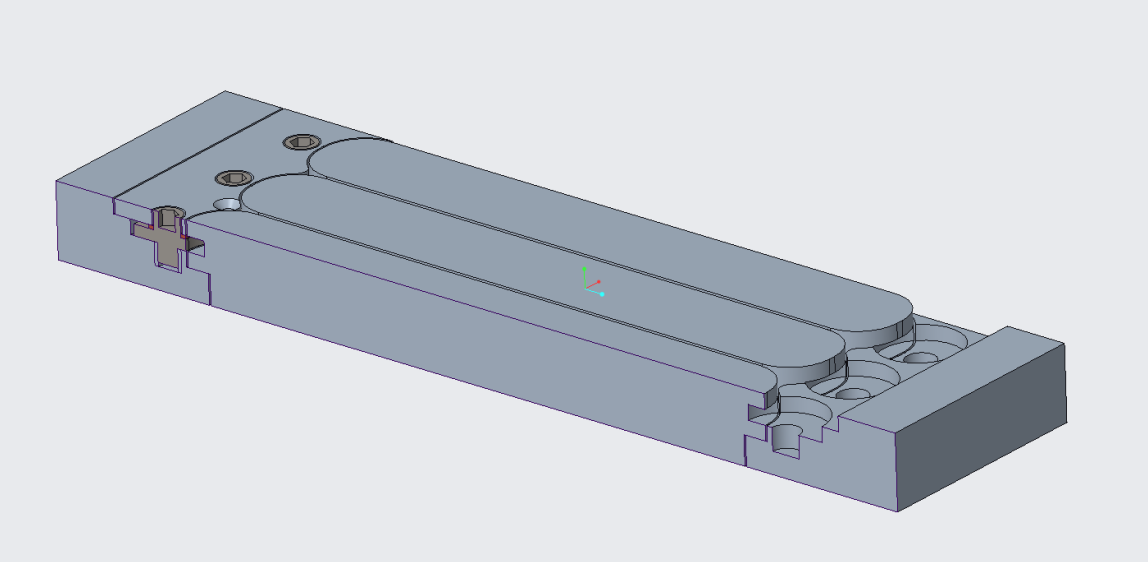
Project Engineers WP2 – WP5
?

VELO U2 mechanics

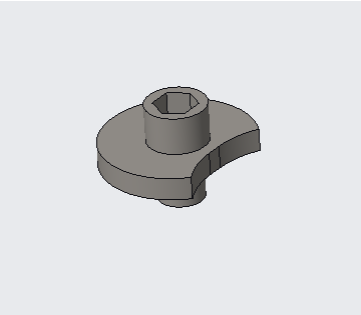
- CAD concept for a replaceable module on a cassette



Slotted module design with locking cam



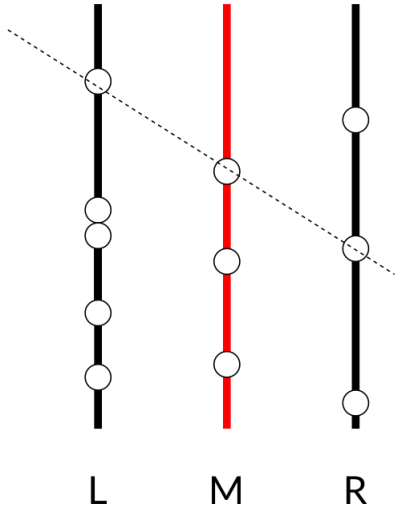
Cross-section



Cam with cutout to accommodate module foot (it's missing the taper that compresses the seal)

ML Track Seeding on FPGA's with Intel OneAPI

- Implement a detector-agnostic ML/NN track seeding algorithm on FPGA, using the LHCb VELO as an example.
- Target FPGA with Intel/OneAPI as development framework:
  - allows to code in a high level language (C++)
  - opens up FPGA targets to non-RTL experts
- Correctness & good performance of NN triplet classifier achieved: efficiency 92%, purity 97%
- However, data routing not optimal with pure C++ builds.
- Switched to also supported mixture of C++ and RTL, resulting in better timings and resource usage.
- Need to add RTL-based I/O components to properly measure throughput.



Find the right combination of three clusters

Altera Agilex 7F-series AGF027 FPGA

See Paras' talk for Eduardo's work on Analysis Facility (U2)

One last thing

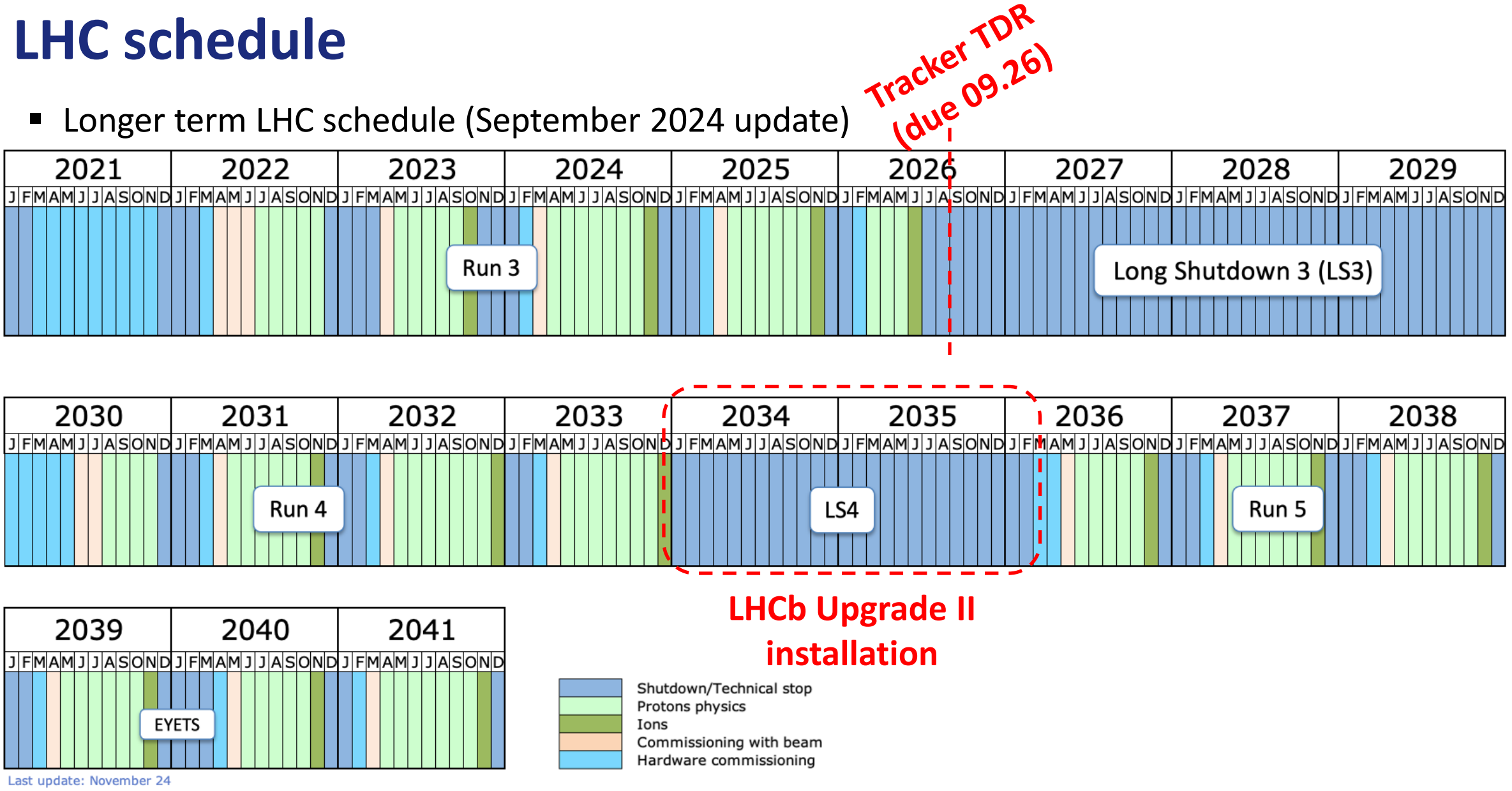
- Currently we are preparing the bid for the next phase of U2 funding –Eva Mighty-Tracker WP lead within LHCb-UK and LHCb U2 PI at Liverpool.

Thanks for listening!

Back up slides

LHC schedule

- Longer term LHC schedule (September 2024 update)

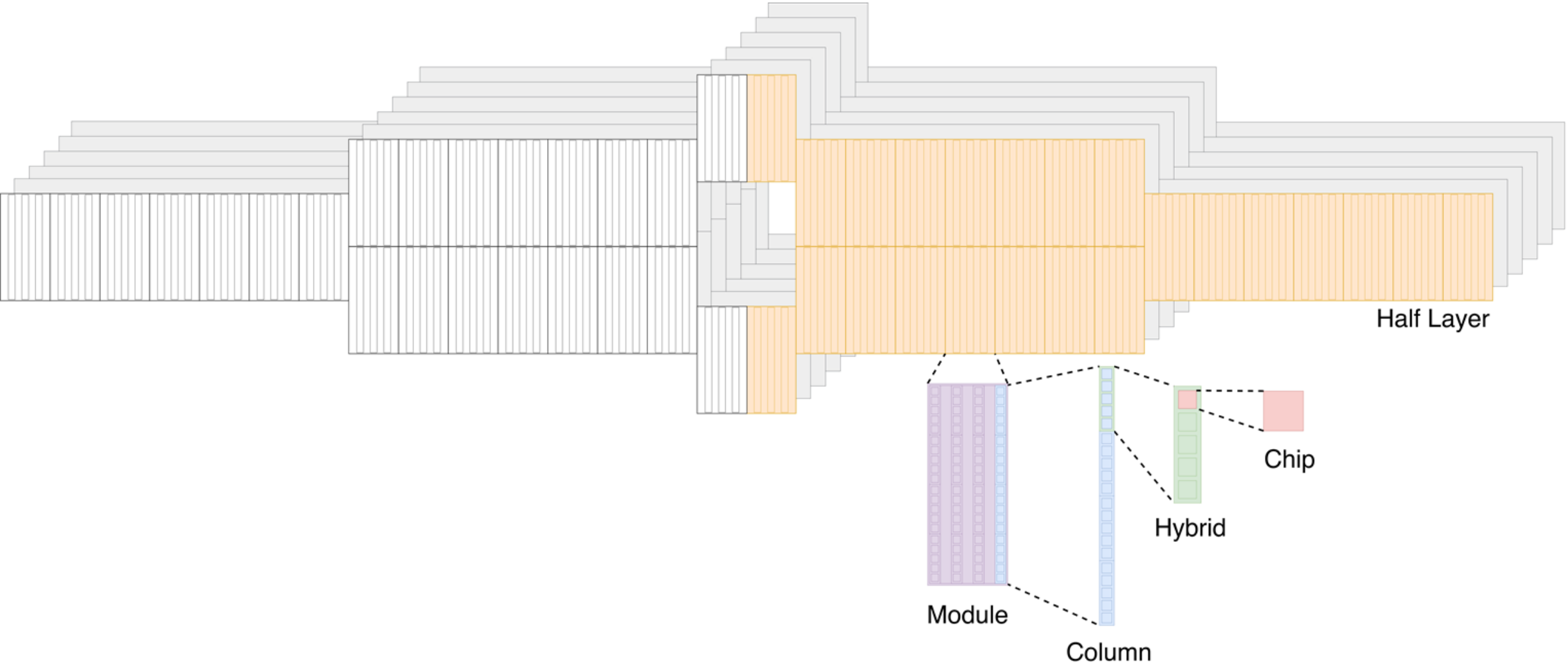


Mighty-Tracker milestones towards the TDR

Preliminary

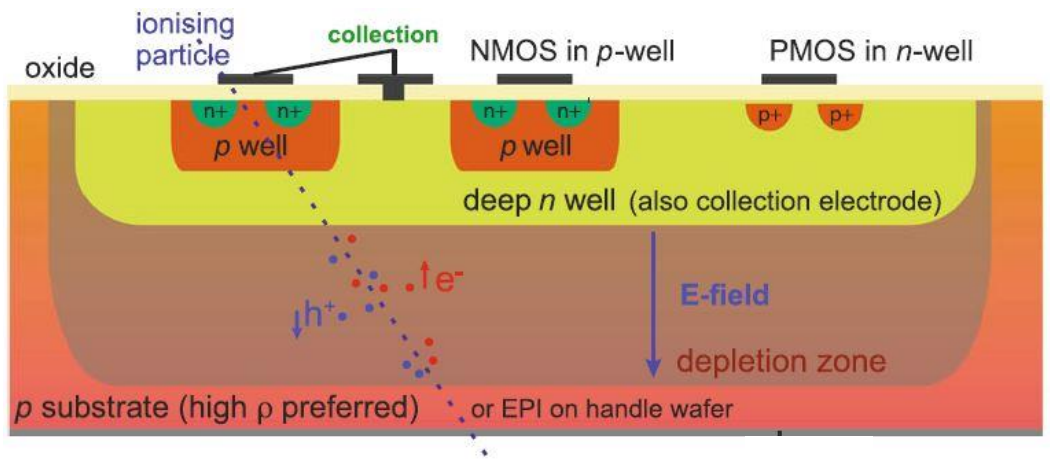
SciFi	Completion of a cryobox demonstrated program	Q4 2025
	Demonstration of radiation hardness of SciFi technology	Q1 2026
Pixel	Demonstration of radiation hardness of MAPS technology	Q2 2025
	First test results of Mighty-Pixel chip	Q2 2026
	Concept of a readout flex	Q3 2025
	Baseline design of the module	Q3 2025
	Proof of concept of a module	Q1 2026
Mighty	Concept design of electronics architecture	Q2 2025
	Concept design of mechanical integration of the Mighty-Tracker (SciFi+Pixel)	Q4 2025
	Proof of concept of a Pixel insulated enclosure box	Q2 2026

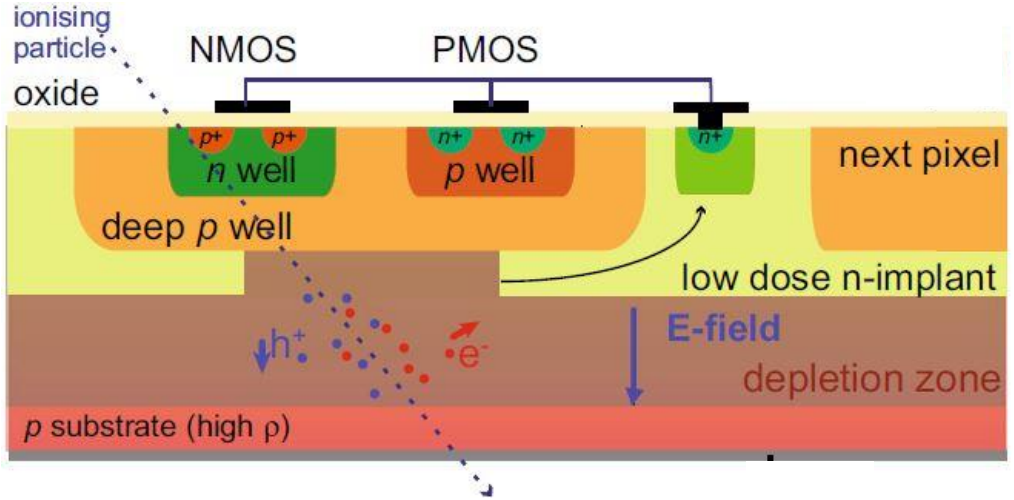
Mighty-Pixel – Naming convention



Monolithic pixels technology

Evolution of Silicon Sensor Technology in Particle Physics, F. Hartmann





Large collection electrode

- Readout electronics inside collection electrode
- High radiation tolerance thanks to HV substrate biasing (a few hundred V)
- *High* sensor capacitance
  - Higher noise
  - Higher power consumption

➔ MightyPix (180 nm), RadPix (150 nm), COFFEE (55 nm)

Small collection electrode

- Readout electronics outside collection electrode
- High radiation tolerance thanks to process modification
- *Low* sensor capacitance
  - Lower noise
  - Lower power consumption

➔ SPARC (65 nm)

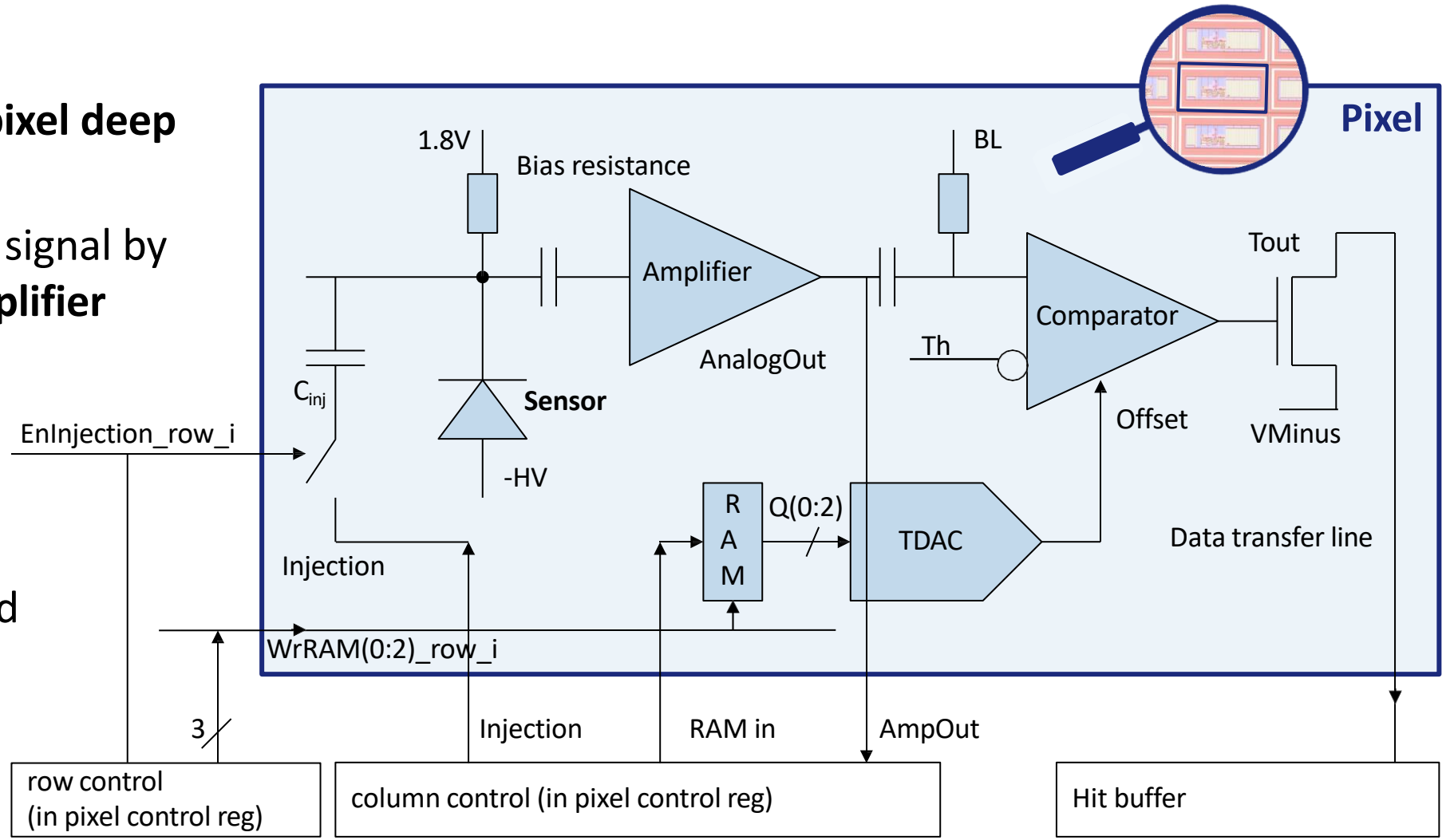
Mighty-Pixel: *Sensor specifications*

- **Compatibility with the LHCb readout system**
  - Run with the LHC clock at 40 MHz
  - Use the lpGBT protocol (low-power GigaBit Transceiver) for communication
    - lpGBT is a high-speed communication protocol and chip for data transmission between detectors and data acquisition systems in physics experiments
    - Maximum input voltage 1.2 V (HV-CMOS chip has VDD = 1.8 V)
    - Protocol compliance (VELO scrambler (8b/10b encoding), clock-data recovery, etc.)
    - I/O standards (LVDS, CML)
    - Clocking requirements and latency
    - Data rate (≤10.24 Gbps)
  - Meet Timing and Fast Control (TFC) + Experiment Control System (ECS)
    - TFC controls the entire readout of the LHCb detector. It is essential for ensuring that the entire detector is working in a synchronised manner, with minimal delays between collision events and data collection.
    - ECS manages and controls all sub-systems involved in the experiment.

MightyPix: *Analogue readout*

Hit detection

- Charge collected by **pixel deep n-well**
- Converted to voltage signal by **Charge Sensitive Amplifier**
- Analogue voltage pulse converted to digital signal by **comparator**
- Hit information stored in **hit buffer**



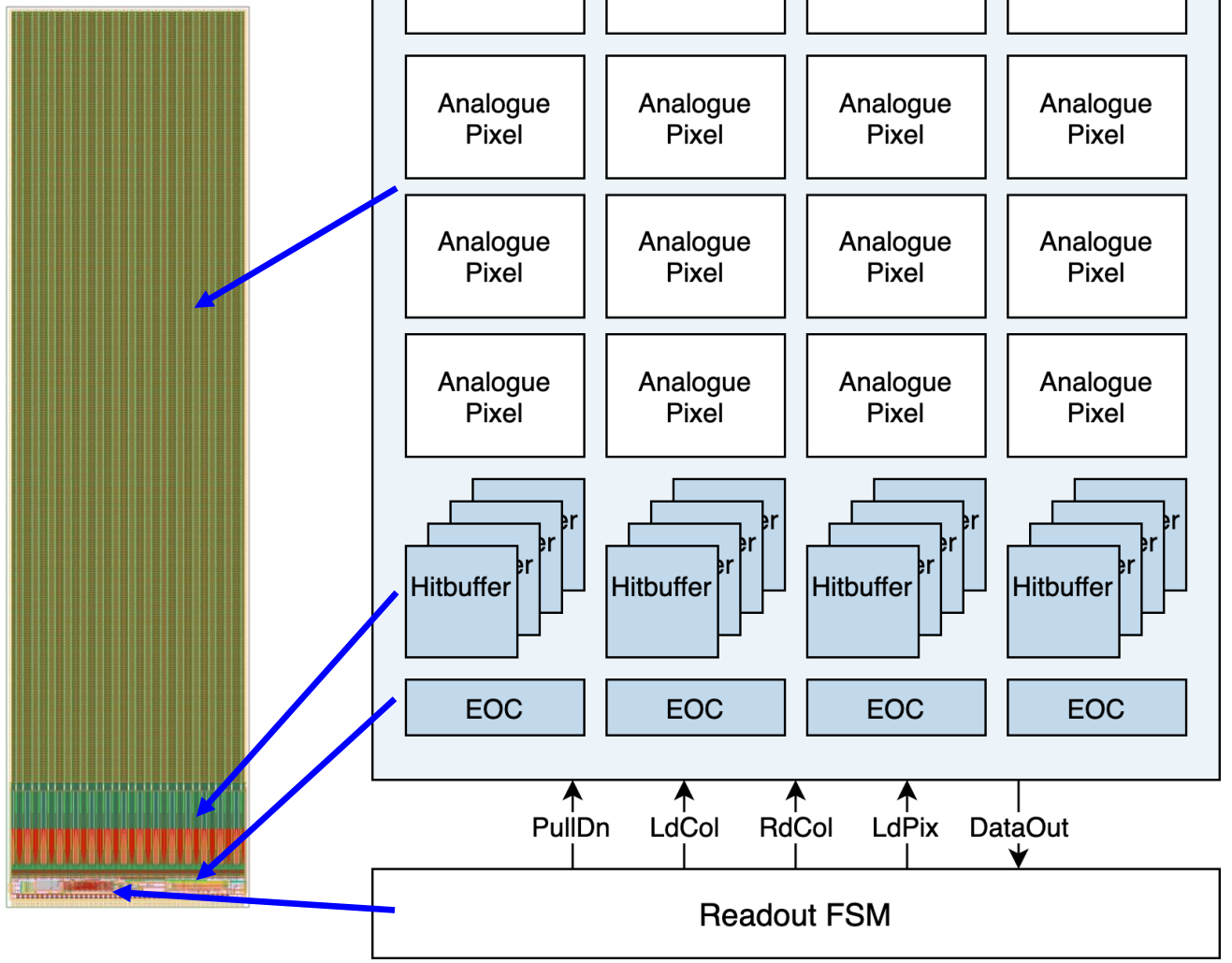
Schematic of the MightyPix1 Analogue Pixel (Adapted from: Ivan Peric, KIT)

MightyPix1: *Digital readout*

- Readout driven by Readout Control Unit (RCU) Finite State Machine (FSM)

Working principle

- Hit information stored in **hit buffer**
- Data loaded from highest active hit buffer to End of Column (EoC) buffer
- Read data from EoC
- For every hit 2 x 32 bit data word is generated
- Parallel scrambler analogue to VELOPix
- Data sent to serialiser tree and sent out

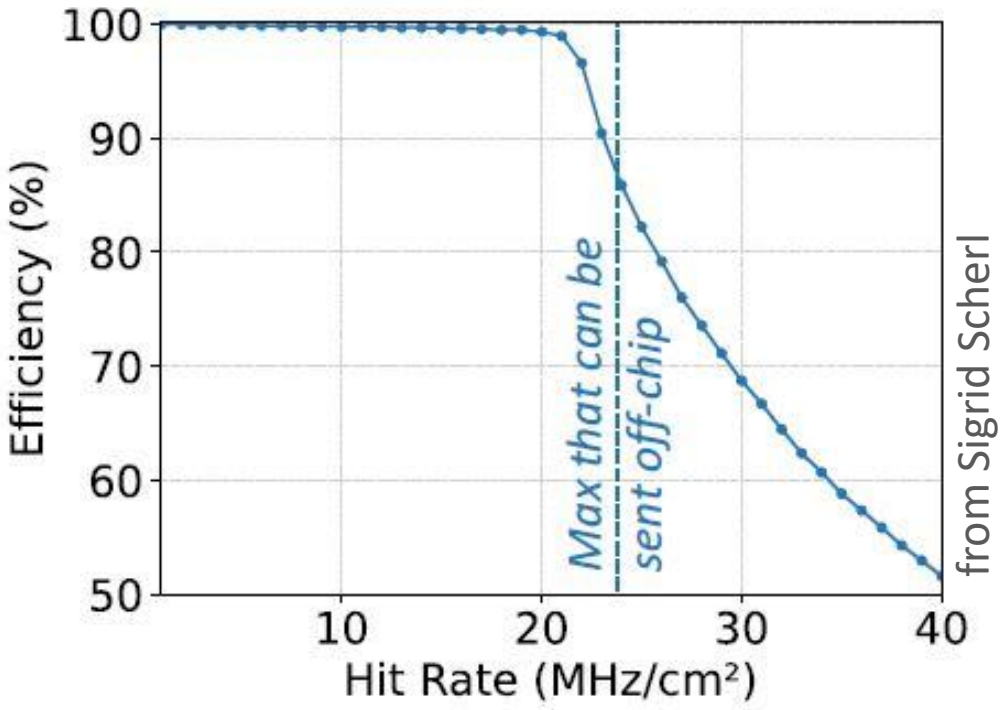


Source: Nicolas Striebig

MightyPix1: *Efficiency simulations*

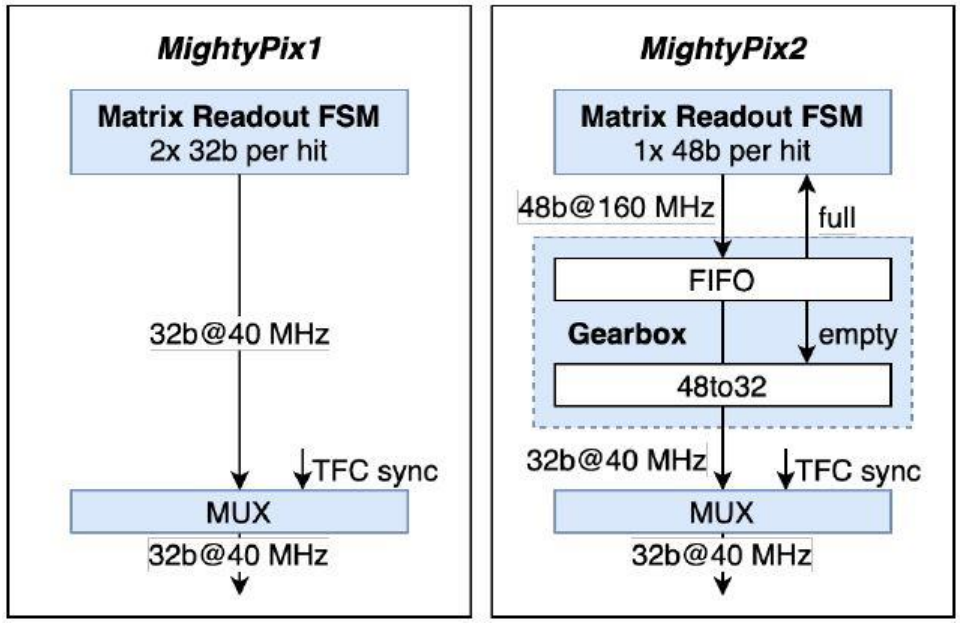
- **Can MightyPix1 handle the expected Mighty-Tracker rates of 17 MHz/cm²?**
  - Simulation of MightyPix1 digital readout with LHCb simulated particle hits

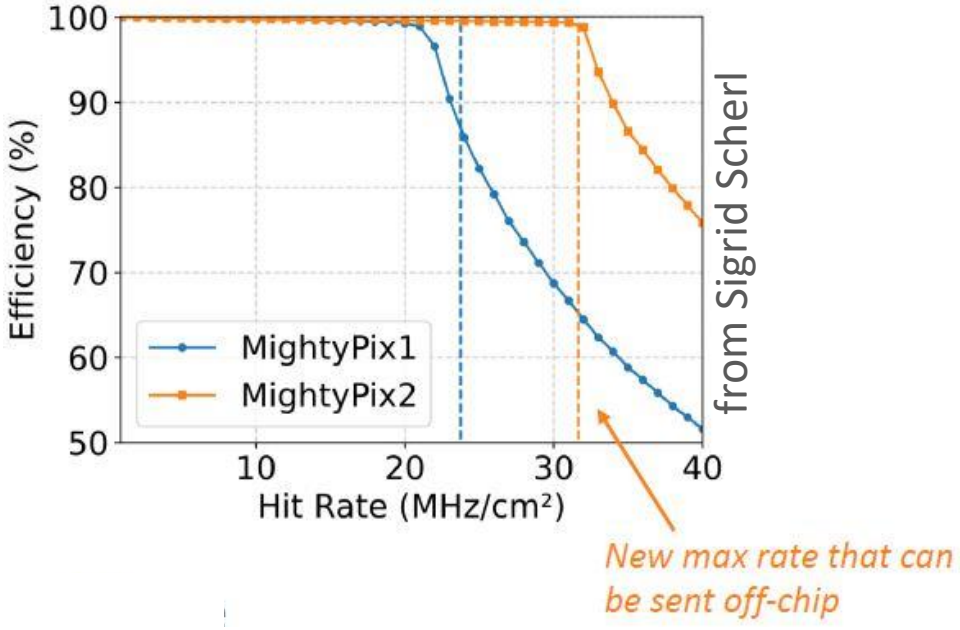
- Simulated efficiency of MightyPix1 readout mechanism > 99% up to 20 MHz/cm²
- Drop at 20 MHz/cm² as readout times reach 89.1 µs
  - Hit buffers are not fast enough → new hits are missed
- Need faster readout for larger safety margin



Towards MightyPix2: *New readout*

- **Decreased data size**
  - 2 x 32 bit per hit → 1 x 48 bit per hit
  - Can send up to 31.66 MHz/cm^2 off-chip
- **Increased FSM readout speed**
  - 32 bit at 40 MHz → 48 bit at 160 MHz
  - Hit buffers read out faster, less hits missed
- **New on-chip memories**
  - 16-bit depth FIFOs which store hits before they are sent off-chip
- Simulated efficiency of improved readout mechanism > 99% up to 31.66 MHz/cm^2 → larger safety margin
  - Drop as 1.28 Gbit/s readout link works at full capacity





Evaluation of TID irradiated chips

Source: Hannah Schmitz

- TelePix2 sample irradiated to 40 MRad (X-rays)
- 99% hit efficiency achieved for
  - 40 MRad (TID)
  - 1×10^{14} n_{eq}/cm^2 (NIEL, protons)
- Negligible noise rate
- Evaluation done with MARS setup, which is fully functional