Silicon R&D HV-CMOS

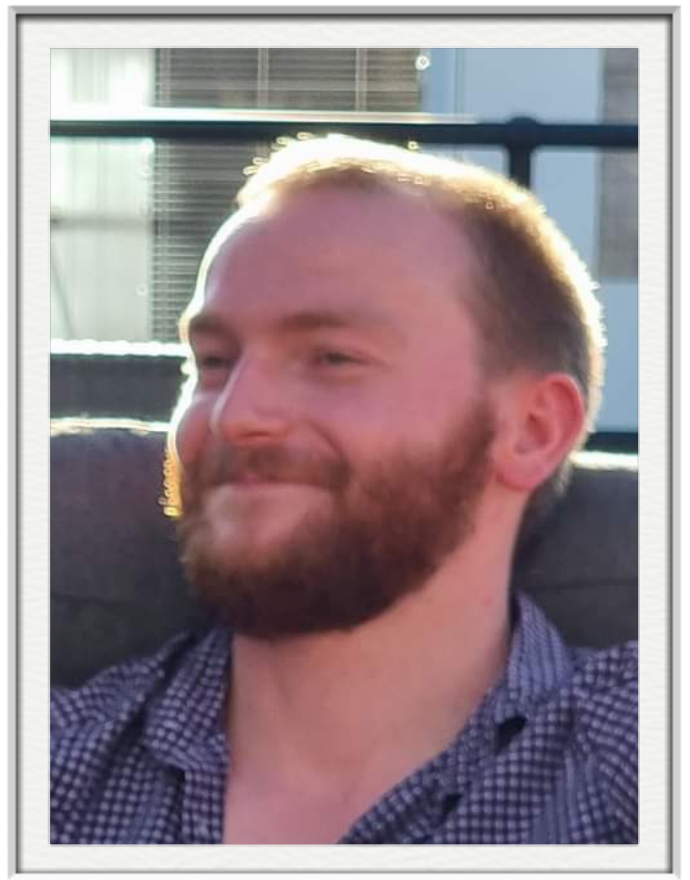
Chenfan Zhang
on behalf of the HV-CMOS group

UNIVERSITY OF
LIVERPOOL

HEP Annual meeting
23 May 2025

Liverpool HV-CMOS group

UNIVERSITY OF LIVERPOOL



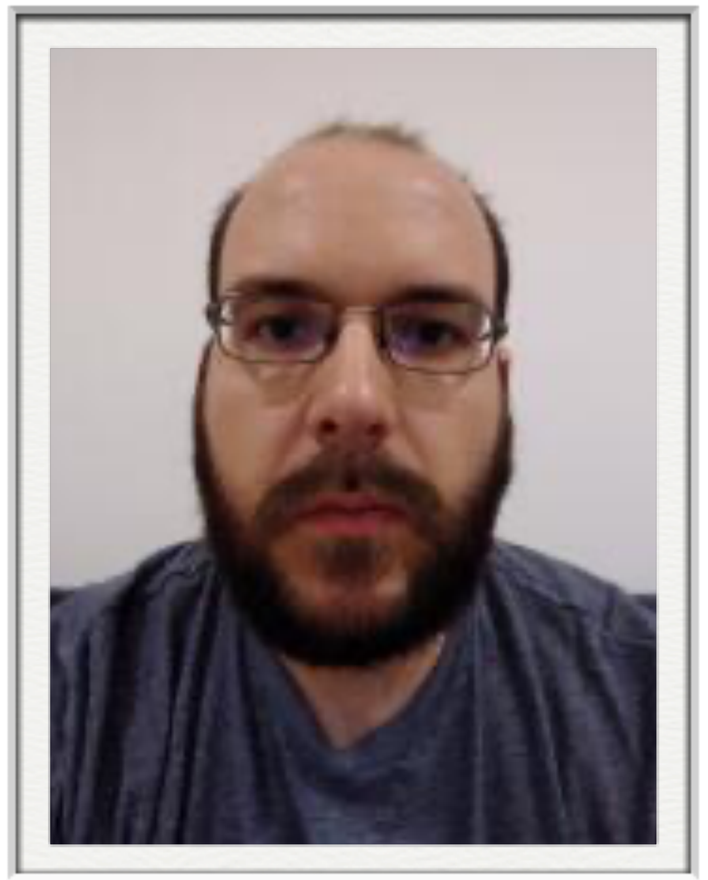
Ben

Chenfan

Eva

Archie

New PhD



Jan

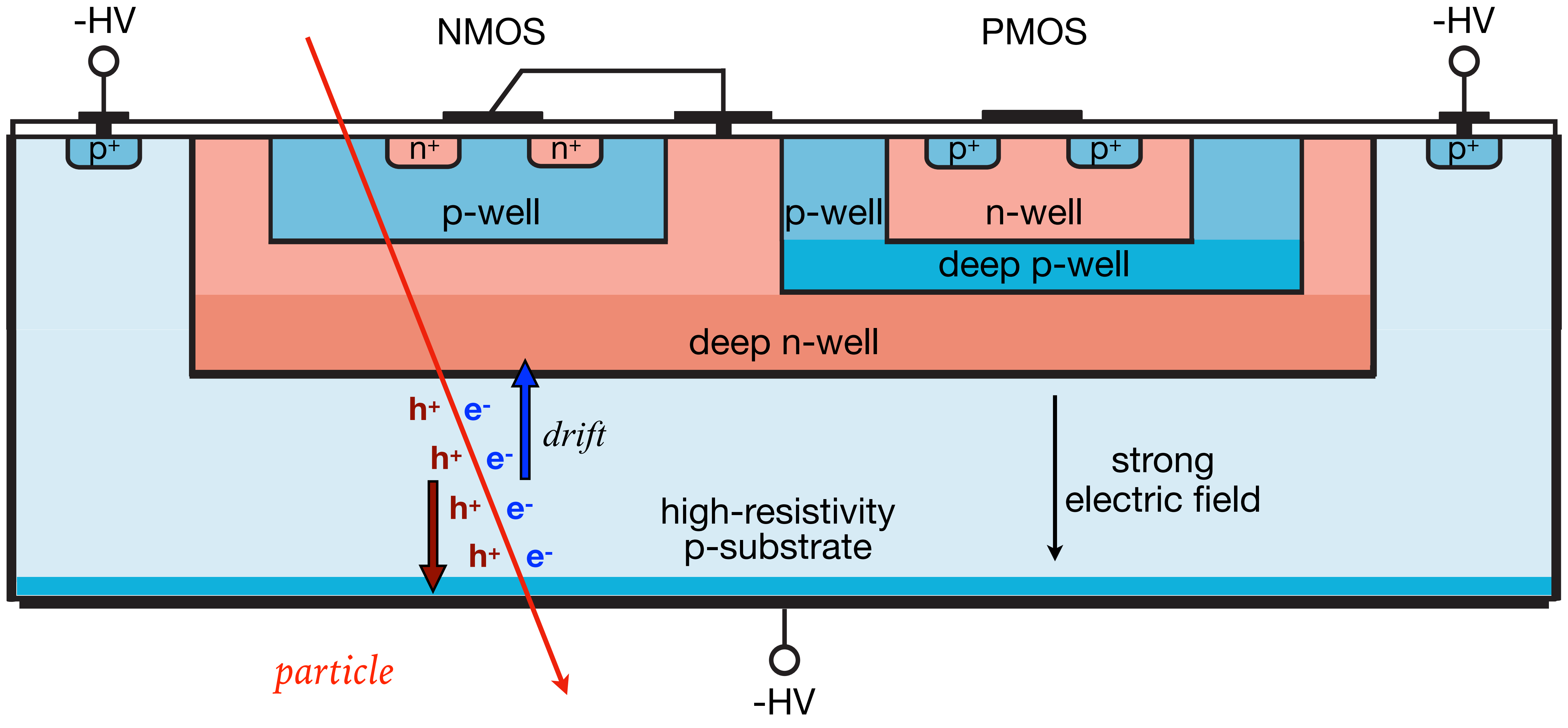
Sam Graduated

Sigrid Graduated

- Design advanced HV-CMOS detectors, make DAQ systems and evaluate them in lab and testbeam.

HV-CMOS: monolithic pixel detectors

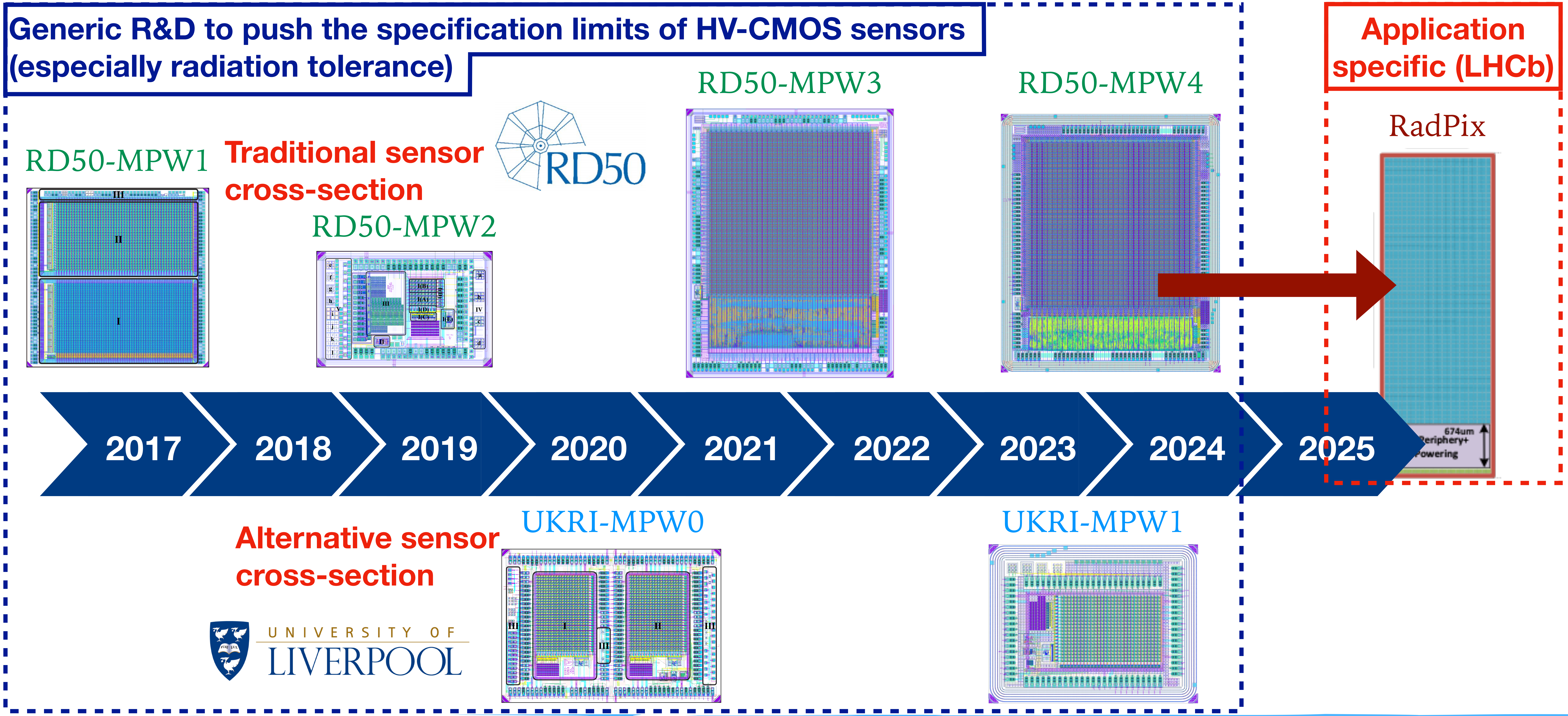
- Monolithic: Sensor and readout electronics in a single silicon wafer.
  - one layer structure: low material (> 50 μm);
  - no bump-bonding assembly: low production cost (~ £100k/m^2);
  - high bias voltage: fast charge collection by drift and wide depletion in substrate → high radiation tolerance (5×10^{15} 1 MeV n_{eq}/cm^2).



- The Mu3e experiment and LHCb Mighty Tracker Upgrade have chosen HV-CMOS pixel detectors.
- Other possible applications: HL-LHC, CEPC, FCC, and fields outside HEP experiments.

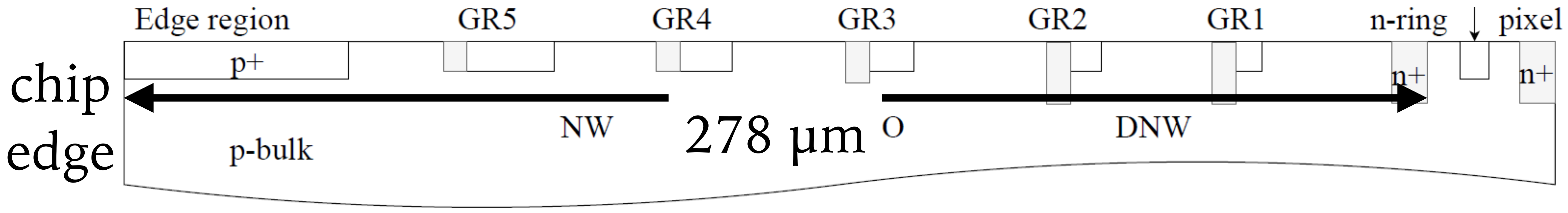
HV-CMOS prototypes from Liverpool

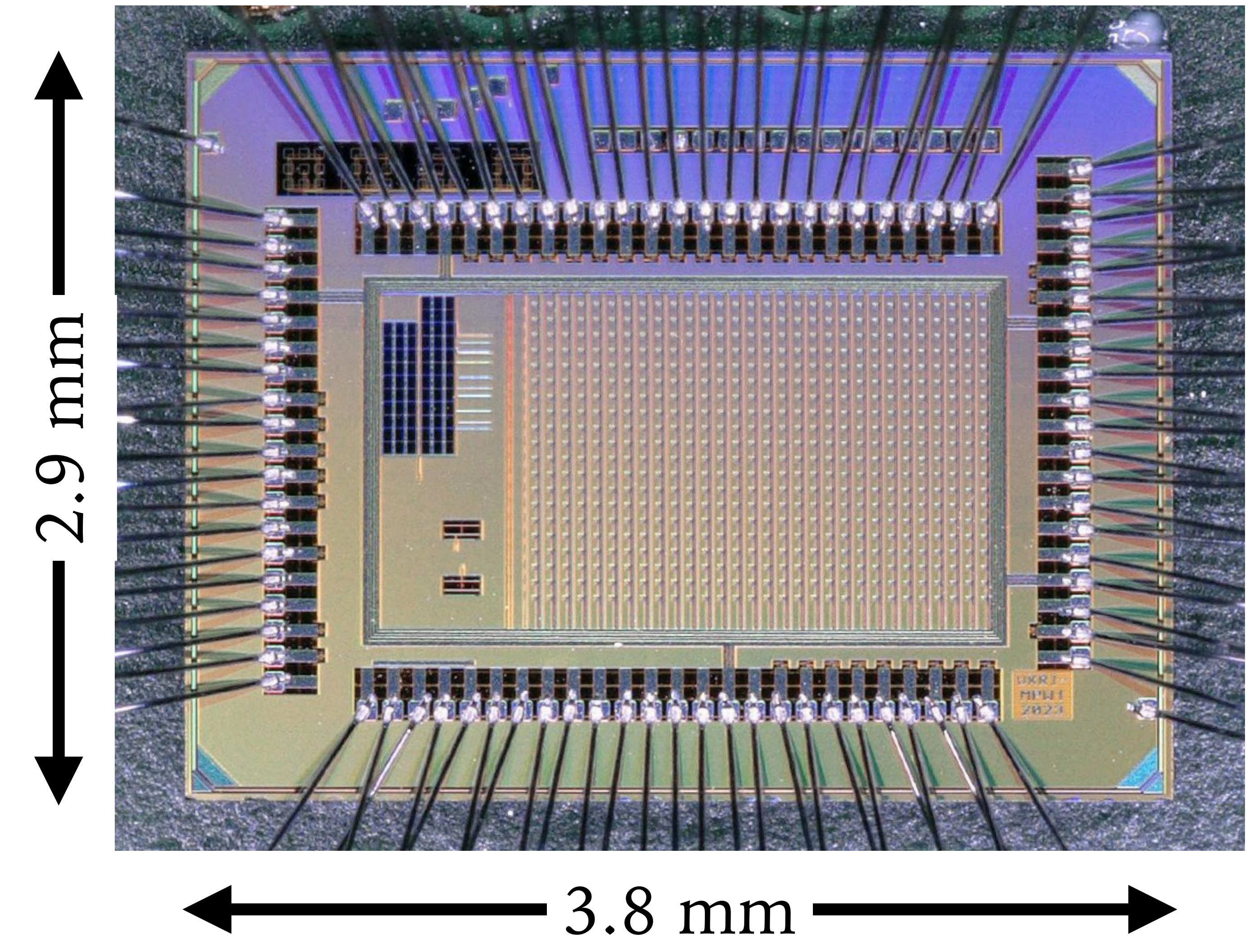
- Developed using LFoundry 150 nm process.



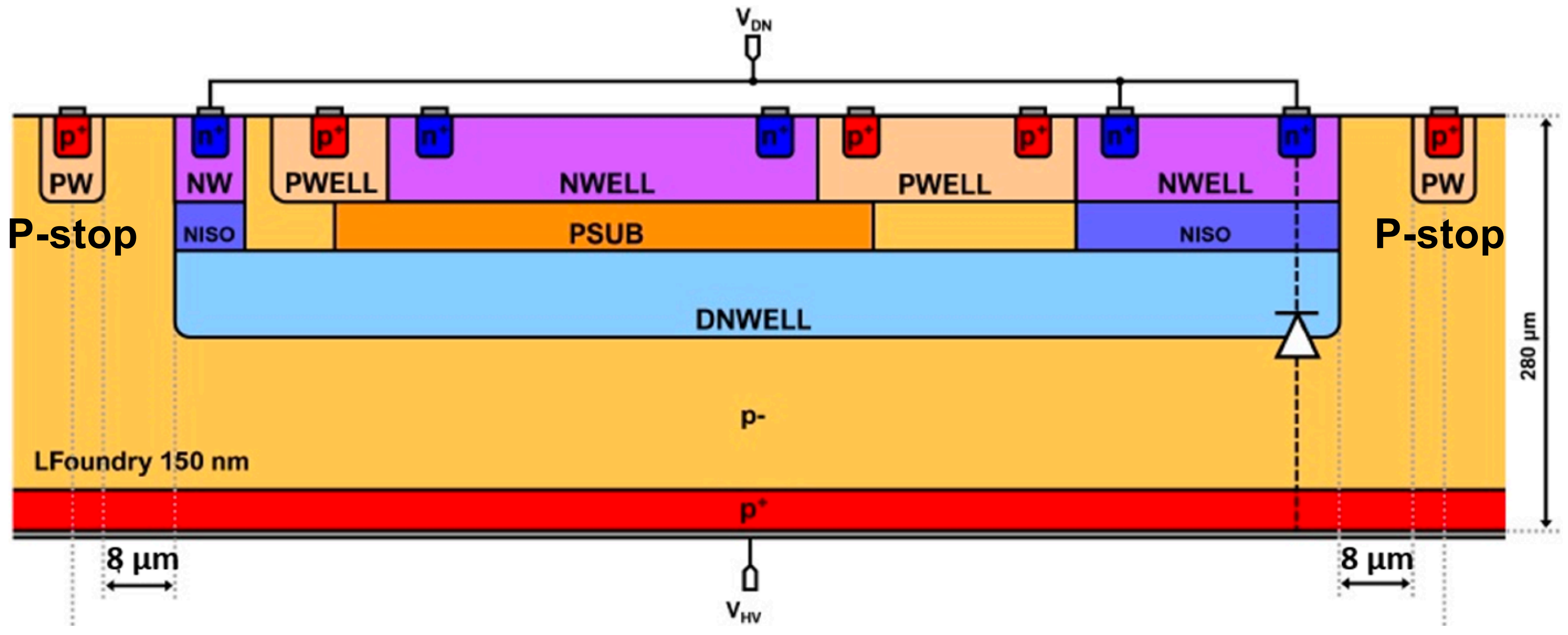
UKRI-MPW1

- Use multiple guard rings to increase breakdown voltage and lower leakage current.

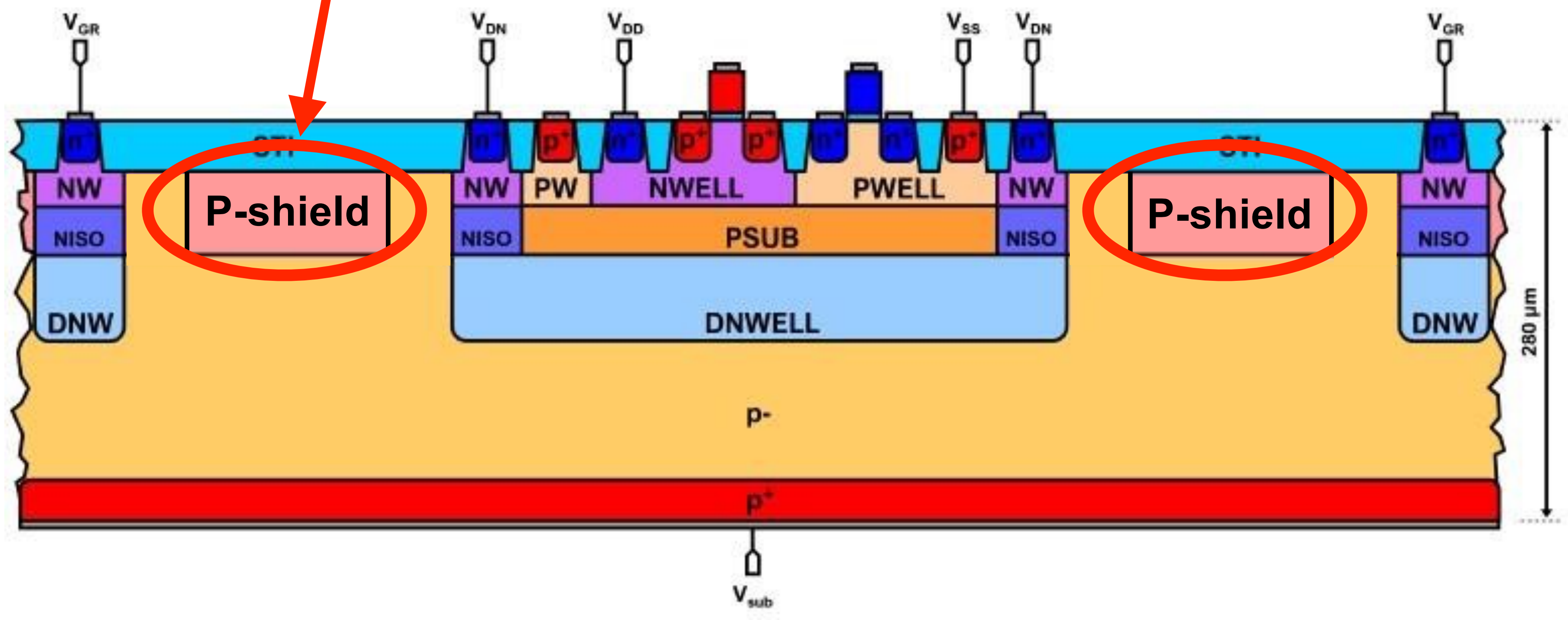




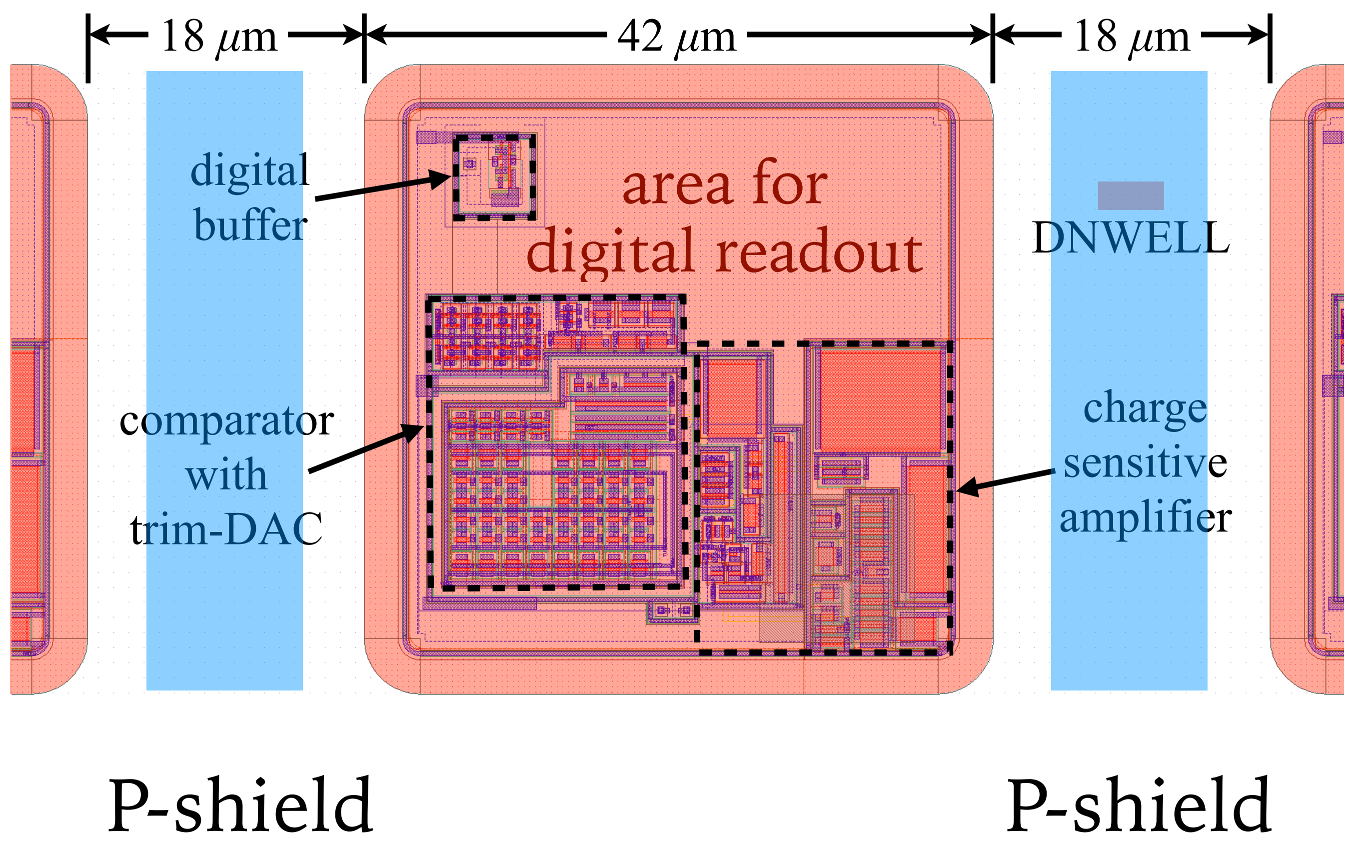
- Use customised low-doped P-type isolation P-shield between pixels, co-developed with LFoundry.
- Backside processing to allow backside biasing.



RD50-MPW4

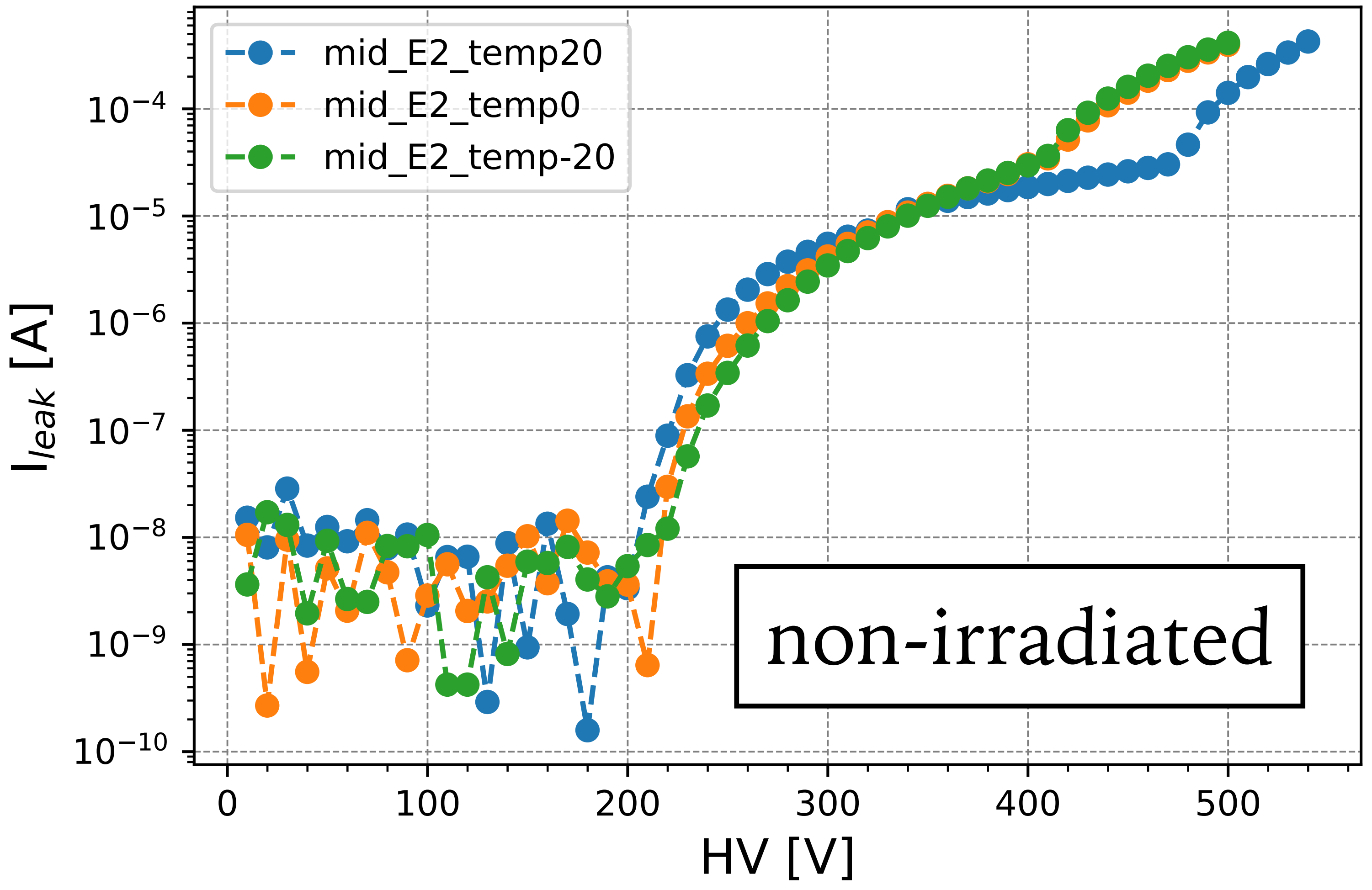


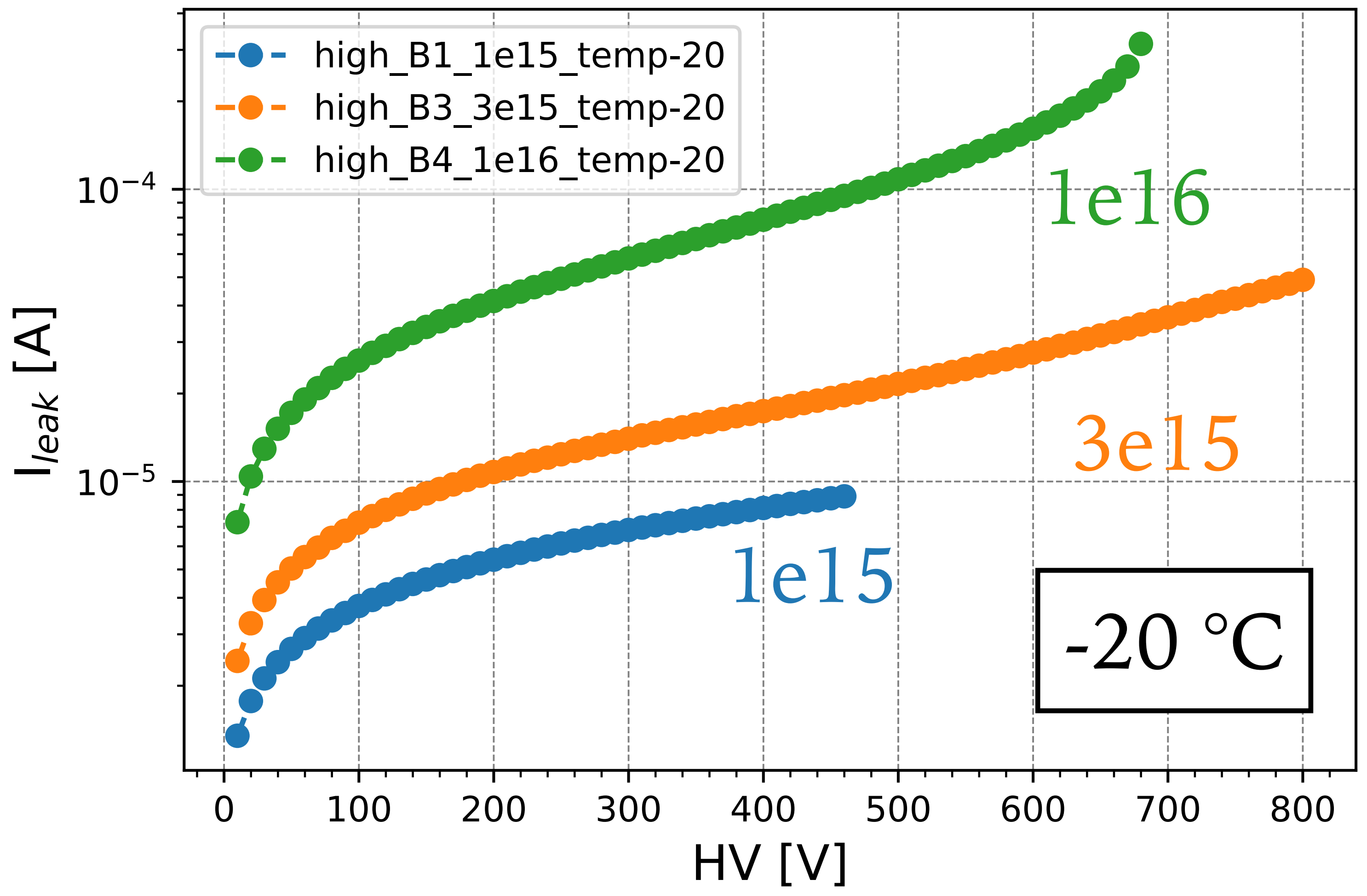
UKRI-MPW1

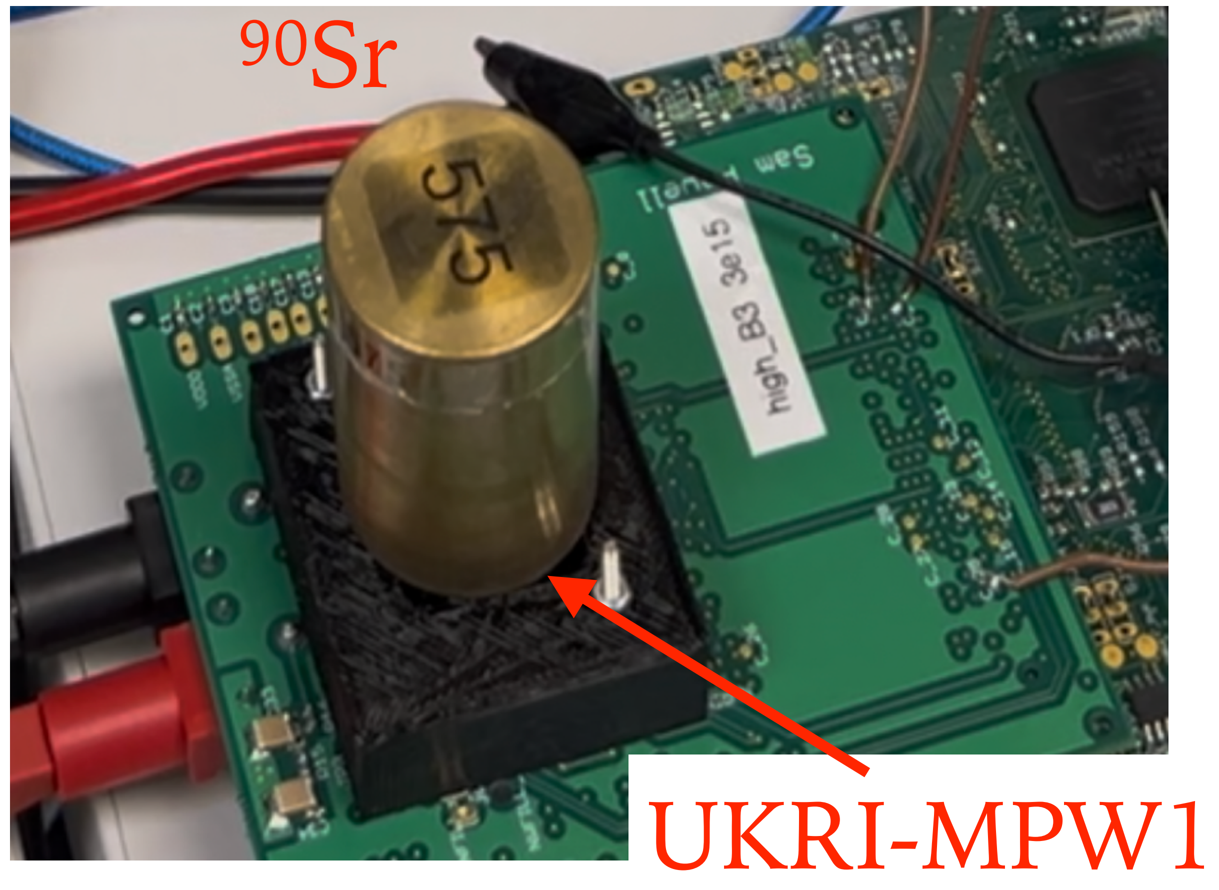


UKRI-MPW1

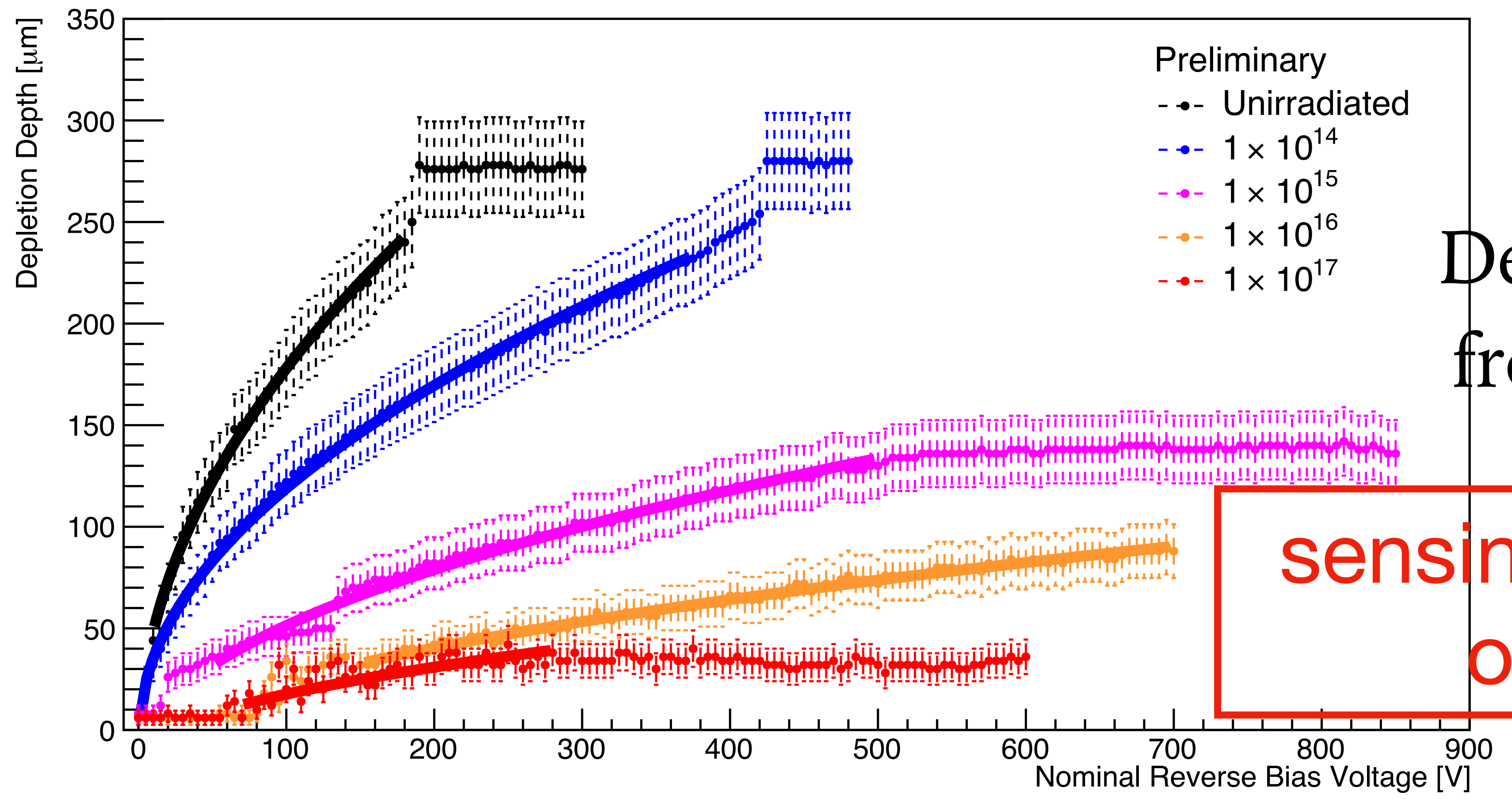
- Leakage currents before and after irradiation. Cooling is mandatory.







- Full depletion around 200 V before irradiation.
- Achieve ~ 90 µm depletion in 1e16 sample.



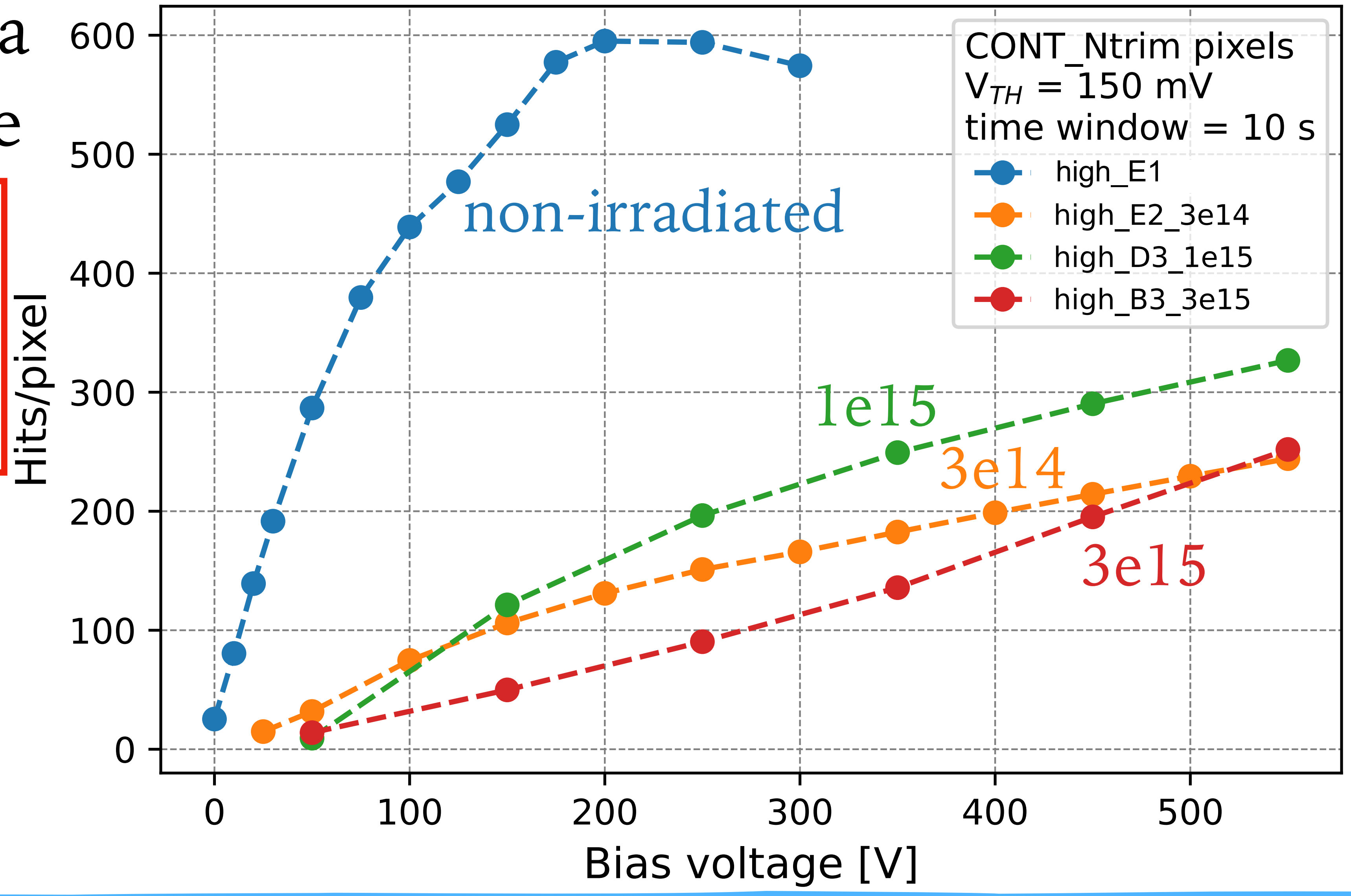
Depletion depth from Edge-TCT

sensing diode only

- Still working after 3e15 irradiation.

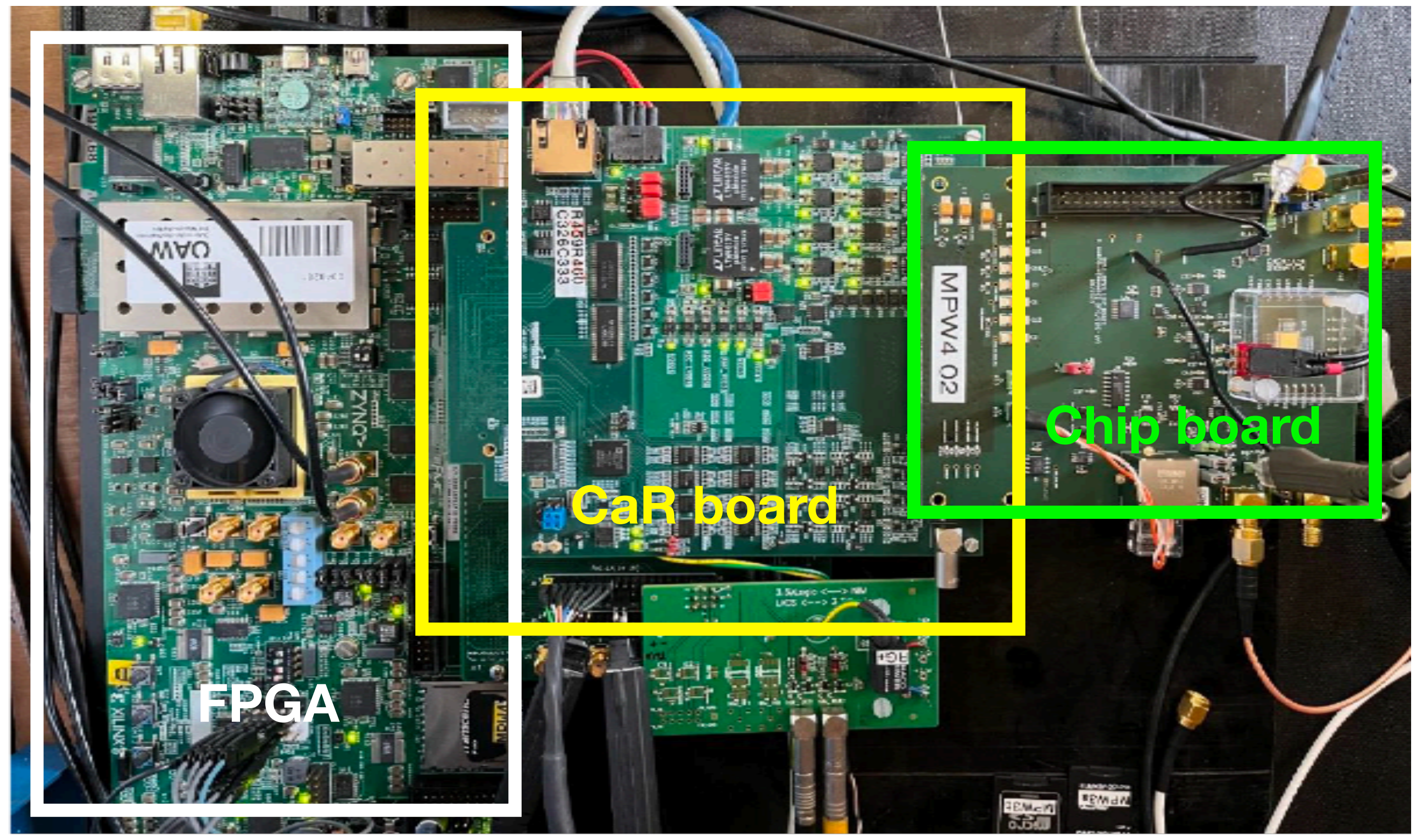
Hits from a ^{90}Sr source

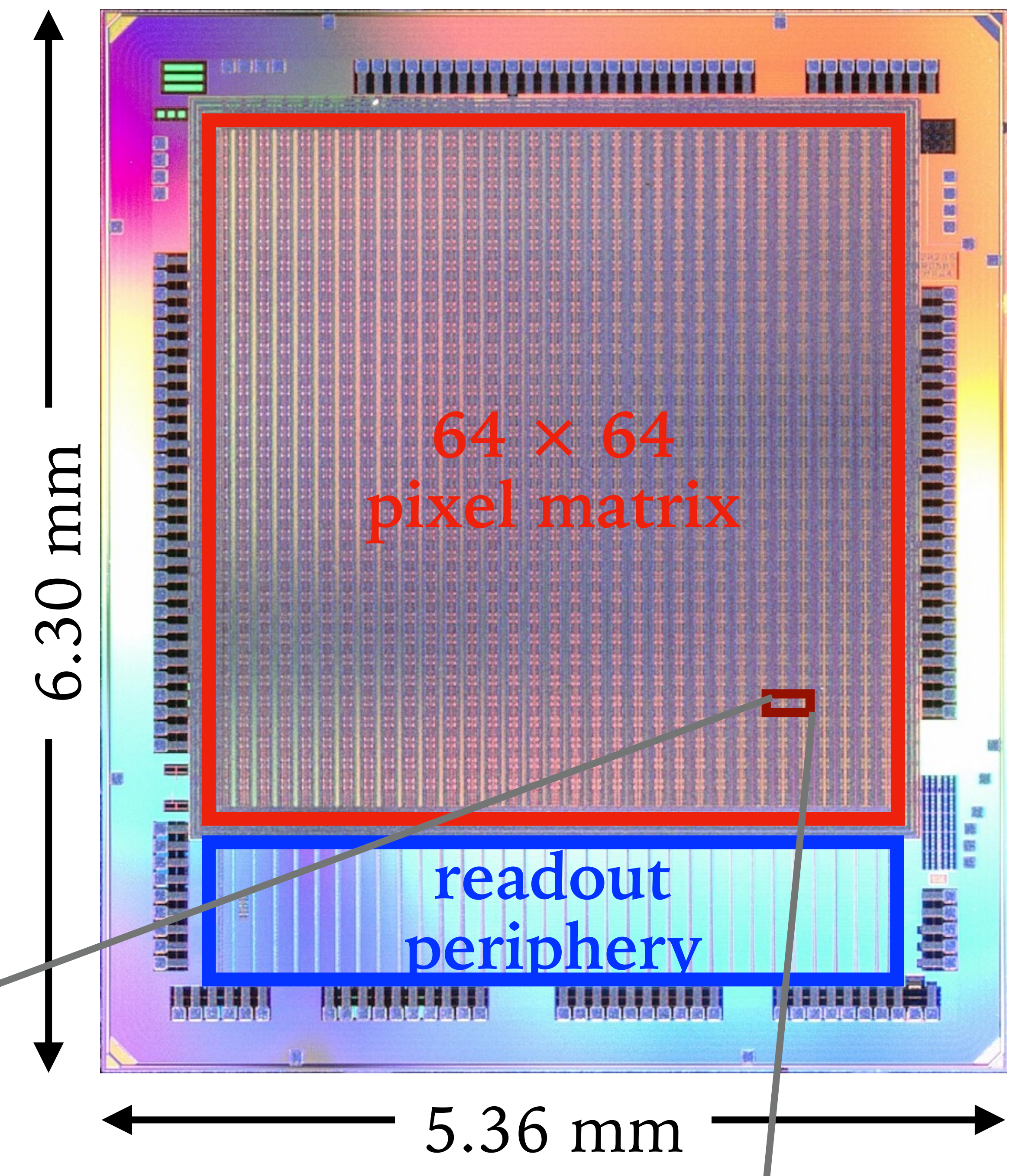
sensor and on-chip electronics

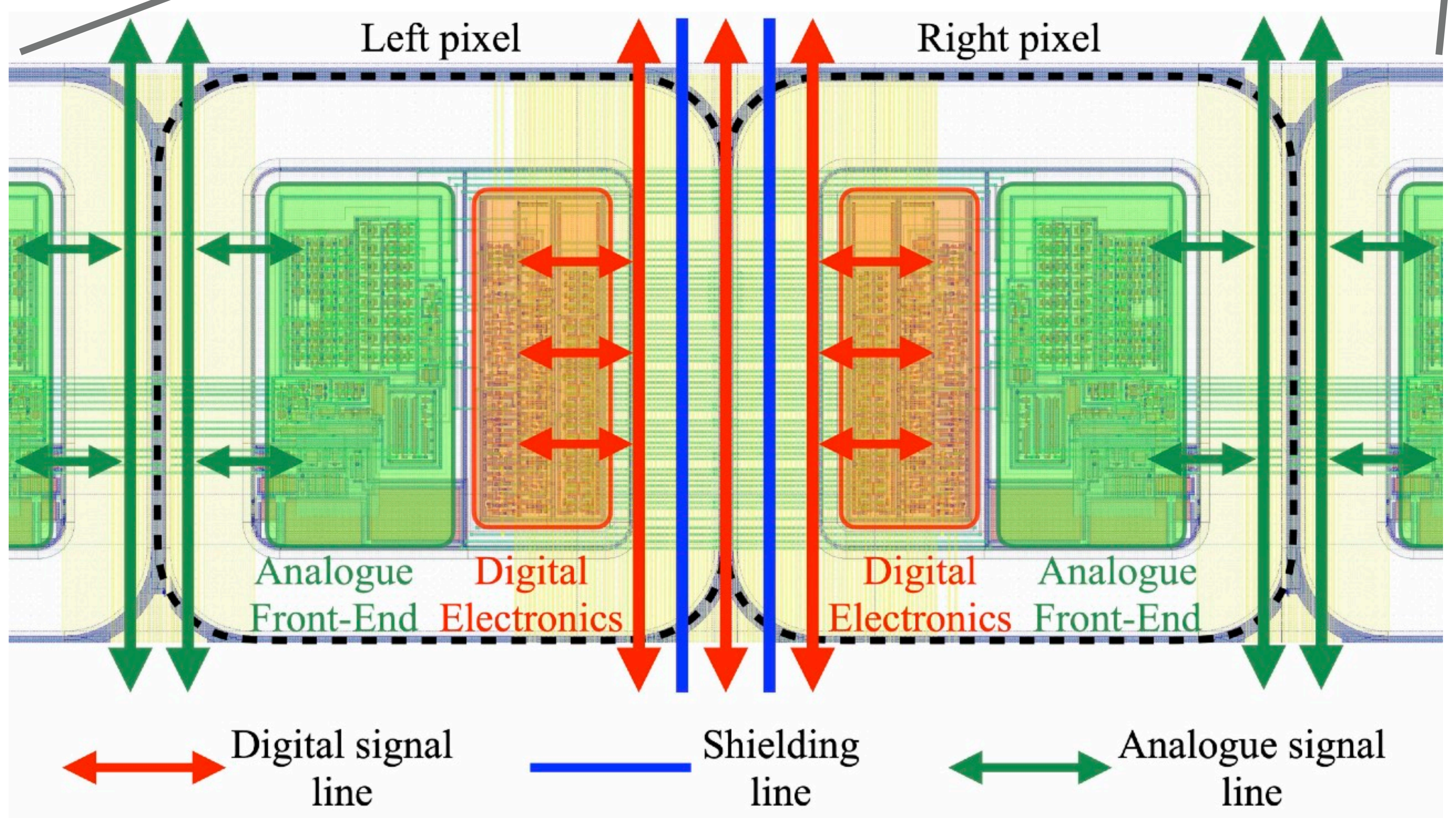


RD50-MPW4

- Fabricated on 3 kΩ·cm wafers and thinned to 280 μm.
- Mainly composed of a 64 × 64 pixel matrix and a digital readout periphery.
- **pixel matrix**:
  - 62 μm × 62 μm pixel size;
  - both analogue and digital readout embedded inside pixel;
  - pixel matrix in double-column architecture.
- **readout periphery**:
  - optimised readout periphery for fast chip configuration and data transmission.
  - I2C protocol for slow control.
  - Serialise data and send out through a 640 Mbit/s LVDS link.
- DAQ based on Caribou.

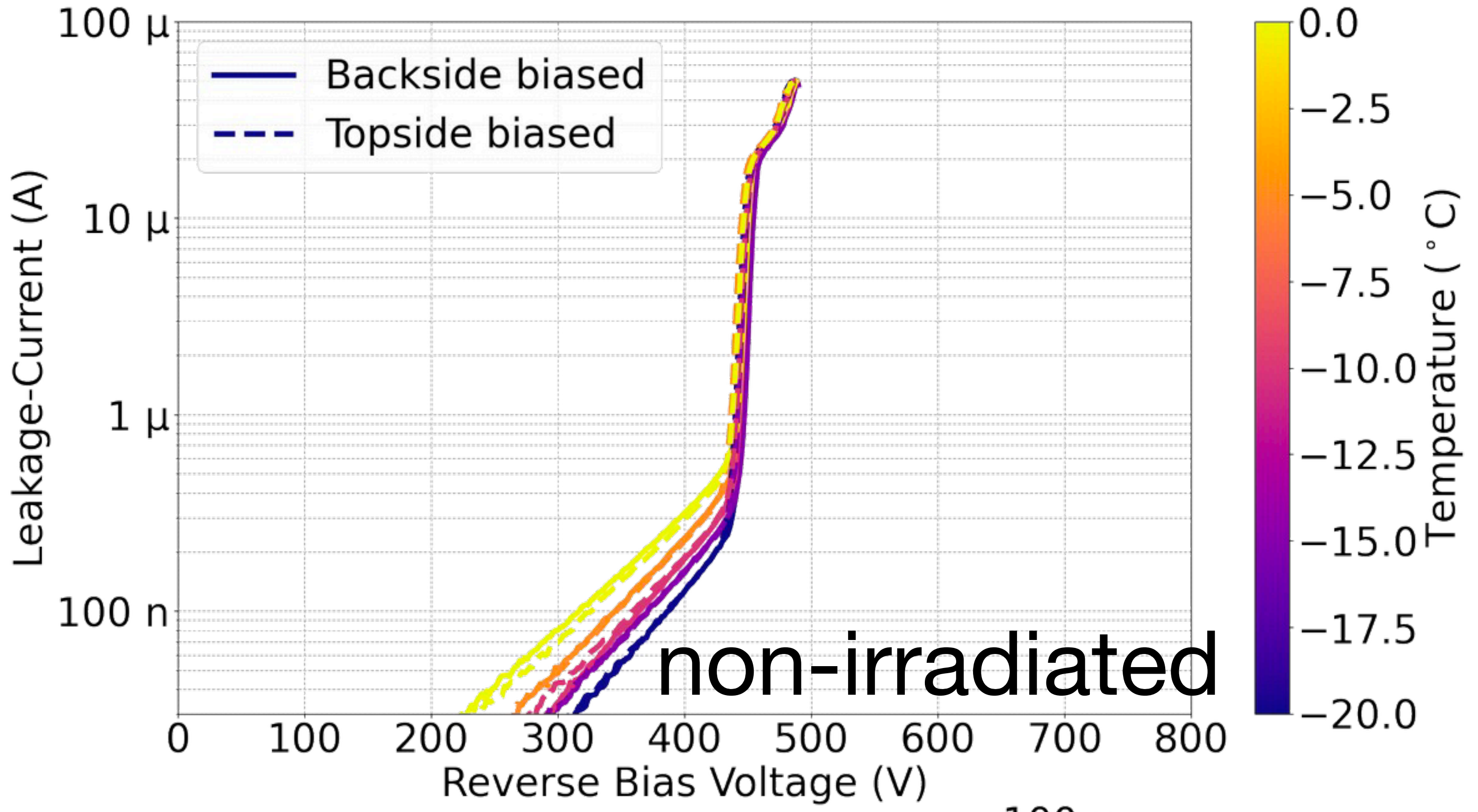


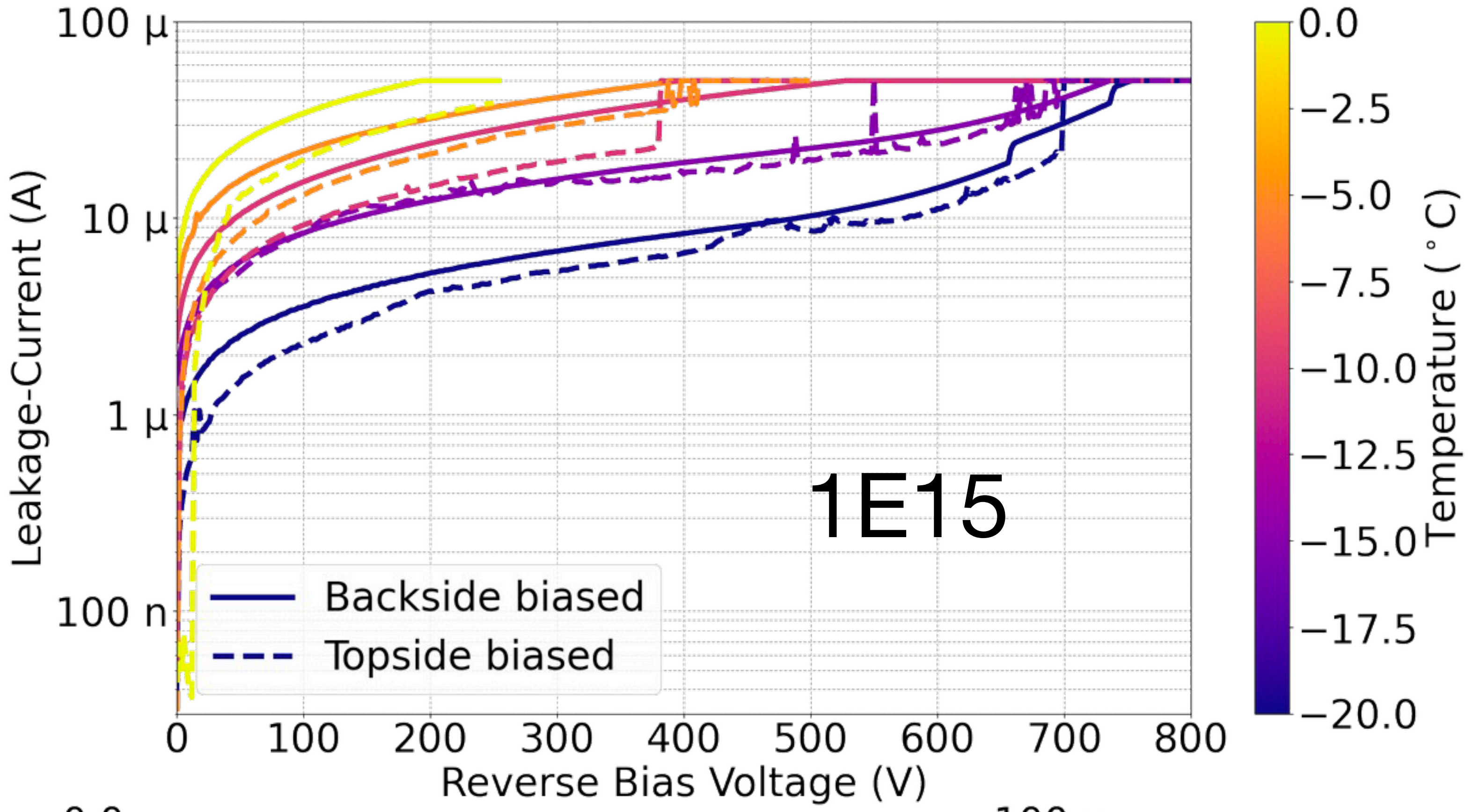




RD50-MPW4 - Irradiation campaign & I-V

- Neutron irradiation up to at TRIGA Mark III reactor in Ljubljana.
- Leakage current of the whole chip while configured, cooling from 0 °C to -20 °C in a climate chamber.
- Currents jump at ~450 V before irradiation.
- Leakage currents increase after irradiation. Cooling is mandatory.





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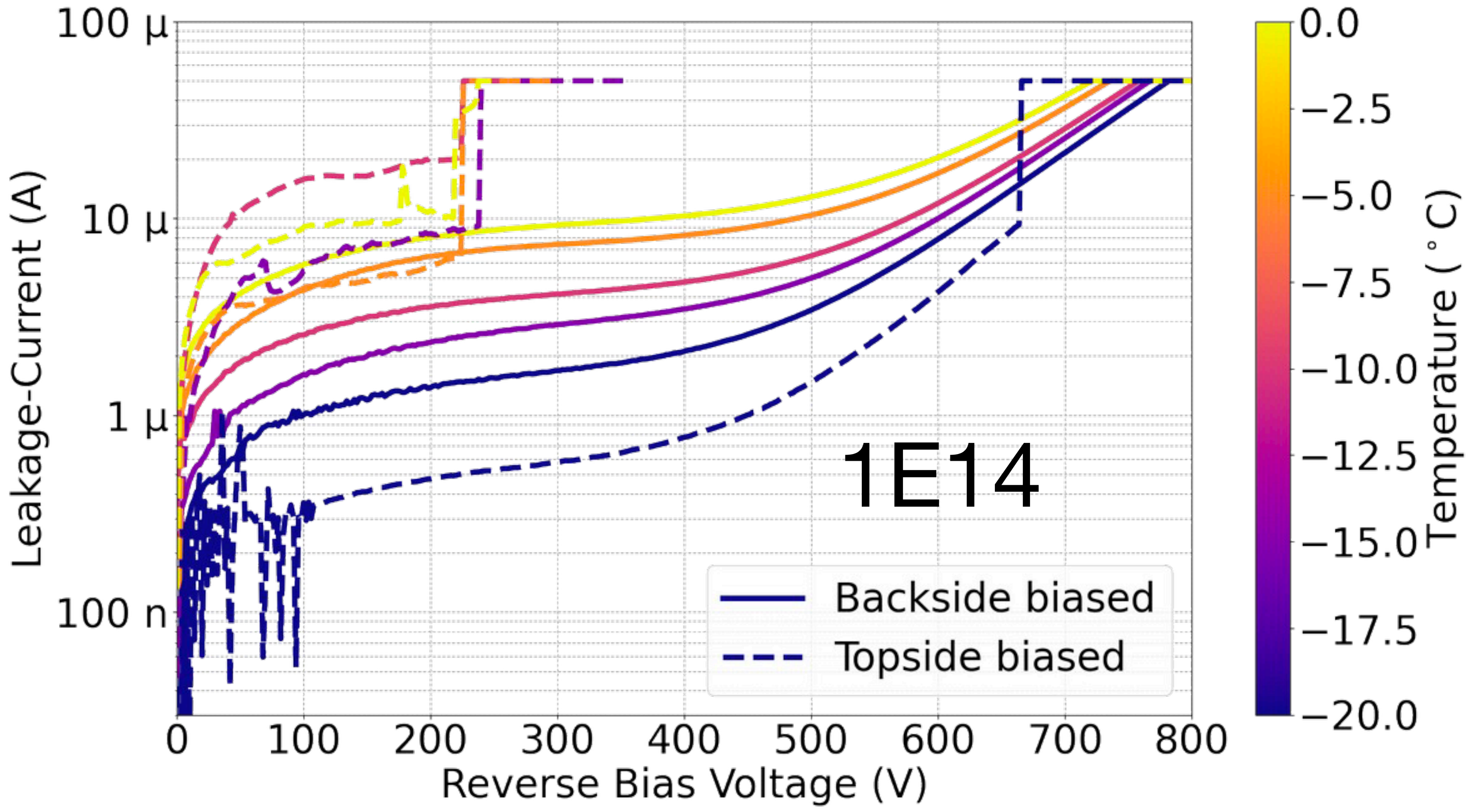
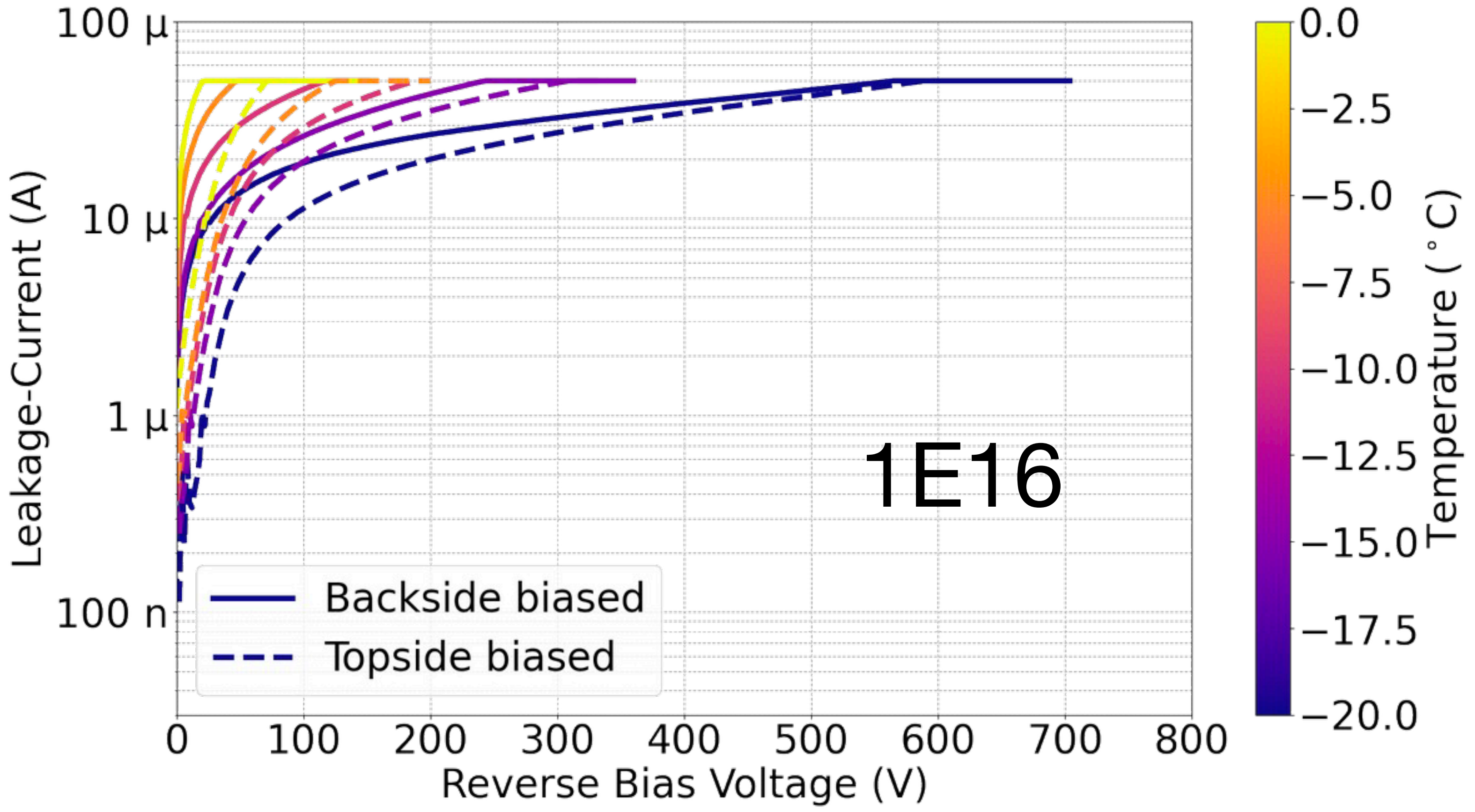
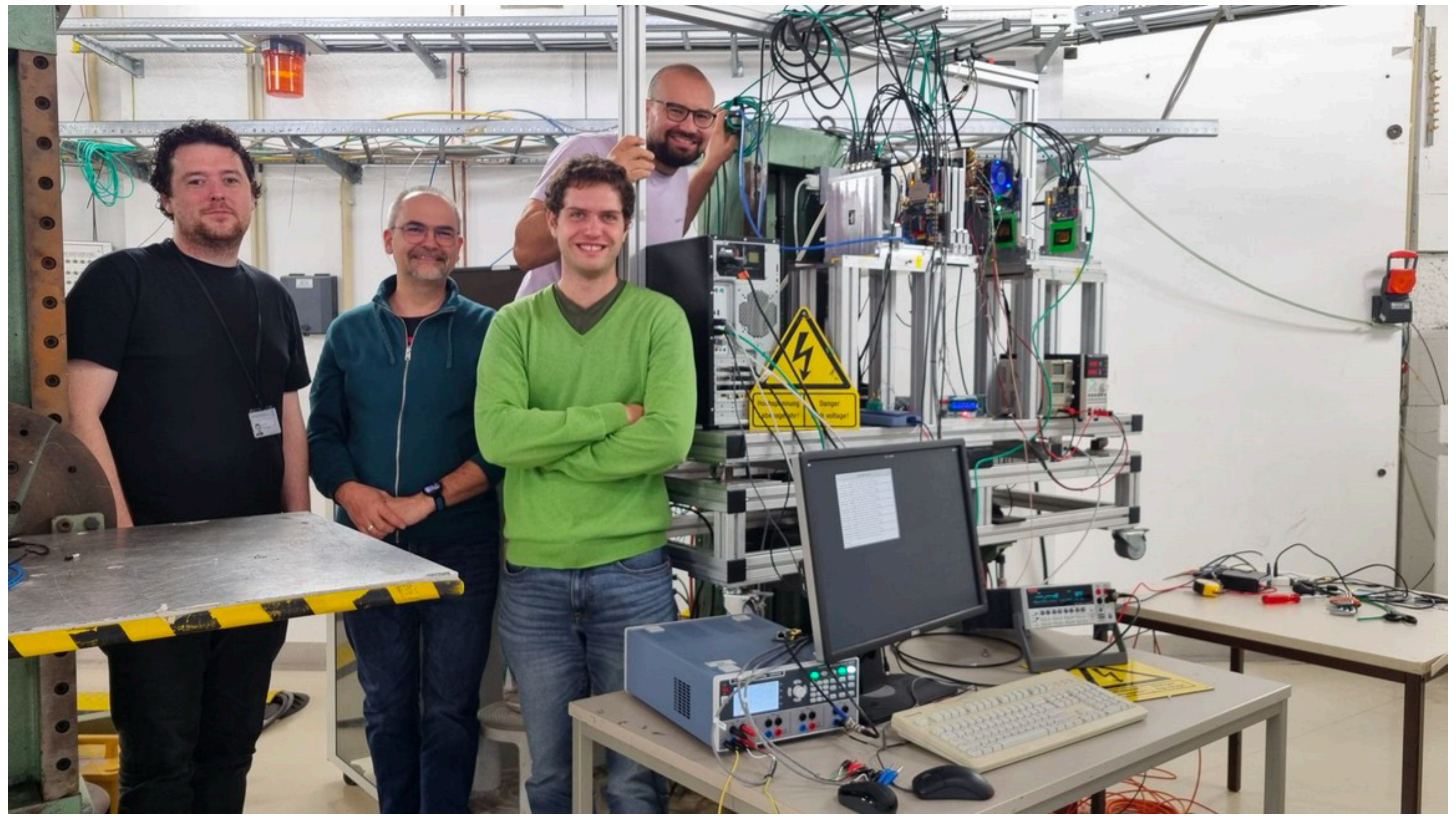
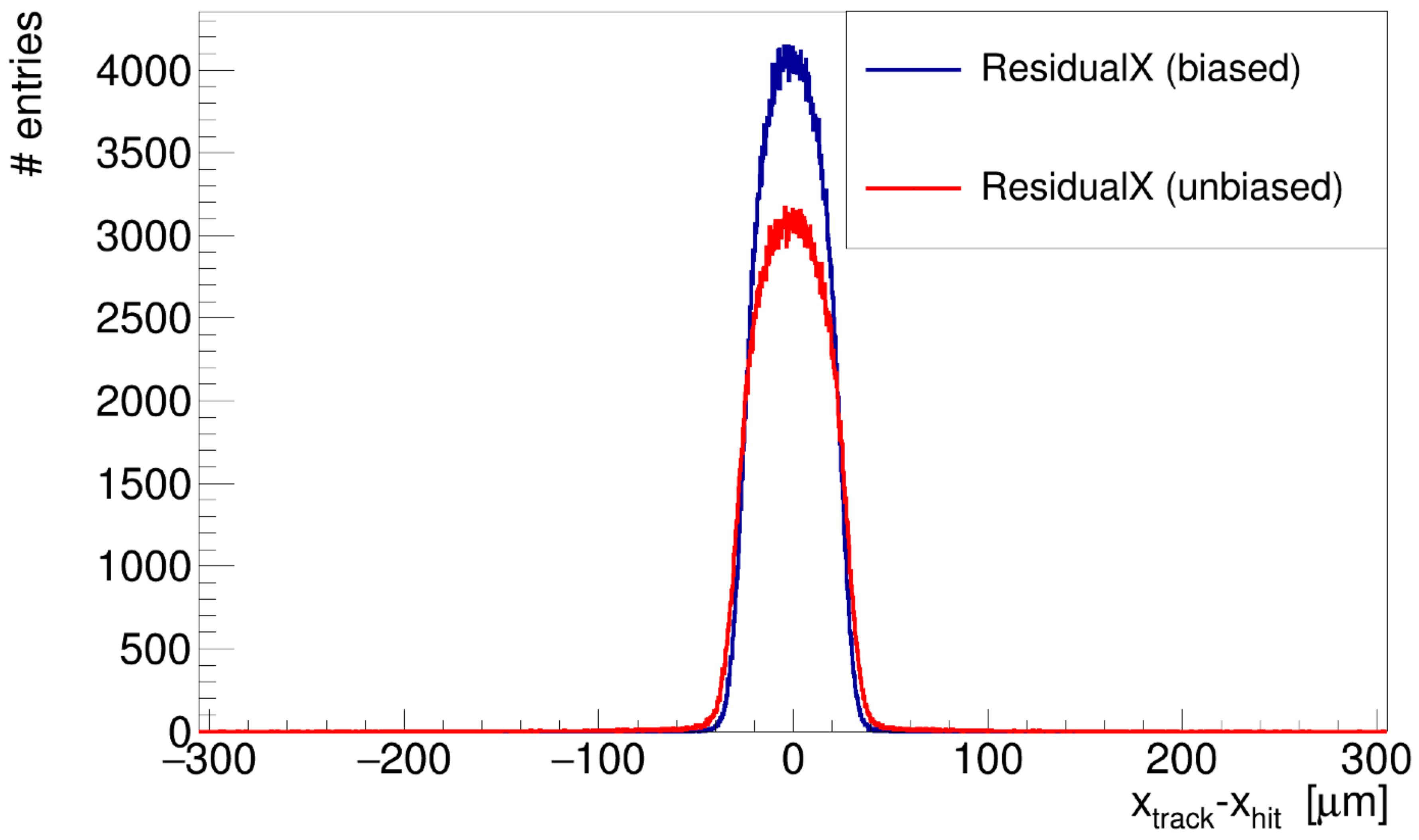


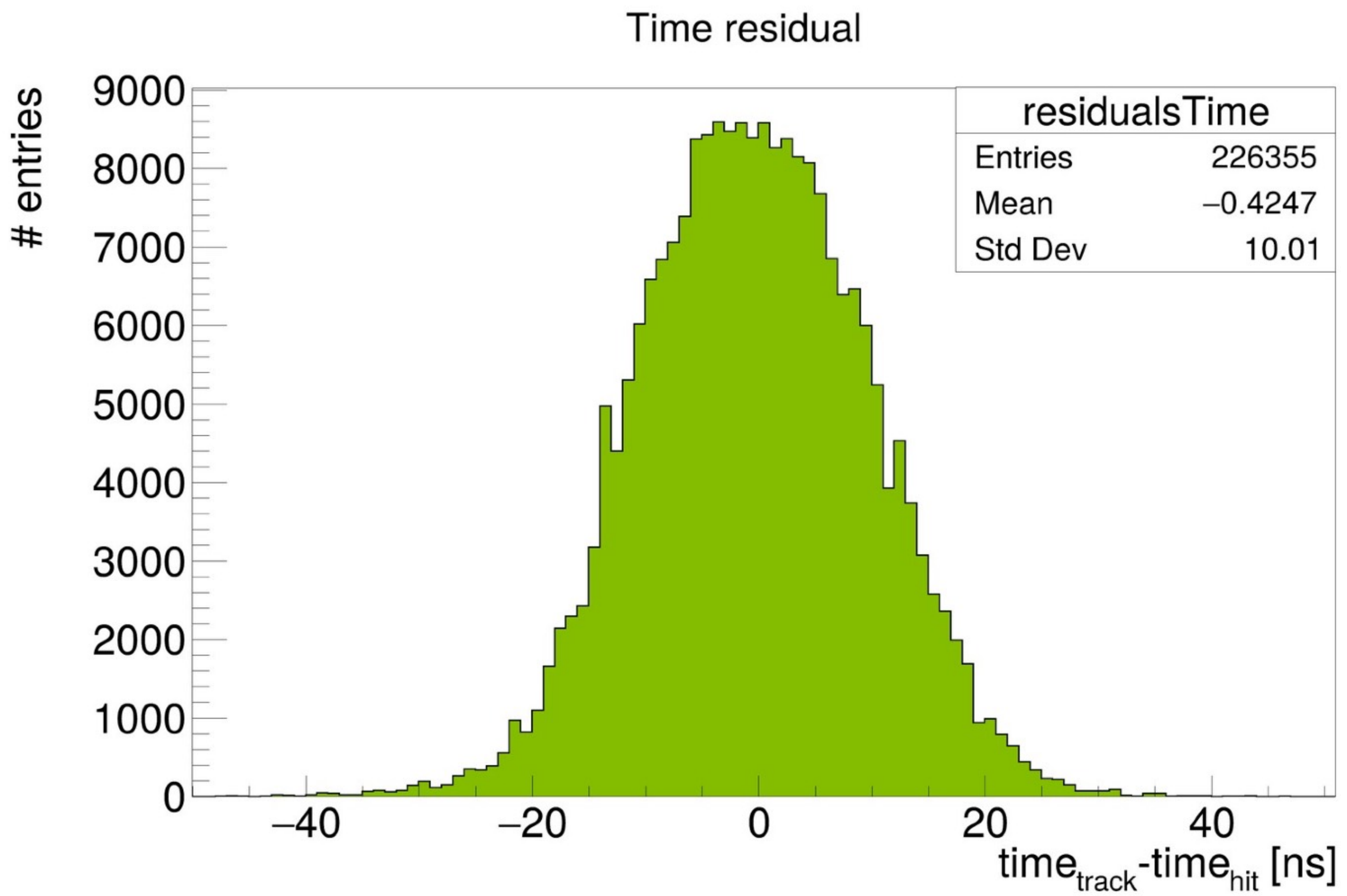


RD50-MPW4 - Testbeam

- Beamtest at DESY II beamline (4.2 GeV electrons, 10 kHz) Oct. 2024.
- Adenium telescope based on 6 Alpide planes, Telepix2 as timing layer, AIDA-2020 TLU as RoI trigger.
- Chip board cooled to -15 °C using a Peltier based cooling setup.
- Corryvreckan used for data analysis.
- 15.9 µm space resolution.
- ~10 ns time resolution.

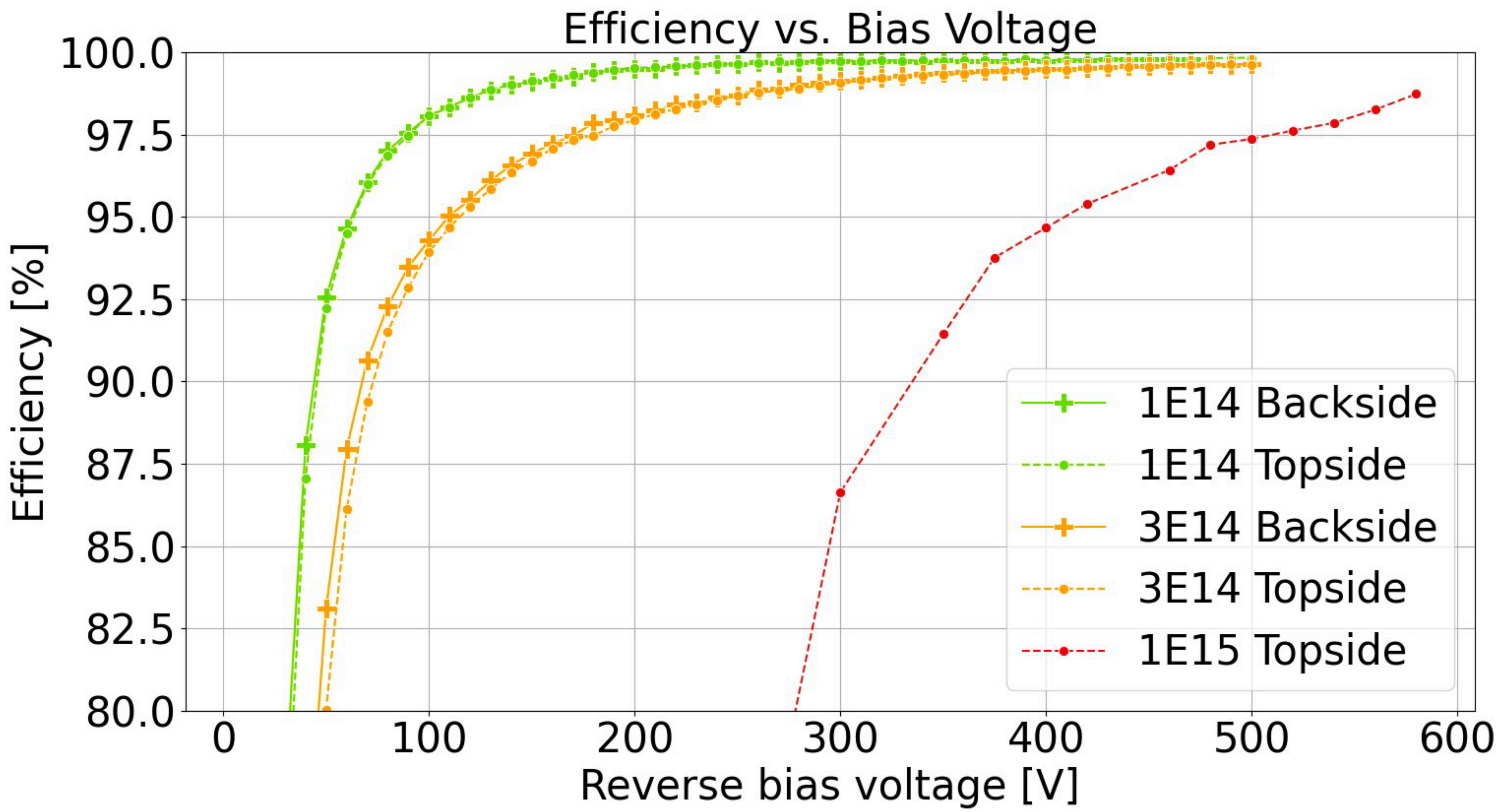






RD50-MPW4 - Testbeam after irradiation

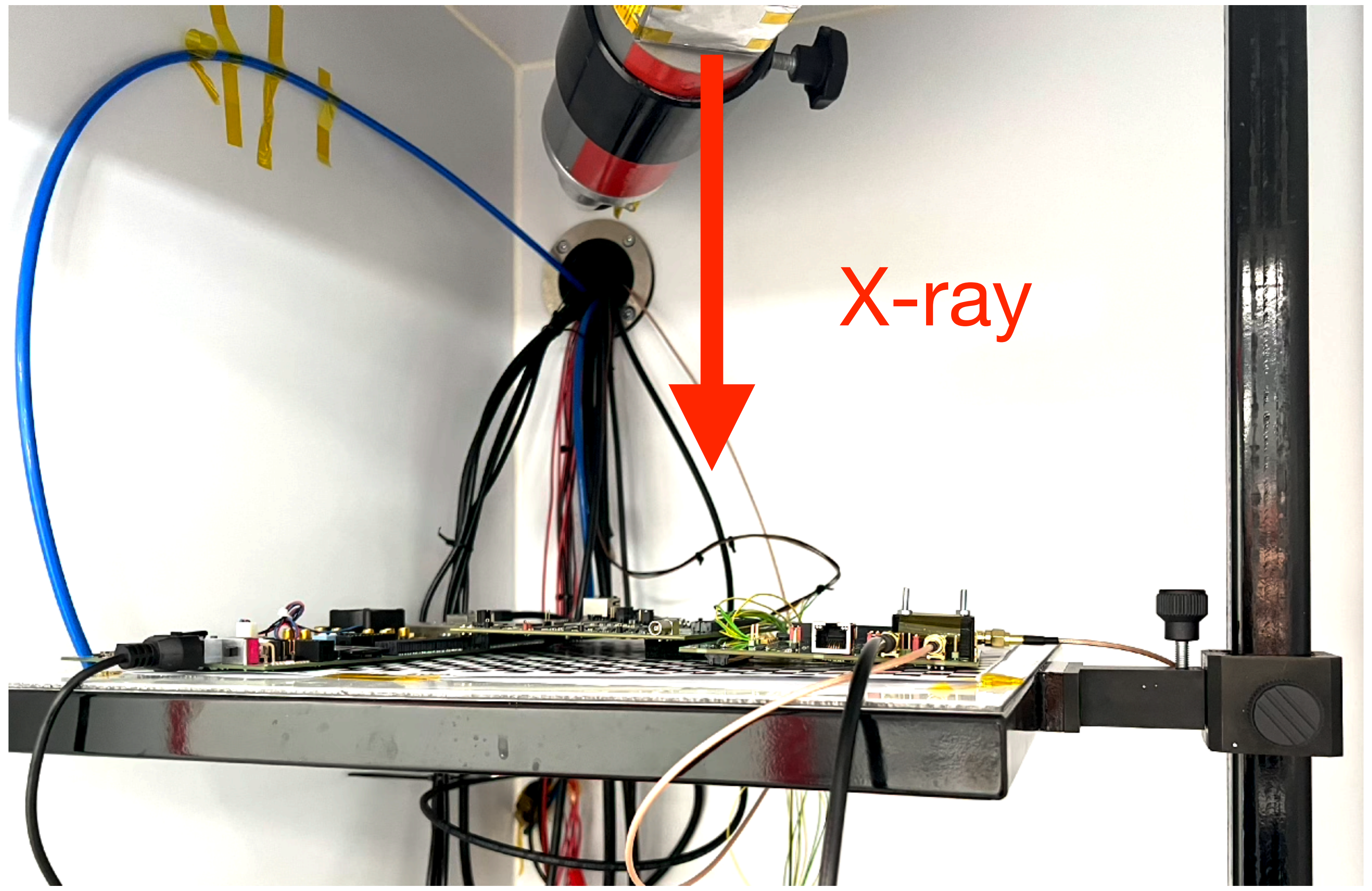
- Efficiency decreases with irradiation fluence, but recovers with higher bias voltage.
- Difference between topside bias and backside bias is minimal → backside processing may already affects the substrate.
- Need to disentangle the effect of backside processing → test more samples with no backside processing.
- A second irradiation campaign at more intermediate fluences: 5E14, 1E15, 2E15, 3E15, 5E15, on samples with/without backside processing → **A new testbeam at DESY in June 2025**.

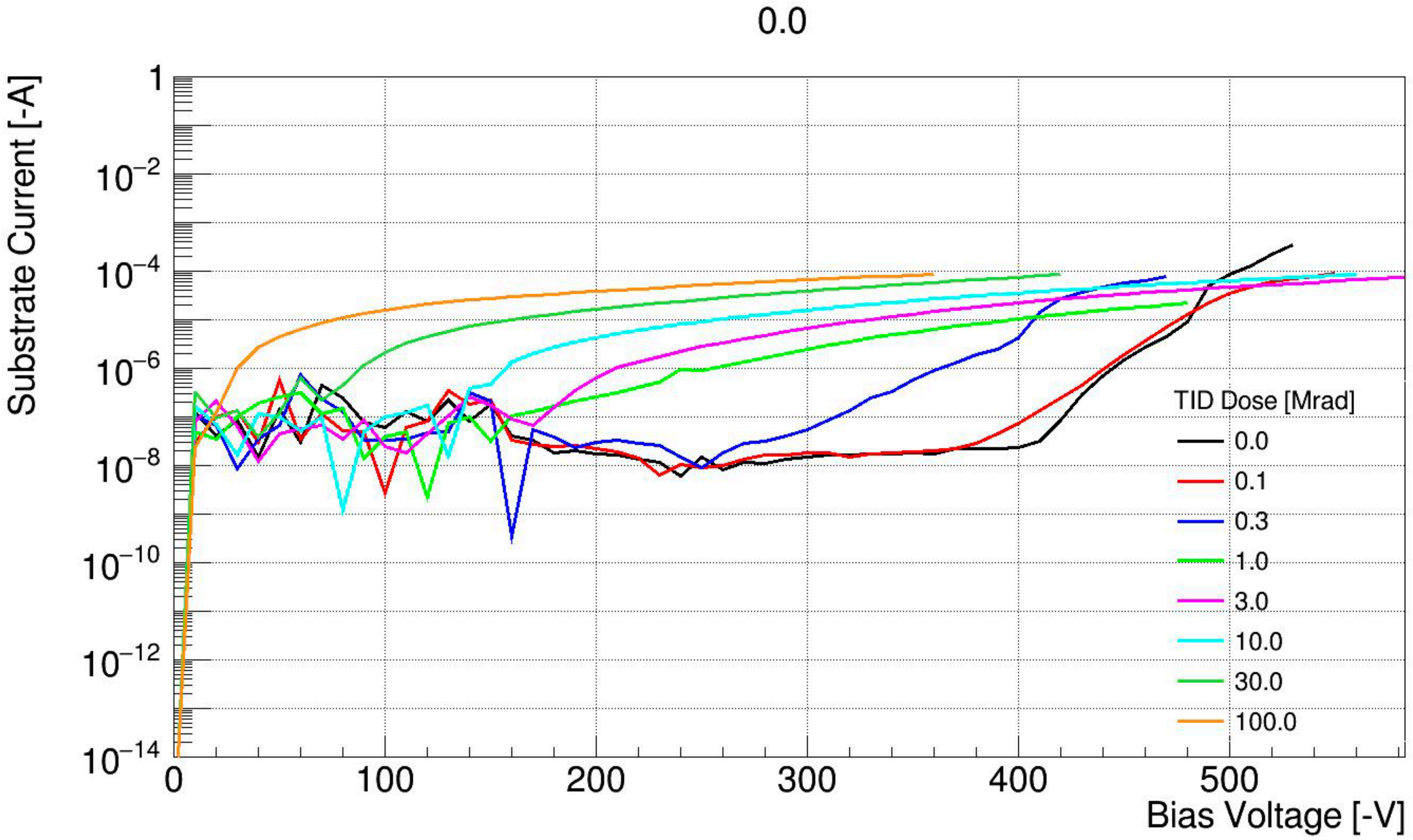


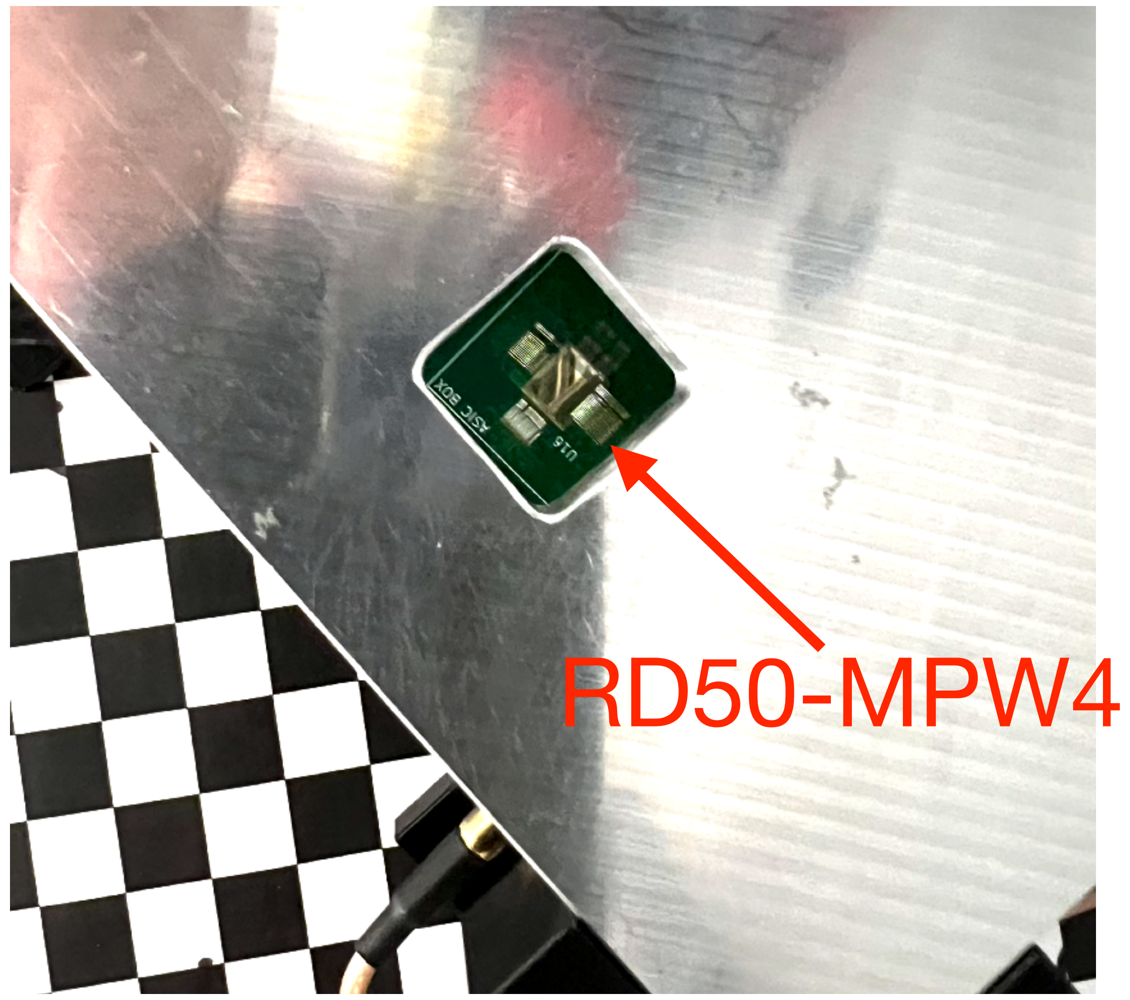
1E14 and 3E14 samples are backside processed, 1E15 sample is not backside processed.

TID measurements

- Total Ionising Dose (TID) measurement using X-ray machine in Oxford.
- Both UKRI-MPW1 and RD50-MPW4 were irradiated:
  - UKRI-MPW1 was biased, but not powered, leakage currents increased with X-ray dose.
  - RD50-MPW4 was biased and powered. The DAQ was protected by a 5 mm aluminium shield.
  - A few components on the DAQ were damaged by the X-ray, due to insufficient shielding. Second run with reinforced 20 mm shield.

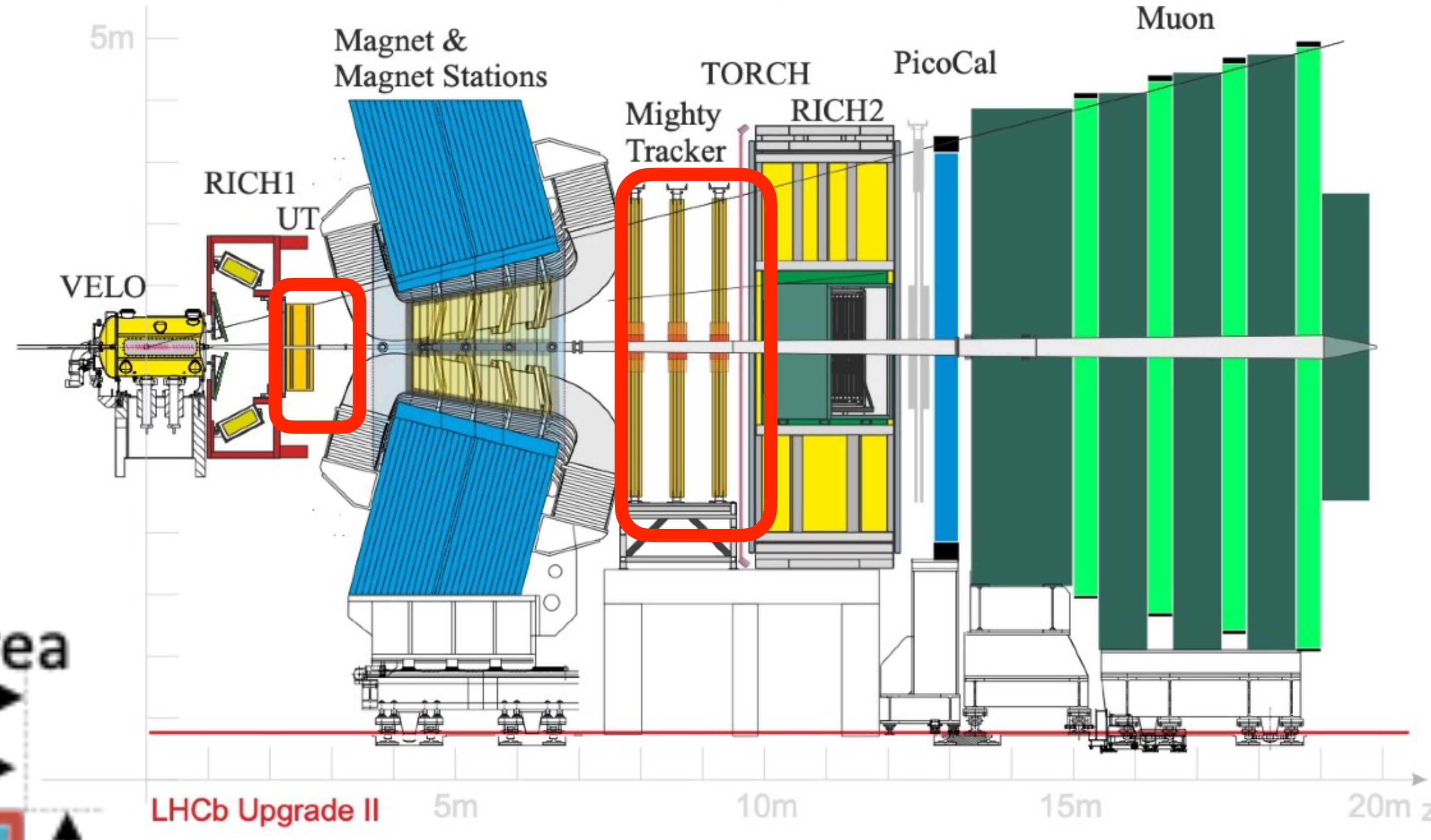






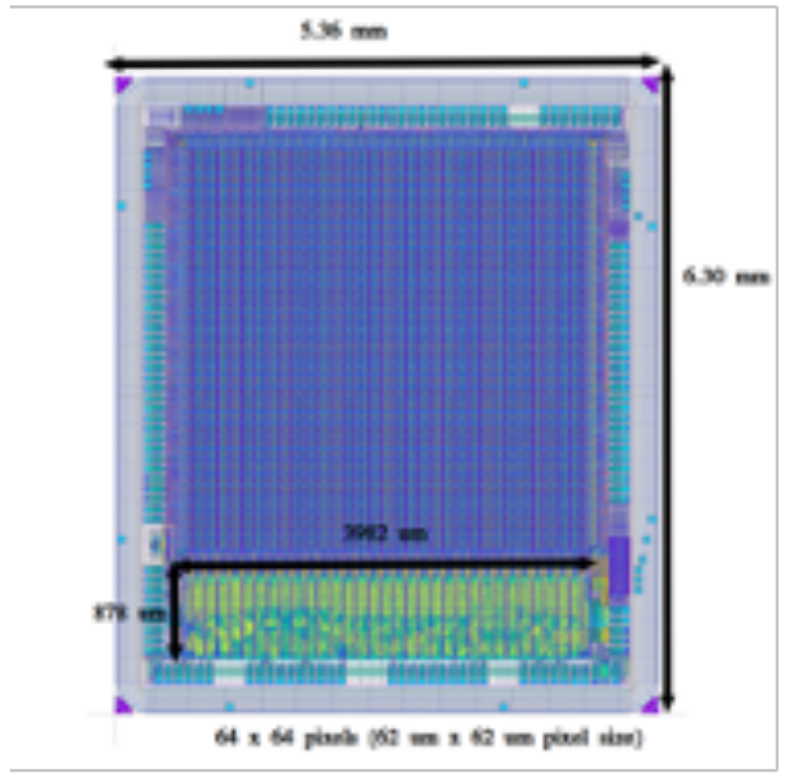
RadPix

- Based on RD50-MPW4, develop RadPix for LHCb Mighty Tracker and Upstream Tracker upgrade.



LHCb Upgrade II

RD50-MPW4
Lfoundry 150nm

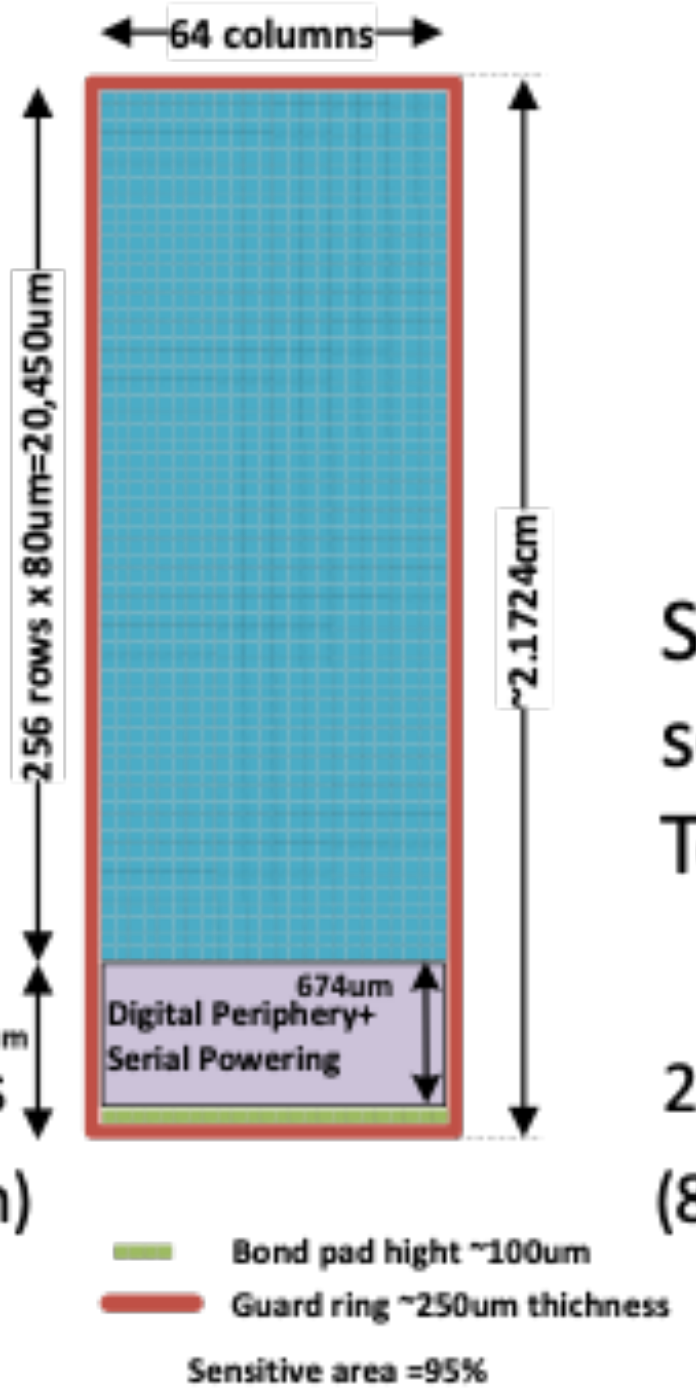


64 × 64 pixels
(62 µm × 62 µm)

Received in early 2024

Step 1- upgrade from RD50-MPW4 to RadPix

RadPix1
¼ of the final Radpix Lfoundry 150nm

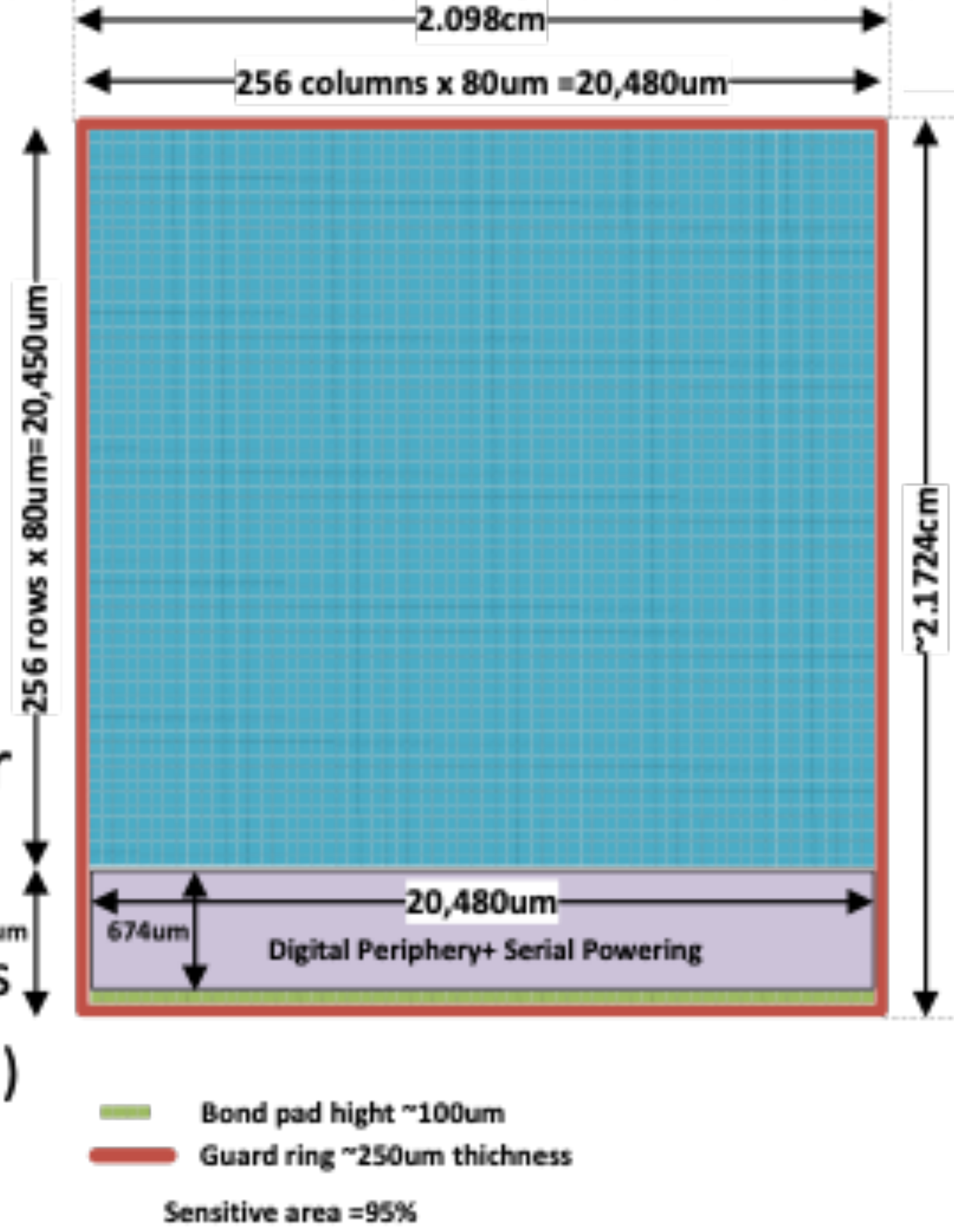


256 × 64 pixels
(80 µm × 80 µm)

To be submitted in Nov. 2025

Step 2
scale up
To full sensor

RadPix2
Full size RADPIX with 95% sensitive area



256 × 256 pixels
(80 µm × 80 µm)

To be submitted in late 2026

RadPix design

- The Radpix sensor design is divided into few work packages:

Pixel Matrix:

- Optimisation of the Pixel array size and power consumption.
- Pixel size 80 µm × 80 µm, Matrix size 256 rows × 64 columns (¼ of full size for RadPix1)

Readout Periphery:

- RTL description of the digital readout periphery + P&R
- LVDS transmitter and receiver.
- Power-On-Reset block.

Voltage Regulator:

- Design of Shunt LDOs for serial powering.

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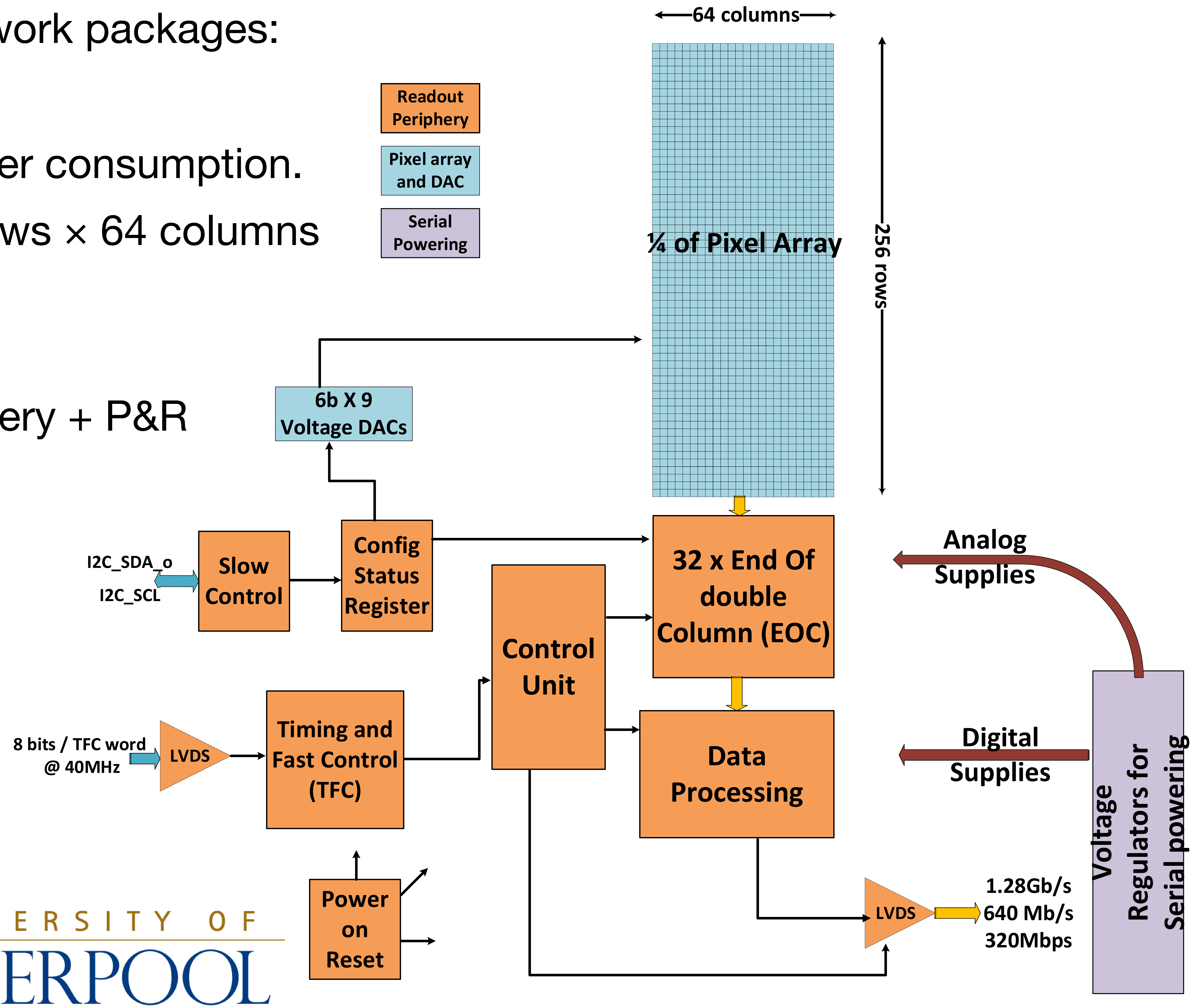
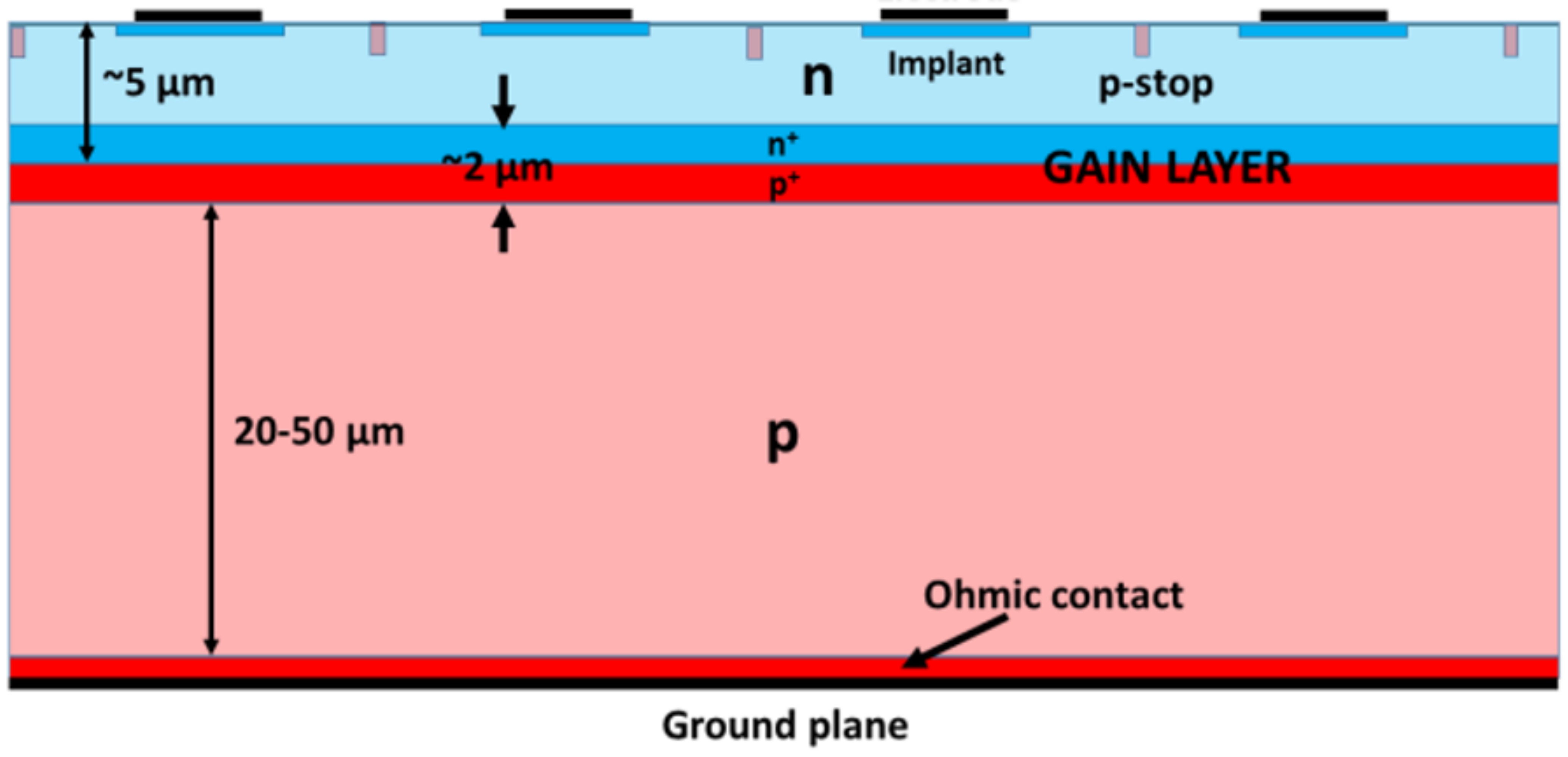
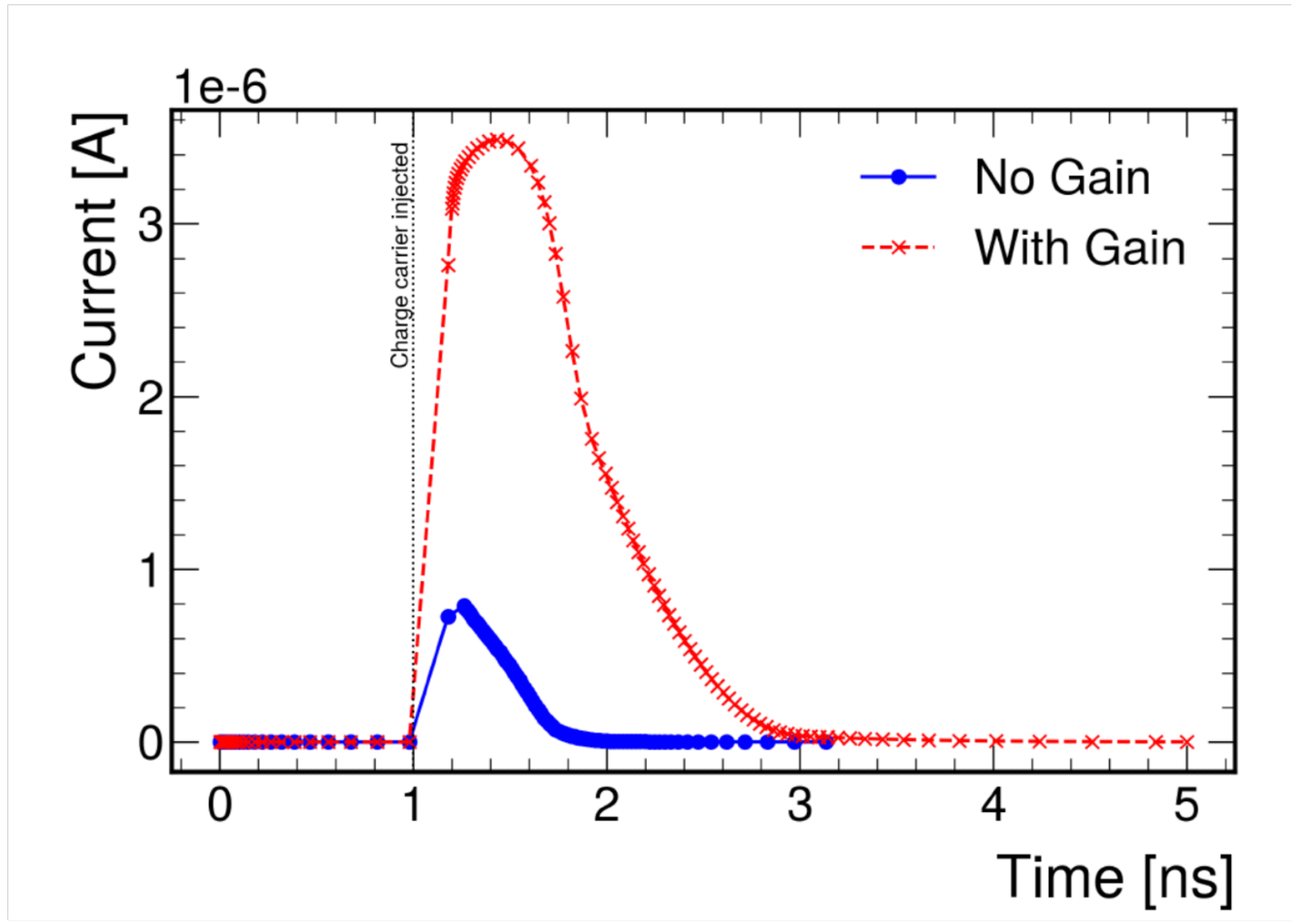


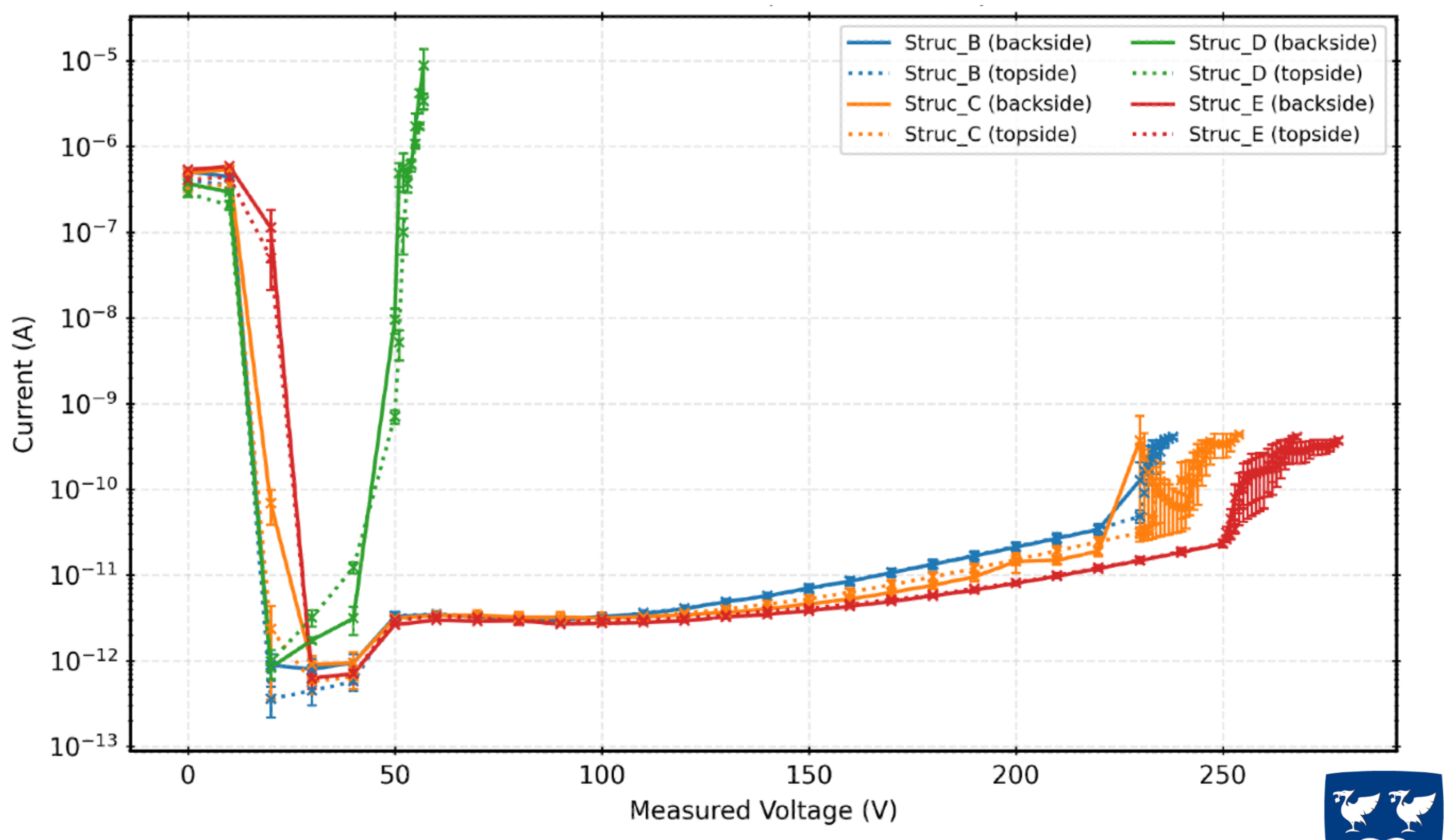
HV-CMOS + LGAD

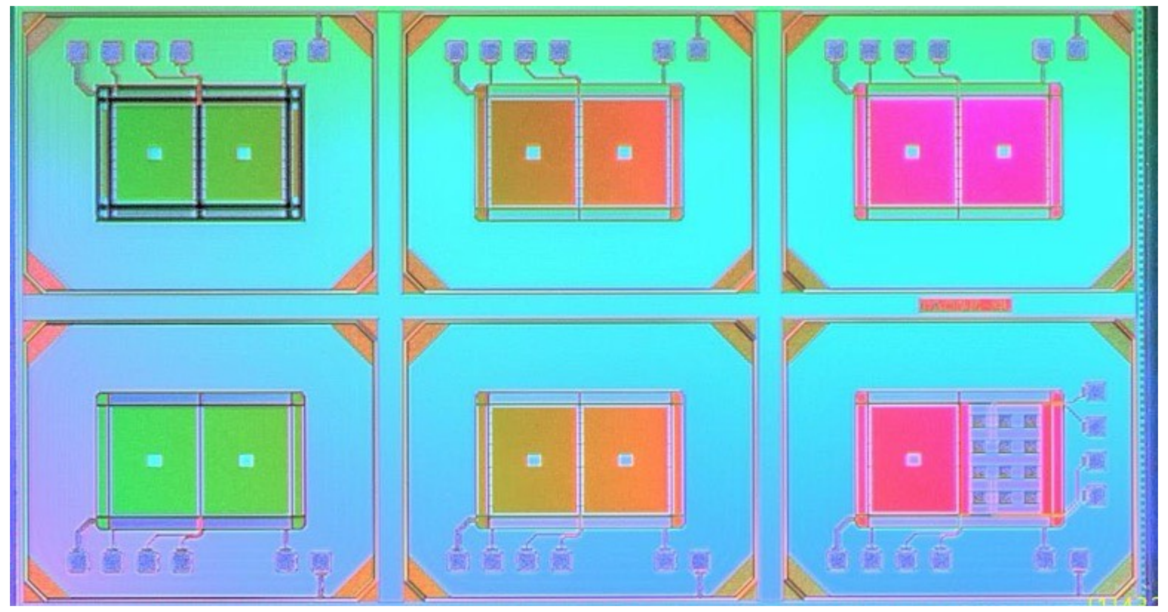
Cactus-GL:

- Incorporate a gain layer into HV-CMOS technology for pico-second time resolution.
- Charge injection TCAD simulation to observe amplification in current with the addition of gain layer.
- Taking I-V measurements of the fabricated Cactus-GL chip. Initial confirmation of a functional gain layer, with further testing to come.









Summary

- Six HV-CMOS prototypes have been developed in Liverpool, achieved high radiation tolerance (> 1e15 n_{eq}/cm^2).
- Designing RadPix for LHCb Mighty Tracker upgrade.