Design and characterisation of high-speed depleted monolithic active pixel sensor (DMAPS) detectors

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HEP Annual Meeting
Thursday, 19th December 2019

UNIVERSITY OF
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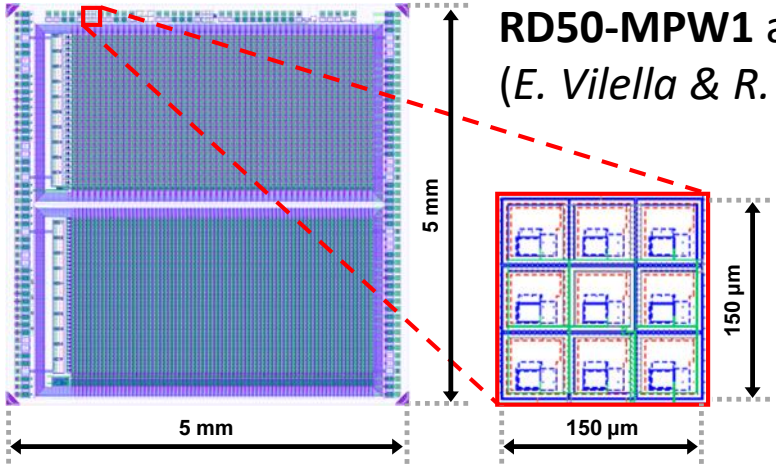
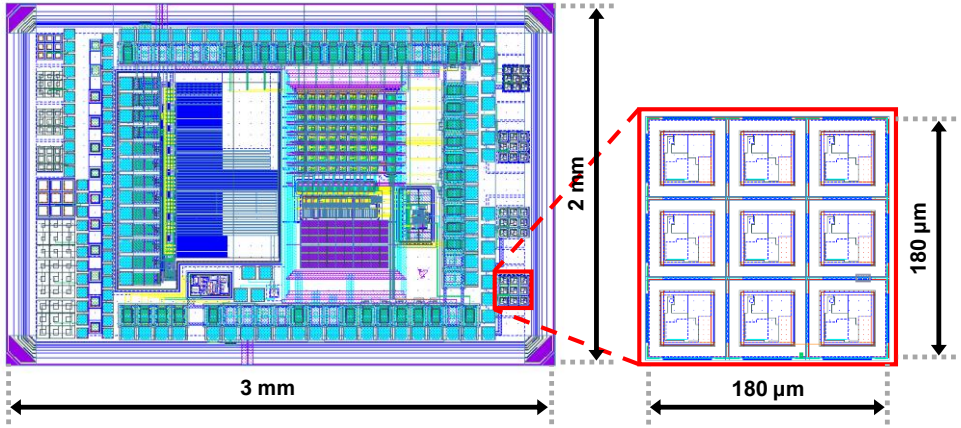
Outline

- Introduction
  - Timelines
  - RD50-MPW1 measurements
  - RD50-MPW2 submission
- **Breakdown voltage** (V_{BD}) simulations
  - Sensing diode electrode spacing
  - Pixel corner geometries
- Summary

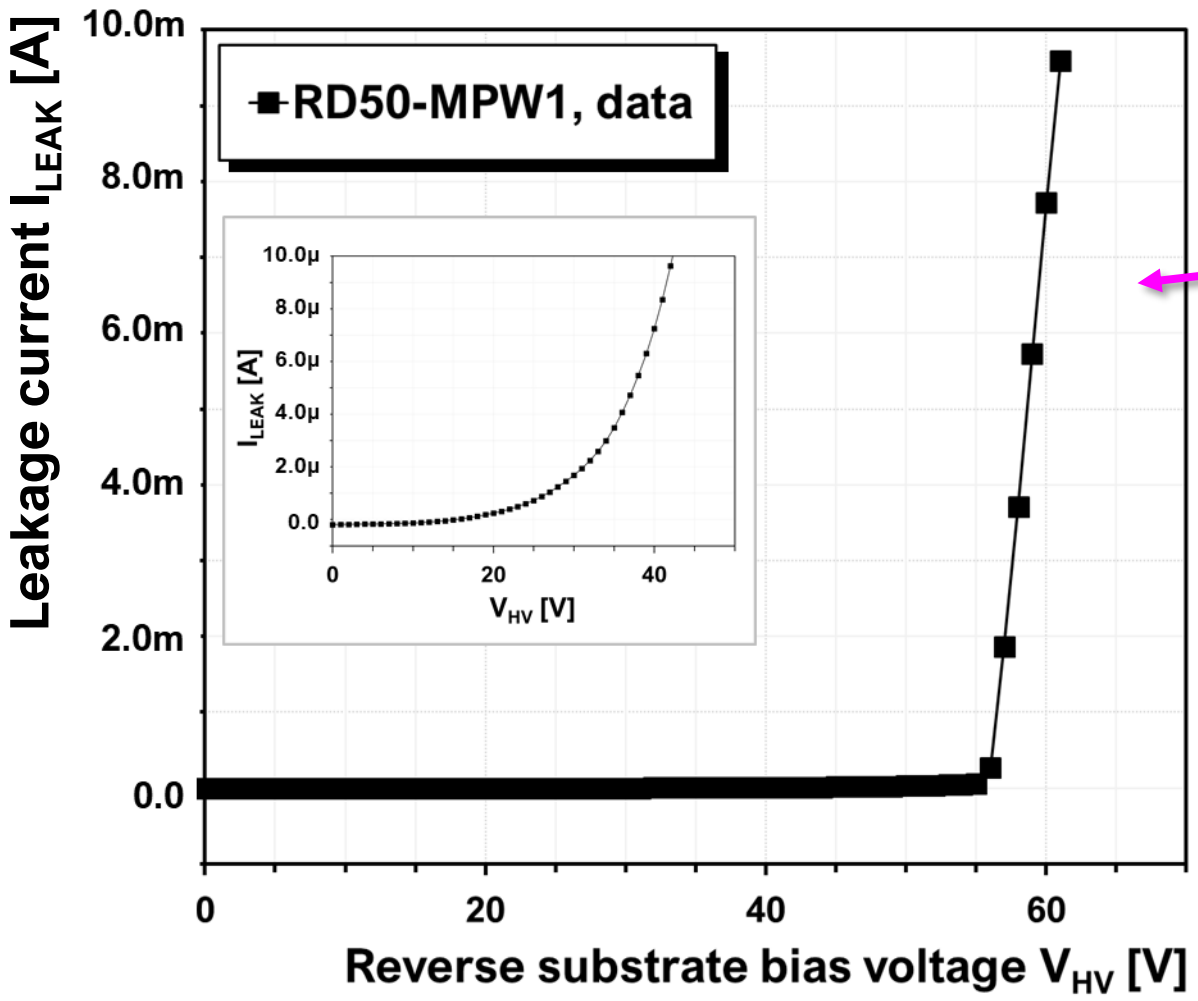


RD50-MPW1 and test structure (*E. Vilella & R. Casanova*)

RD50-MPW2 and test structure (*C. Zhang,* et al.)



Timeline



Nov 2017 — **RD50-MPW1** Submission (*E. Vilella*)

June 2017 — Test structure pixels suffer high leakage current (I_{LEAK}). Cause was investigated

Feb 2019 — **RD50-MPW2** Submission (*C. Zhang, M. Franks, S. Powell, E. Vilella,* & others)

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Jan 2020 — RD50-MPW2 due date. Testing can begin

Apr 2020? — **"RD50-MPW3"** submission? – Another Multi Project Wafer (MPW) in LFoundry technology

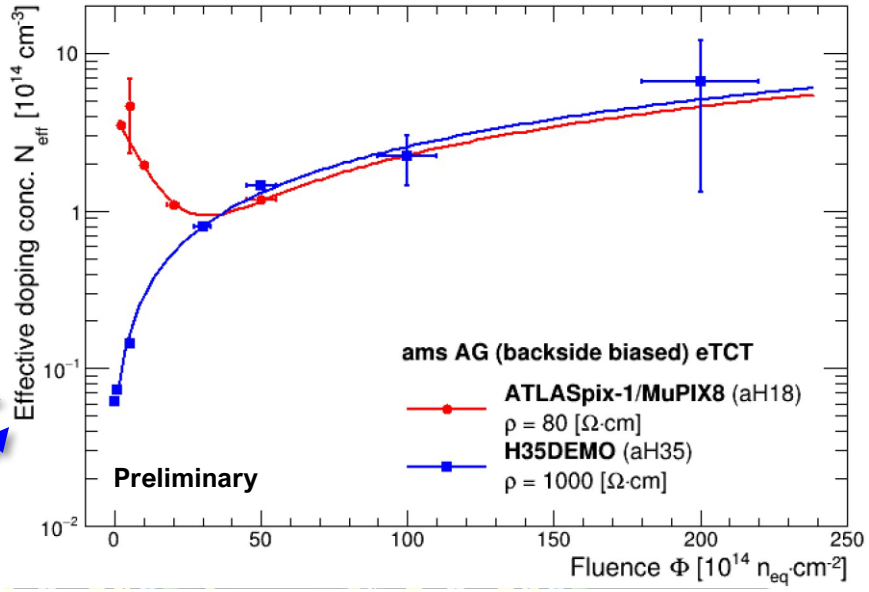
LFoundry "Engineering Run"?

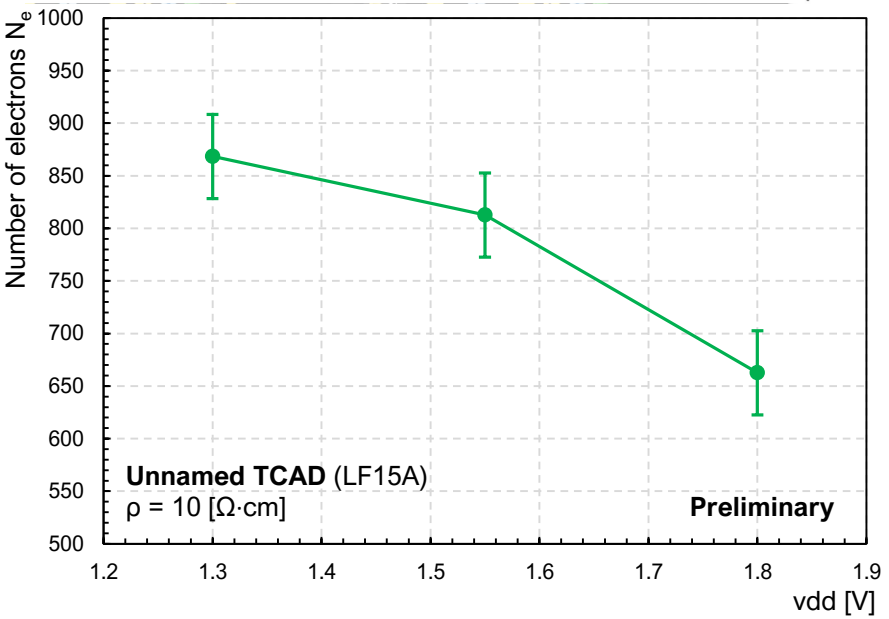
My 2019

- Jan — RD50-MPW2 TCAD simulations
- Feb — RD50-MPW2 design work

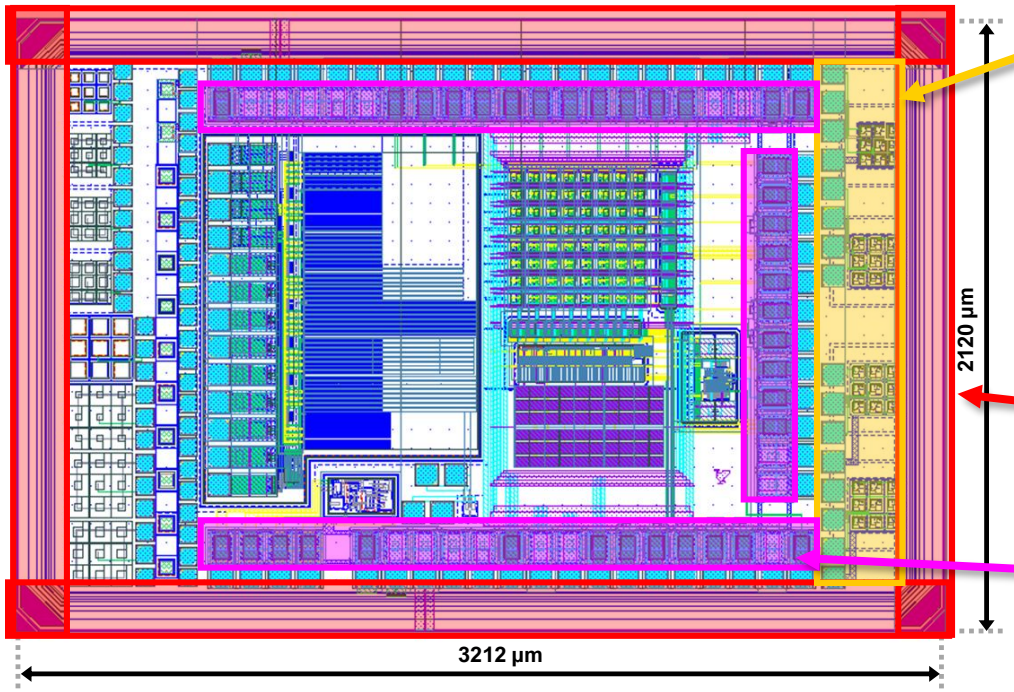
This talk

- Mar — ATLASpix-1/MuPIX8 eTCT measurements
- Apr — ATLASpix-1/MuPIX8 eTCT measurements
- May — ATLASpix-1/MuPIX8 eTCT measurements
- Jun — Unnamed TCAD simulations
- Jul — Unnamed TCAD simulations
- Aug — Unnamed TCAD simulations
- Sep — Unnamed TCAD simulations
- Oct — H35DEMO eTCT measurements
- Nov — H35DEMO eTCT measurements
- YOU ARE HERE → Dec — Unnamed design work





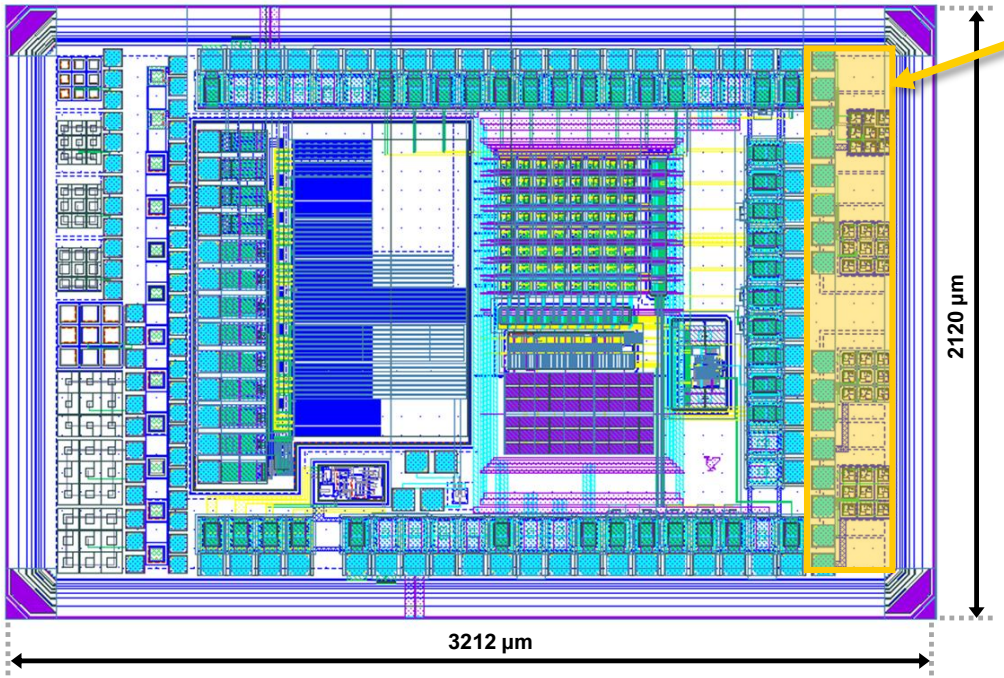
RD50-MPW2 my contributions



(above) RD50-MPW2 chip *(C. Zhang et al.)* Highlighted areas show my contributions **(red)** Guard rings included around the edge of the chip **(yellow)** Test structures for edge-TCT measurements **(pink)** Modified standard library pad diodes and analog buffers

- Four test structures for e-TCT and I-V measurements
  - 3µm rounded corners
  - 8µm rounded corners
  - 8µm chamfered corners
  - 8µm square corners
- Included guard rings at the edge of the device
  - Improve leakage current problem
- Modified standard library pad diodes and analog buffers
  - Chamfered corners to improve breakdown voltage
  - Careful placement of “blocking layers” to improve leakage current

RD50-MPW2 my contributions



(above) RD50-MPW2 chip *(C. Zhang et al.)* Highlighted areas show my contributions **(red)** Guard rings included around the edge of the chip **(yellow)** Test structures for edge-TCT measurements **(pink)** Modified standard library pad diodes and analog buffers

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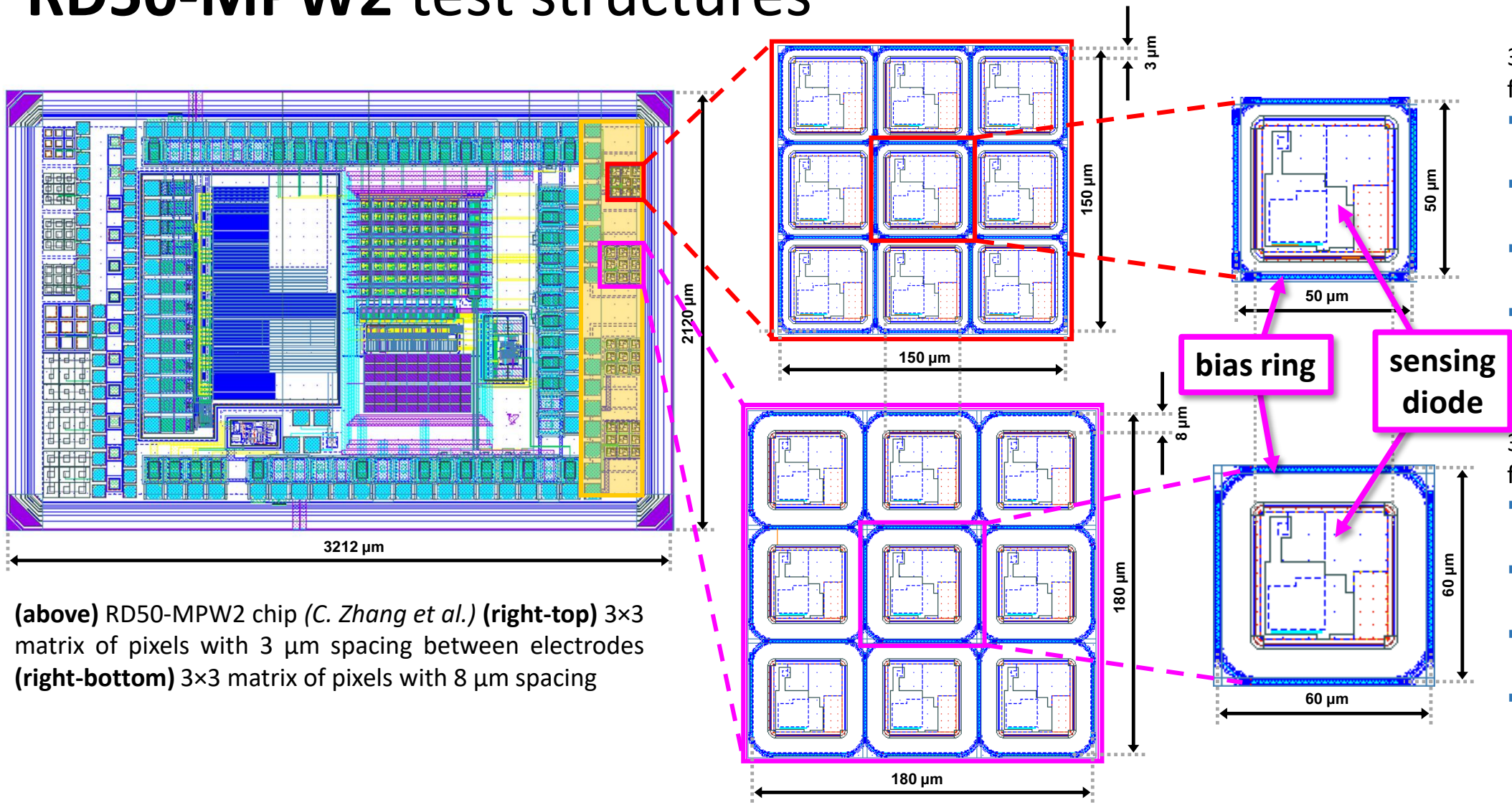
RD50-MPW2 test structures



(above) RD50-MPW2 chip *(C. Zhang et al.)* **(right-top)** 3×3 matrix of pixels with 3 µm spacing between electrodes **(right-bottom)** 3×3 matrix of pixels with 8 µm spacing

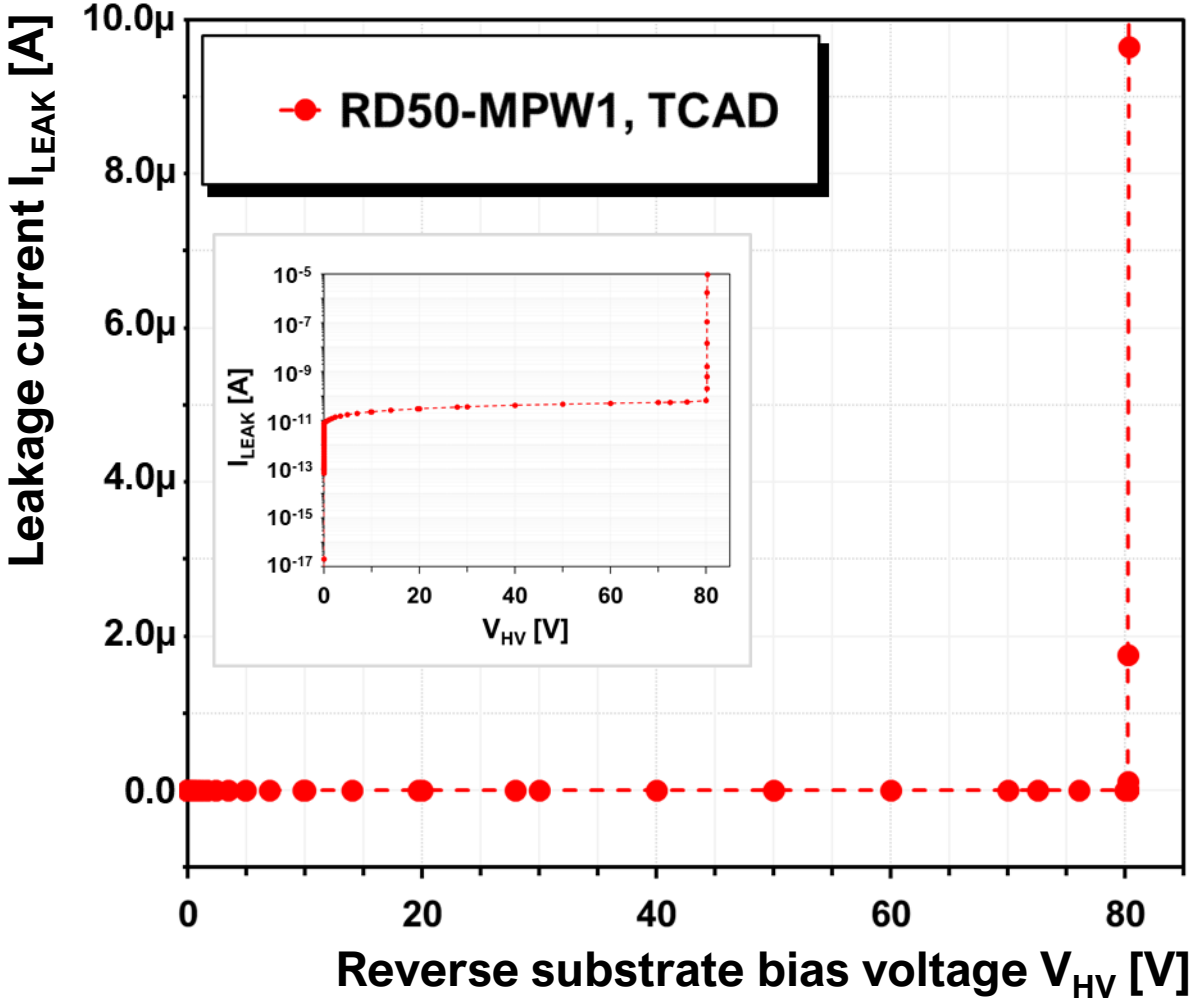
3 × 3 matrix of pixels for edge-TCT

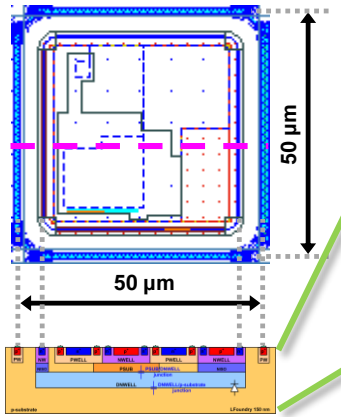
- 50 µm × 50 µm pixel area
- **3 µm electrode spacing**
- Rounded corners (see next section)
- No readout electronics

3 × 3 matrix of pixels for edge-TCT

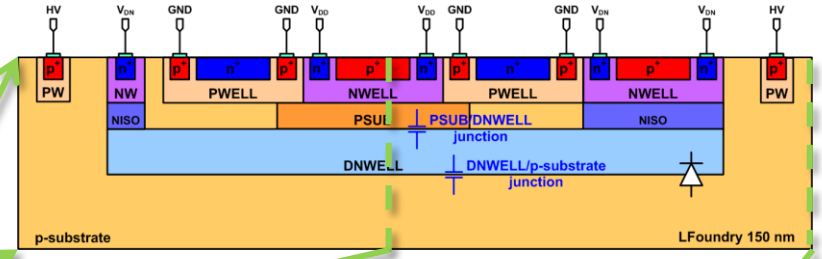
- 60 µm × 60 µm pixel area
- **8 µm electrode spacing**
- Rounded corners (see next section)
- No readout electronics

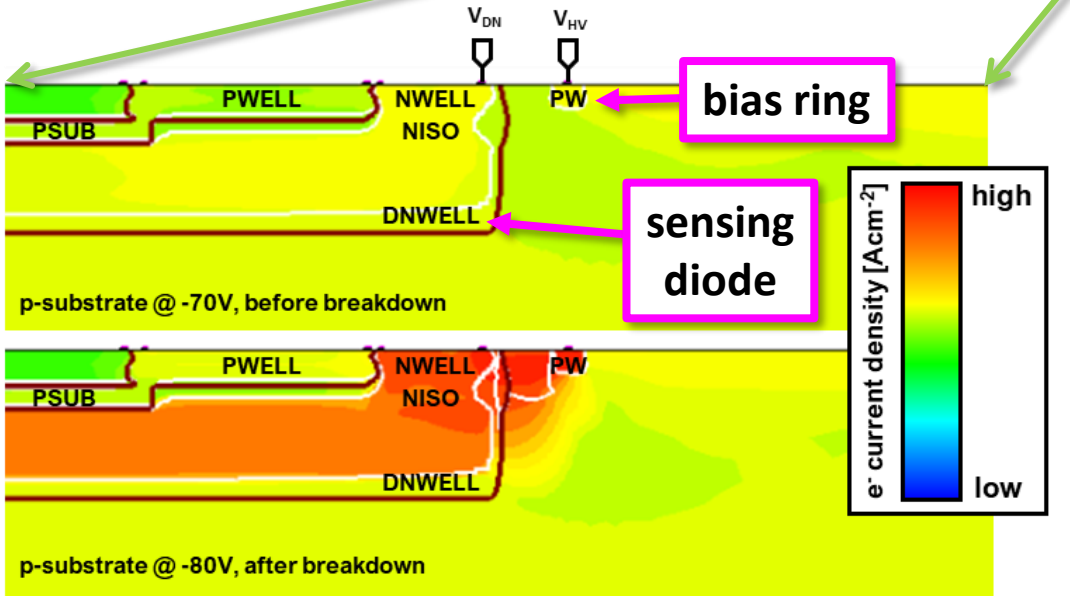
RD50-MPW1 breakdown voltage (V_{BD}) simulations





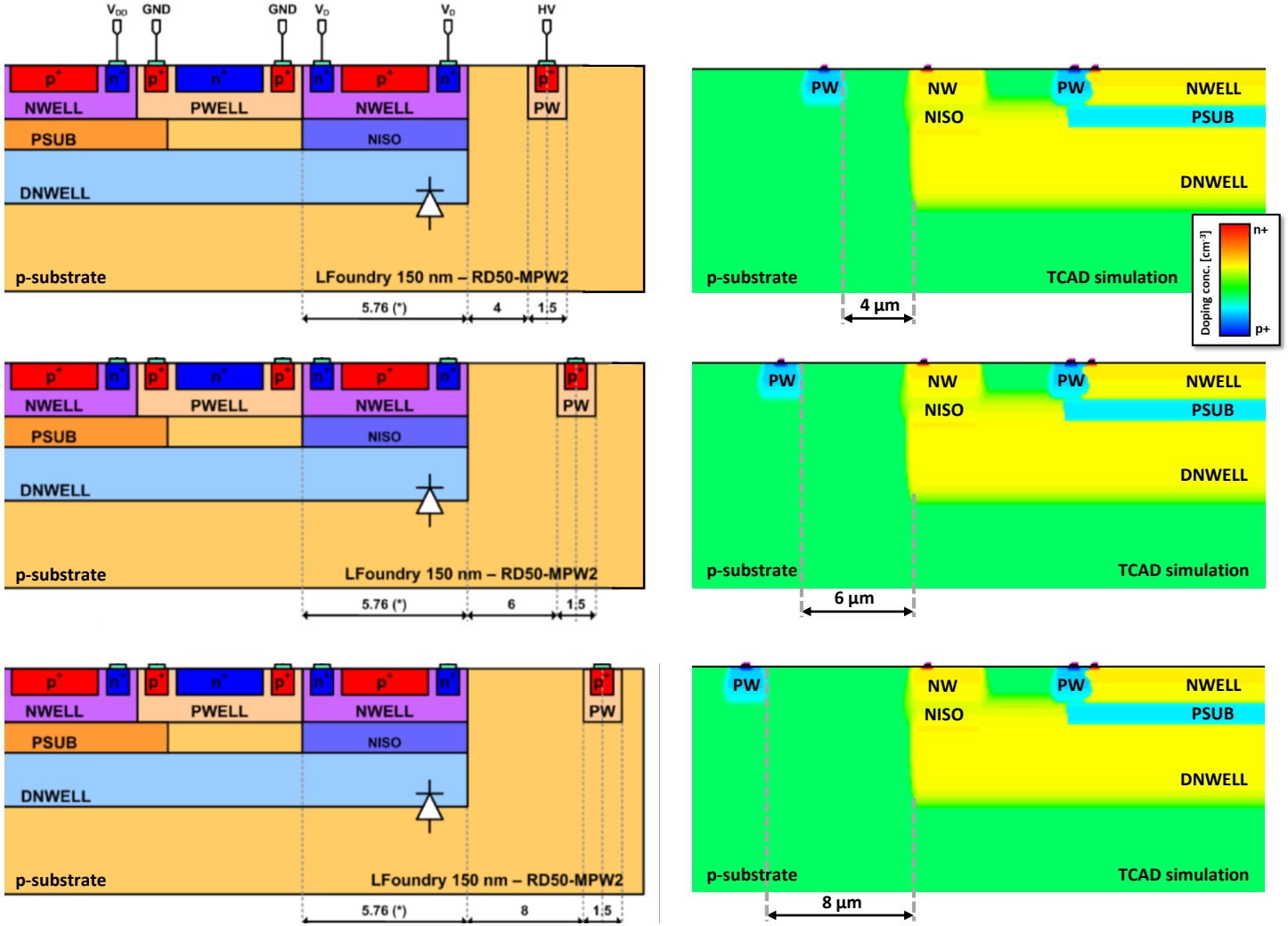
(left) Single pixel **(bottom-left)** Single pixel cross-section diagram **(below)** Zoomed in cross-section





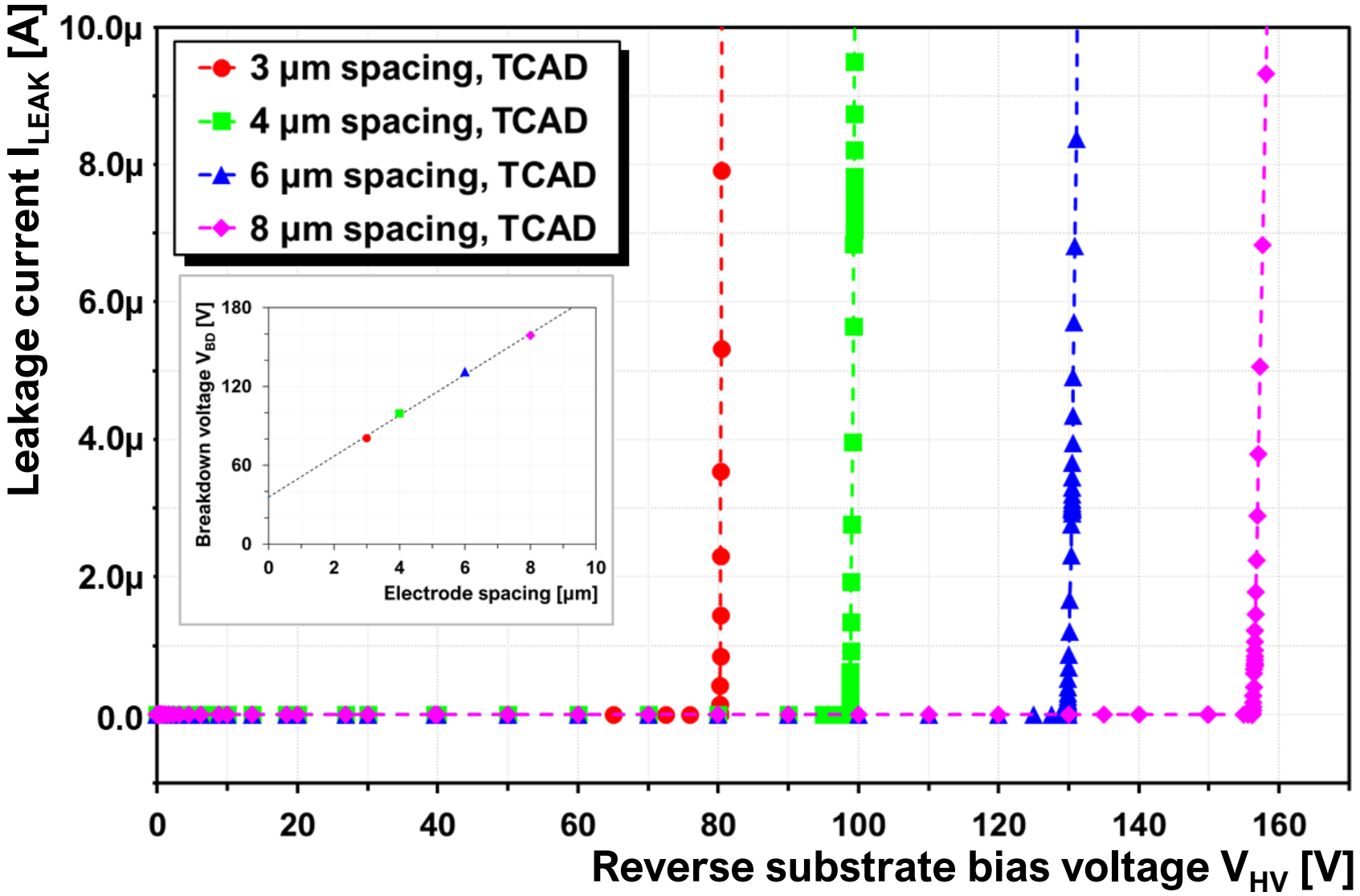
RD50-MPW2 breakdown voltage (V_{BD}) simulations

- Spacing between electrodes was increased from 3 µm (in **RD50-MPW1**) to:
  - 4 µm
  - 6 µm
  - 8 µm (in **RD50-MPW2**)
- Same breakdown simulations were performed to compare with 3 µm spacing

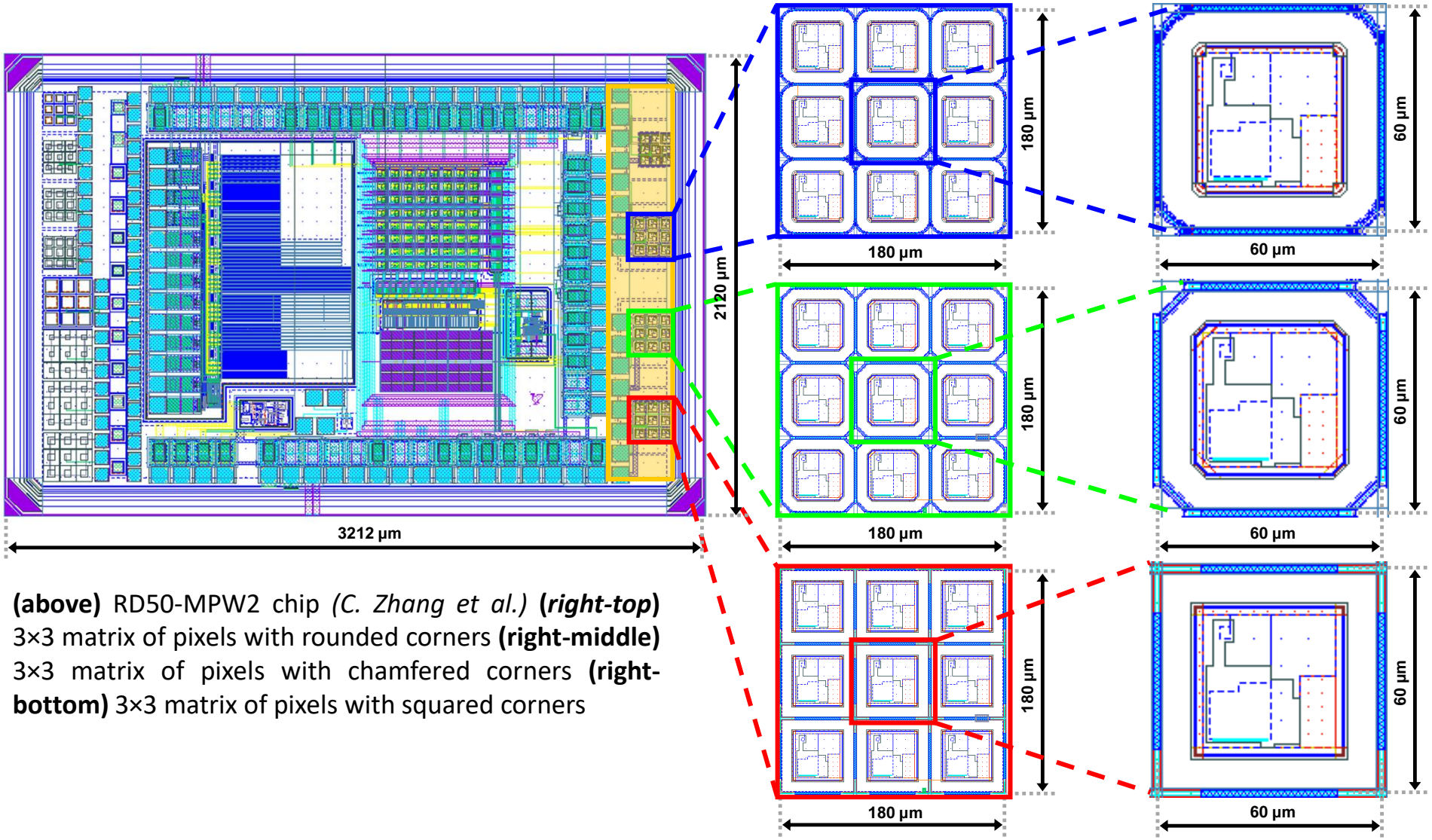


(left) E. Vilella, RD50-MPW2 planning presentation **(right)** TCAD simulations investigating the effect of increasing distance between sensing diode electrodes

RD50-MPW2 breakdown voltage (V_{BD}) simulations



RD50-MPW2 test structures



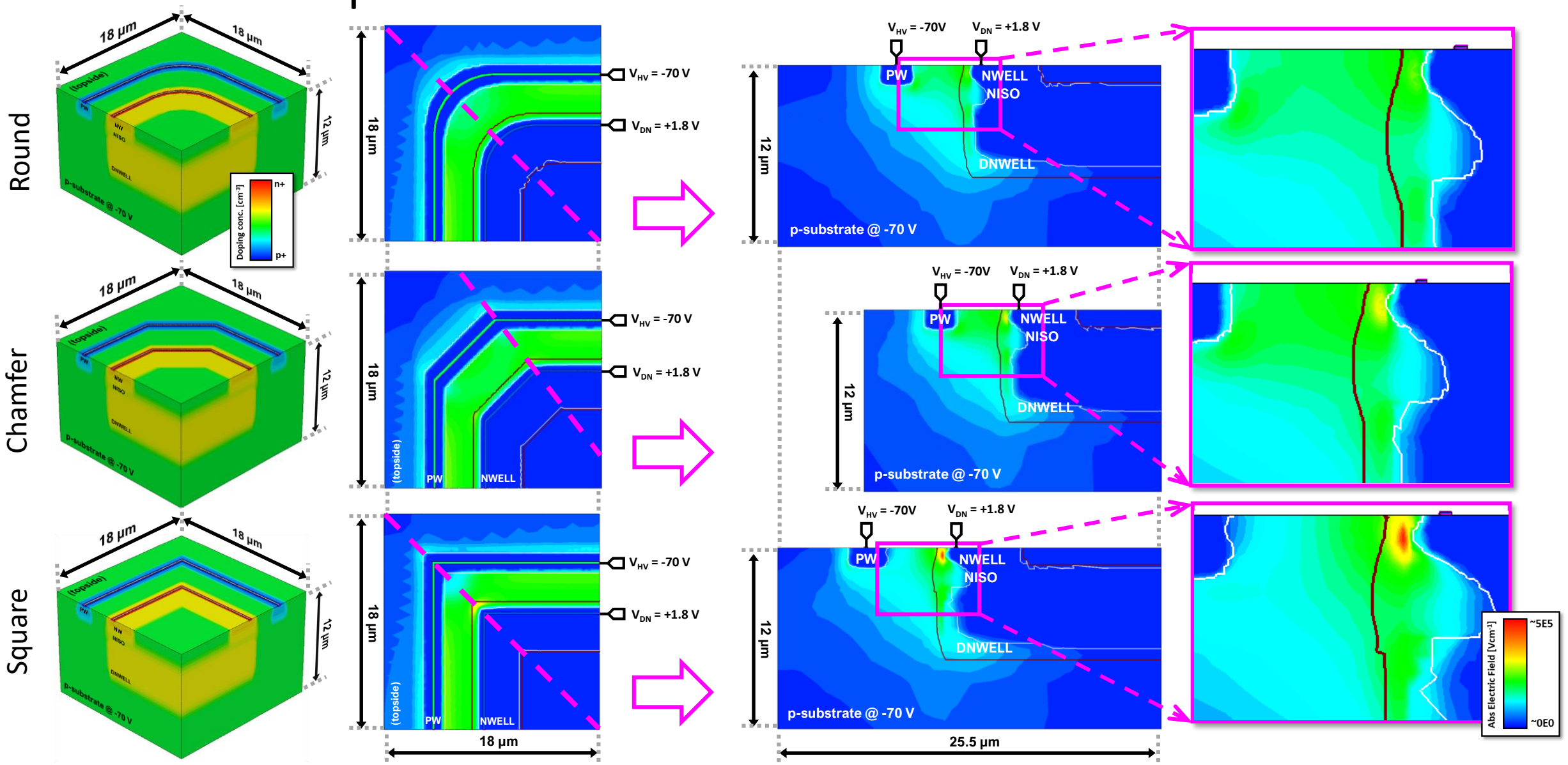
(above) RD50-MPW2 chip *(C. Zhang et al.)* **(*right-top*)** 3×3 matrix of pixels with rounded corners **(right-middle)** 3×3 matrix of pixels with chamfered corners **(right-bottom)** 3×3 matrix of pixels with squared corners

3 × 3 matrix of pixels for edge-TCT
- 60 µm × 60 µm pixel area
- 8 µm electrode spacing
- **Rounded corners**
- No readout electronics

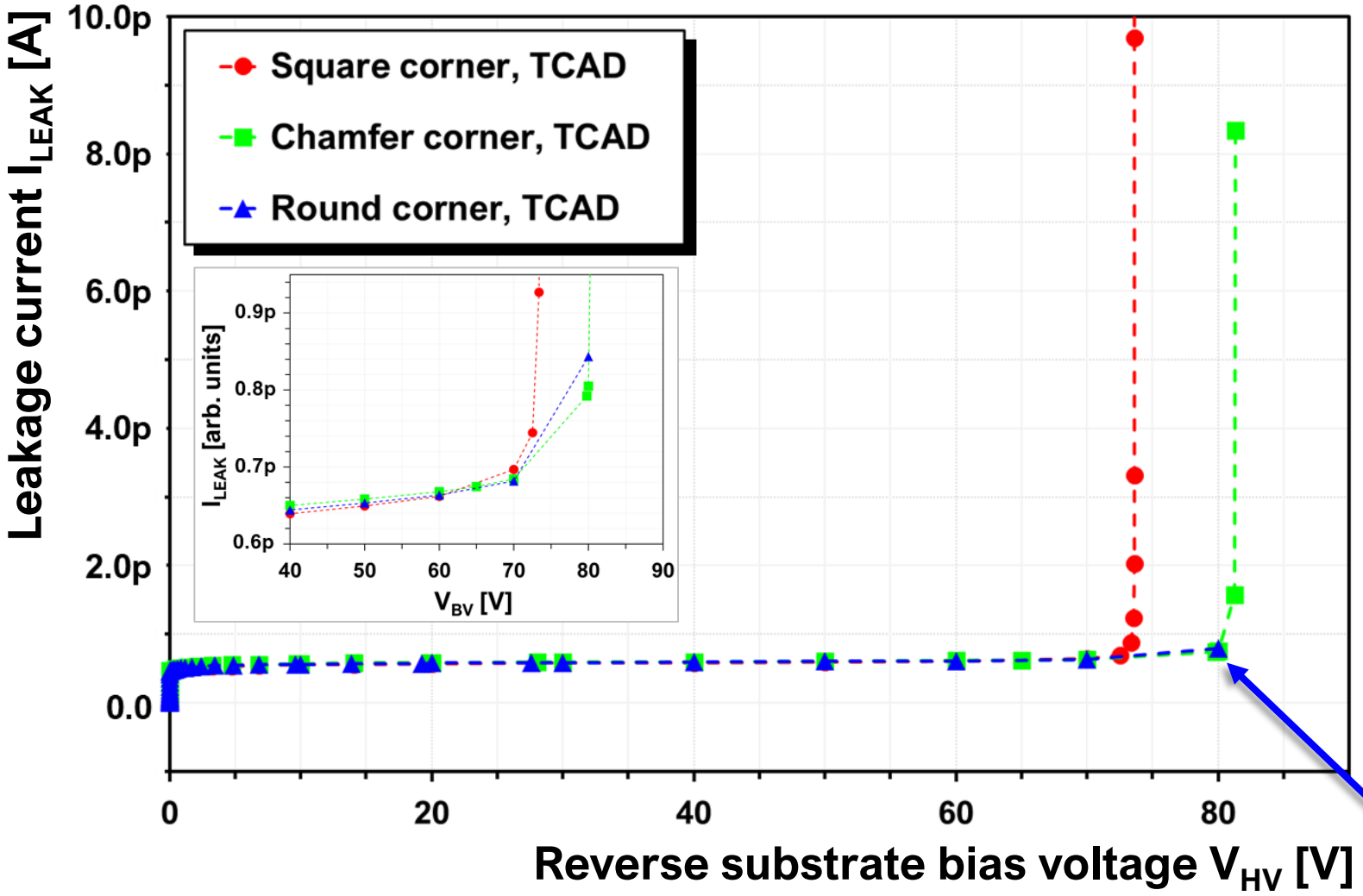
3 × 3 matrix of pixels for edge-TCT
- 60 µm × 60 µm pixel area
- 8 µm electrode spacing
- **Chamfered corners**
- No readout electronics

3 × 3 matrix of pixels for edge-TCT
- 60 µm × 60 µm pixel area
- 8 µm electrode spacing
- **Squared corners**
- No readout electronics

RD50-MPW2 pixel corner electric field simulations



RD50-MPW2 V_{BD} simulations I-V curves



Comparison of I-V curve of **square**, **chamfer**, and **round** corners:

- **Square** corners:
  - $V_{BD} \approx -70V$
- **Chamfer** corners:
  - $V_{BD} \approx -80V$
- **Round** corners:
  - $V_{BD} \approx -80V$

Round corners simulation ended abruptly

Summary

- Aims
  - Improve **leakage current** for RD50-MPW2 submission
  - Improve **breakdown voltage** for RD50-MPW2 submission
- RD50-MPW2 submitted Feb 2019
  - TCAD simulations of **electrode spacing** showed increase in breakdown voltage
  - TCAD simulations of **corner geometries** show increase in breakdown voltage
- RD50-MPW2 due to be shipped Jan 2020
  - Testing can begin

Backup slides

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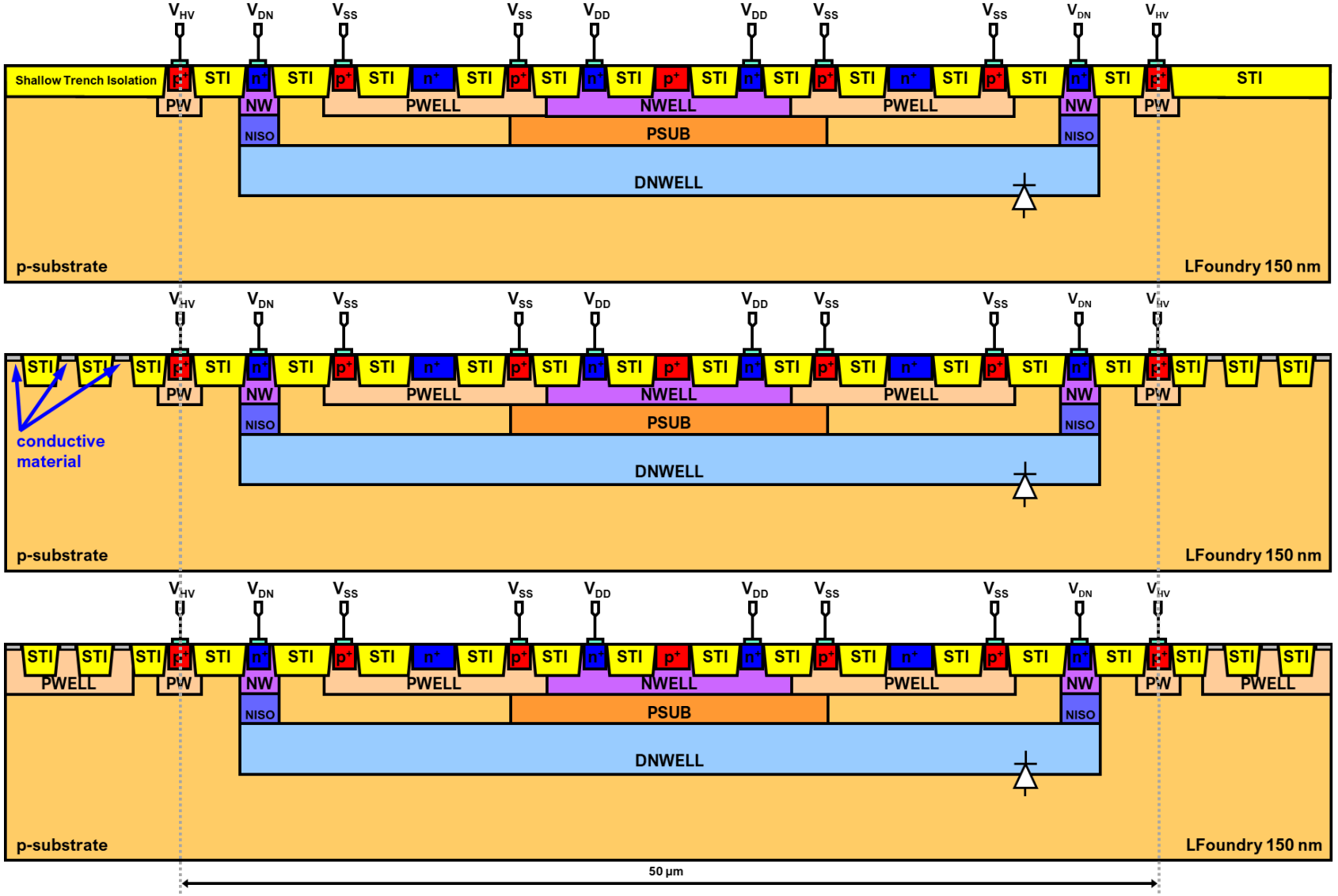
RD50-MPW1 leakage current (I_{LEAK}) simulations

"Ideal"

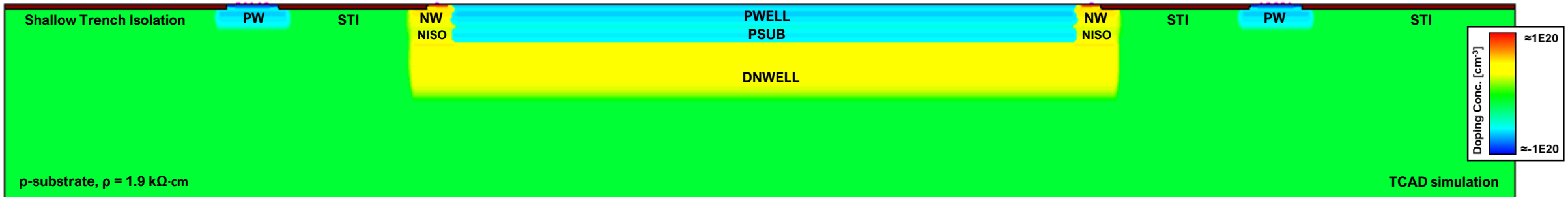
RD50-MPW1

RD50-MPW2

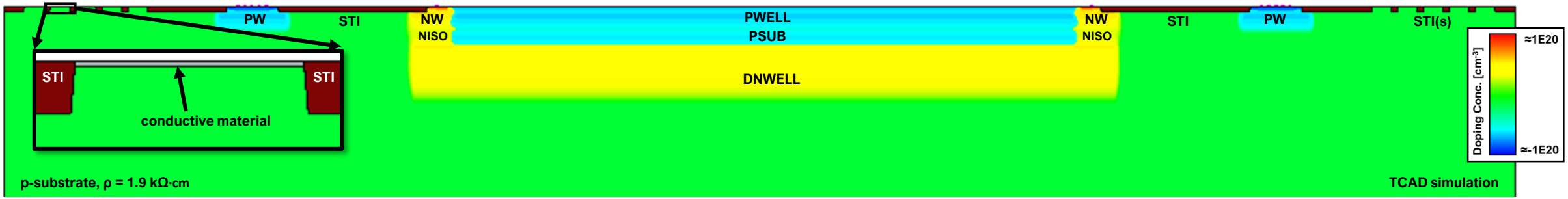


RD50-MPW1 leakage current (I_{LEAK}) simulations

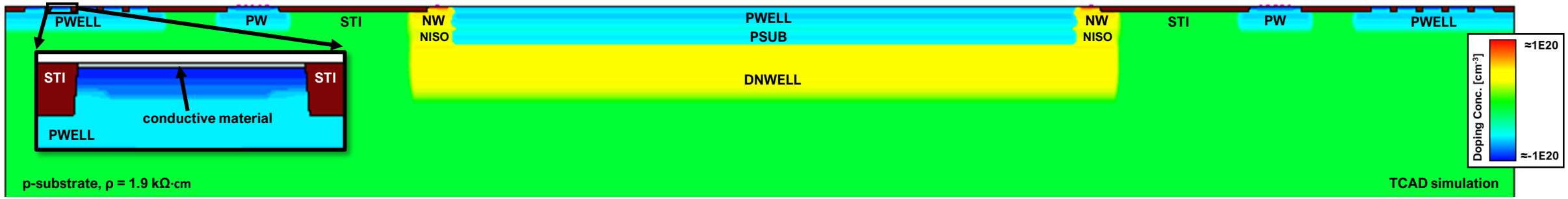
"Ideal"



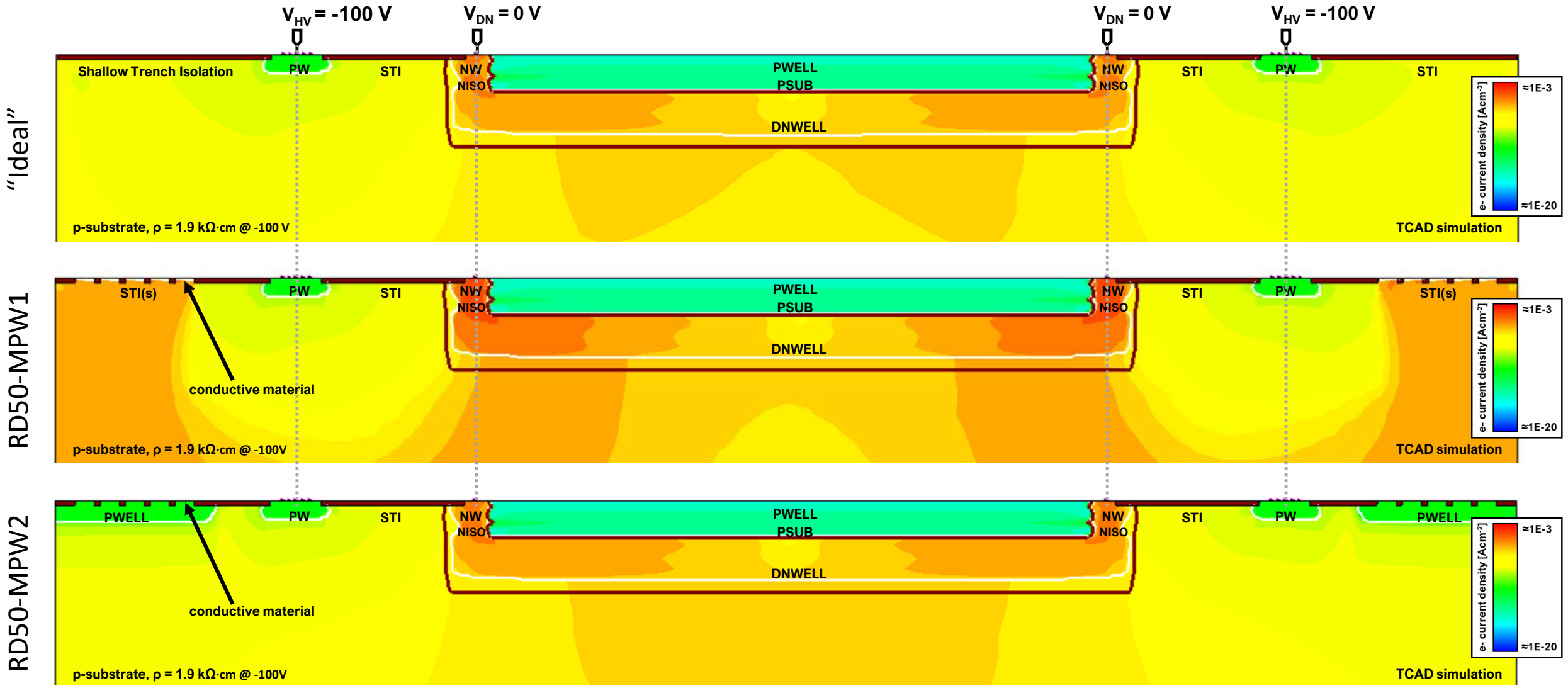
RD50-MPW1



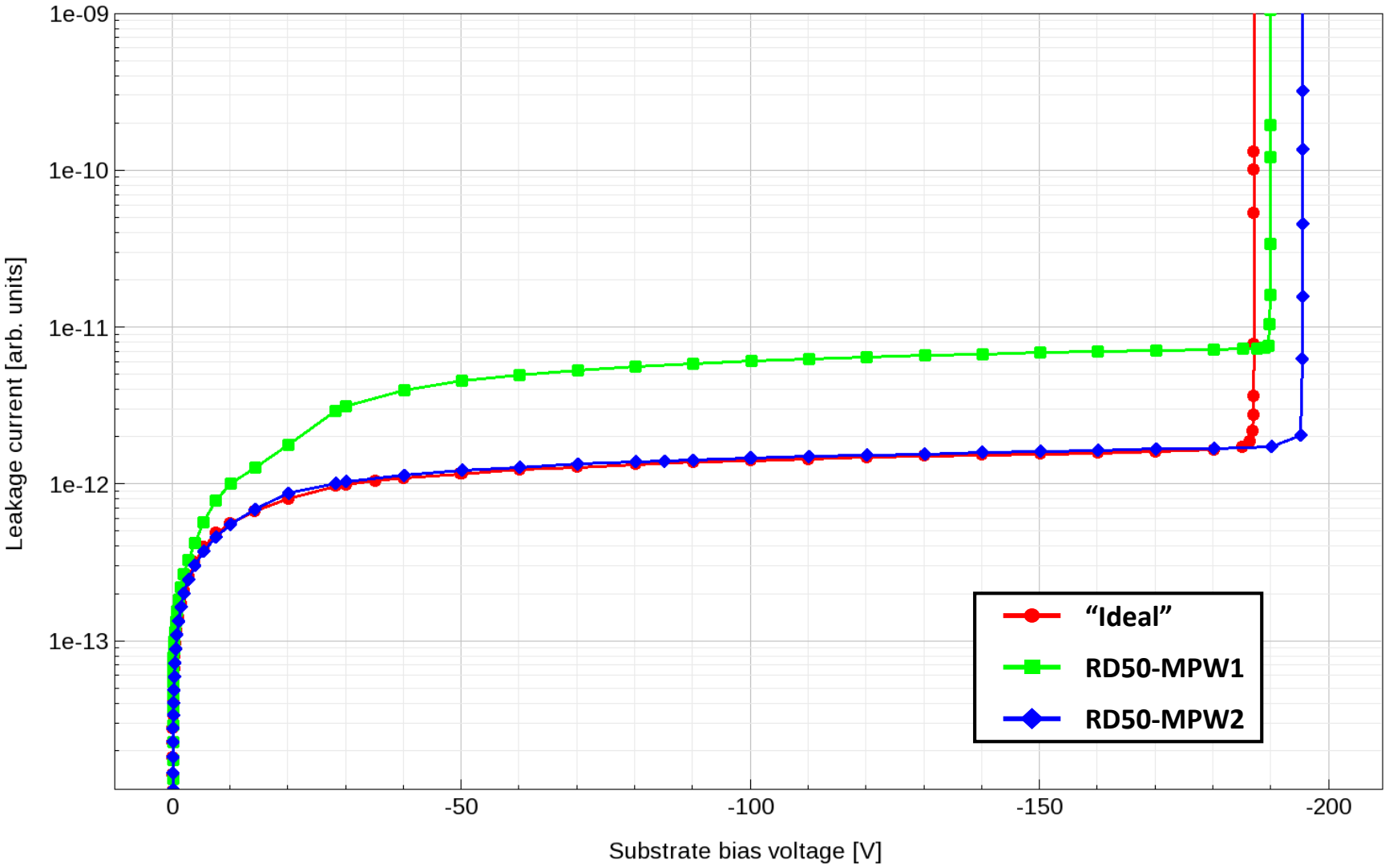
RD50-MPW2



RD50-MPW1 leakage current (I_{LEAK}) simulations



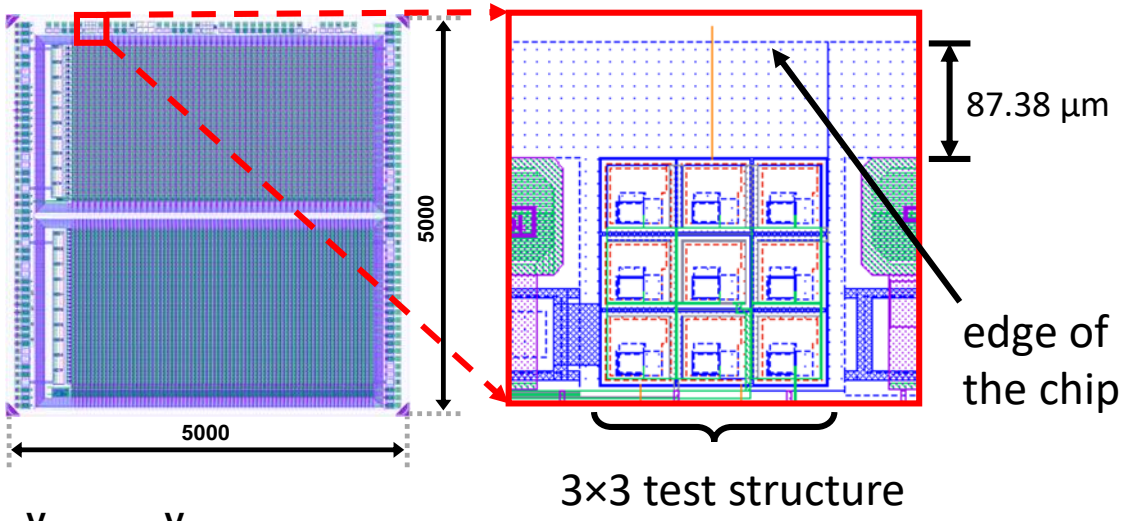
RD50-MPW1 leakage current (I_{LEAK}) simulations



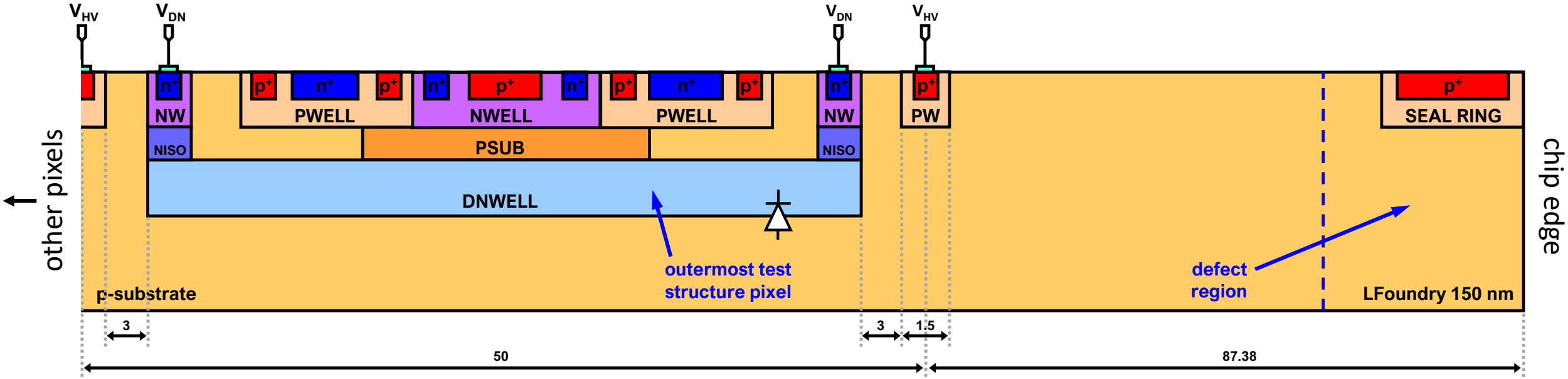
Comparison of I-V curves of the three simulations:

- Increase in I_{LEAK} when conductive material is present on the surface (**RD50-MPW1**)
- I_{LEAK} is reduced when conductive material is placed in PWELL (**RD50-MPW2**)

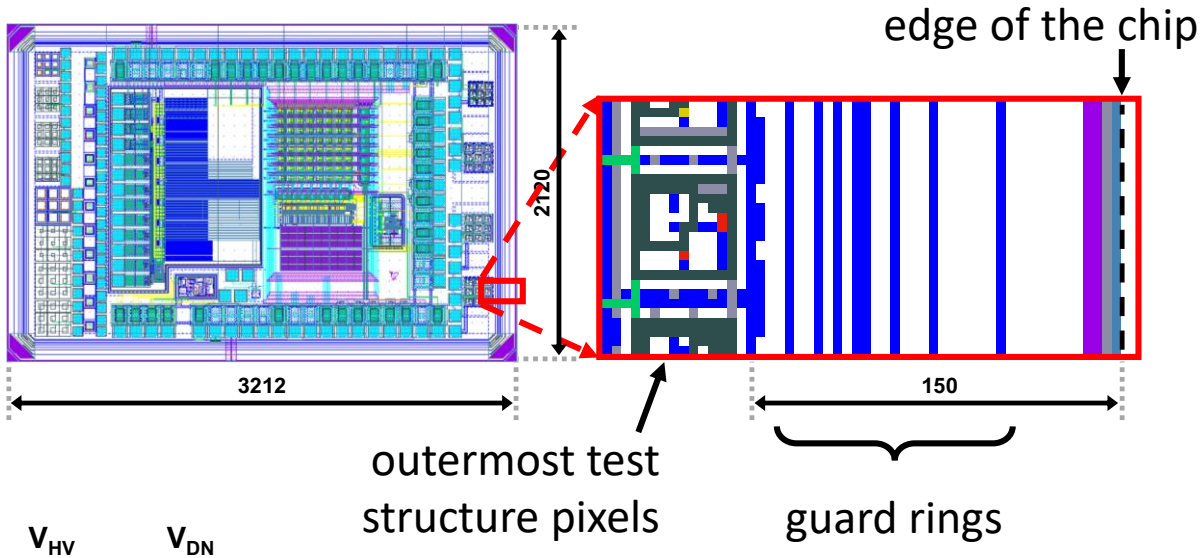
RD50-MPW1 leakage current due to edge defects



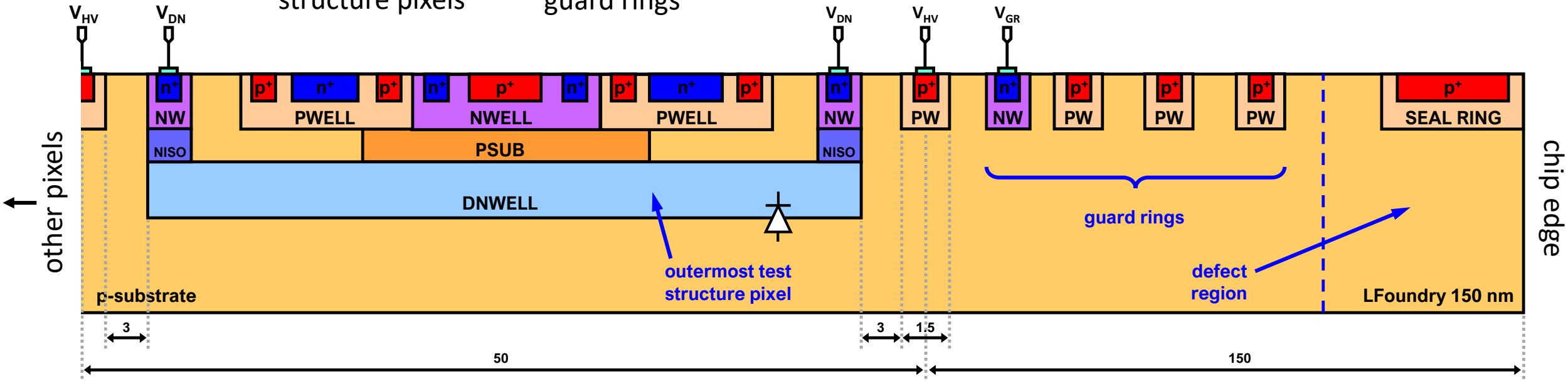
- Test structure lies close to the edge of the device
- Defects in silicon lattice **due to dicing** become significant
- Leakage current increases when pixel depletion region is near defect region



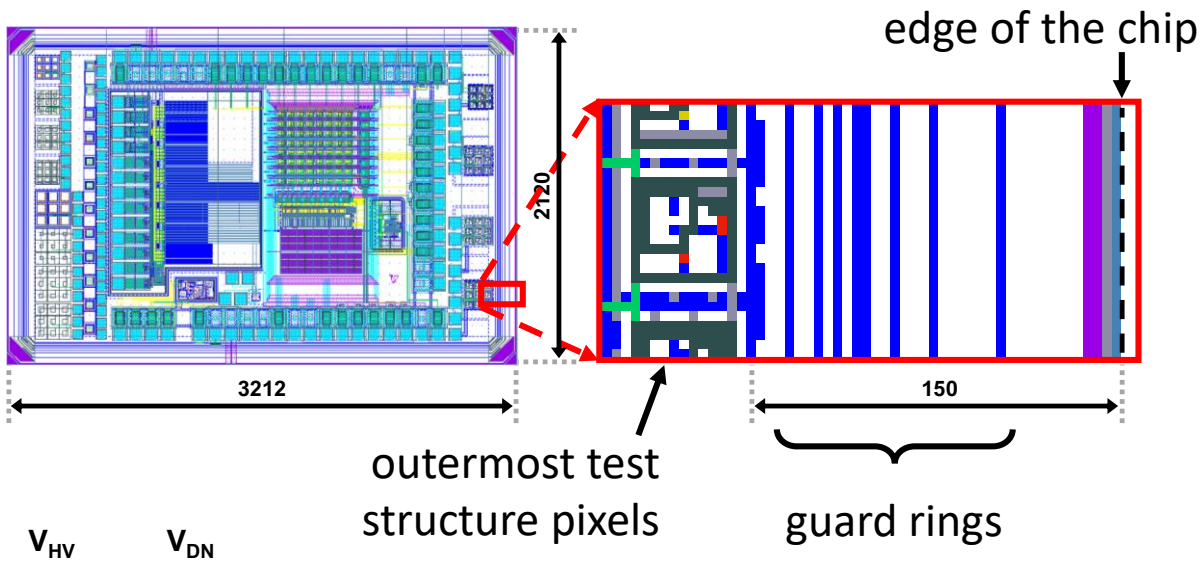
RD50-MPW2 guard rings



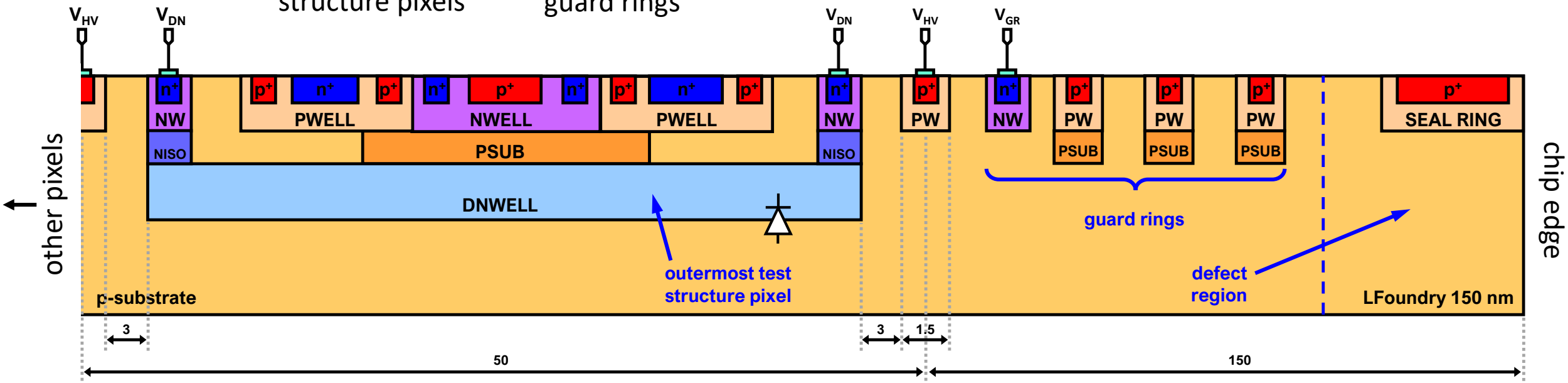
- Leakage current increases when pixel **depletion region** is near defect region
- n-type guard ring added as safeguard to “collect” leakage current
- p-type guard rings can be added to reduce ‘lateral’ **depletion**



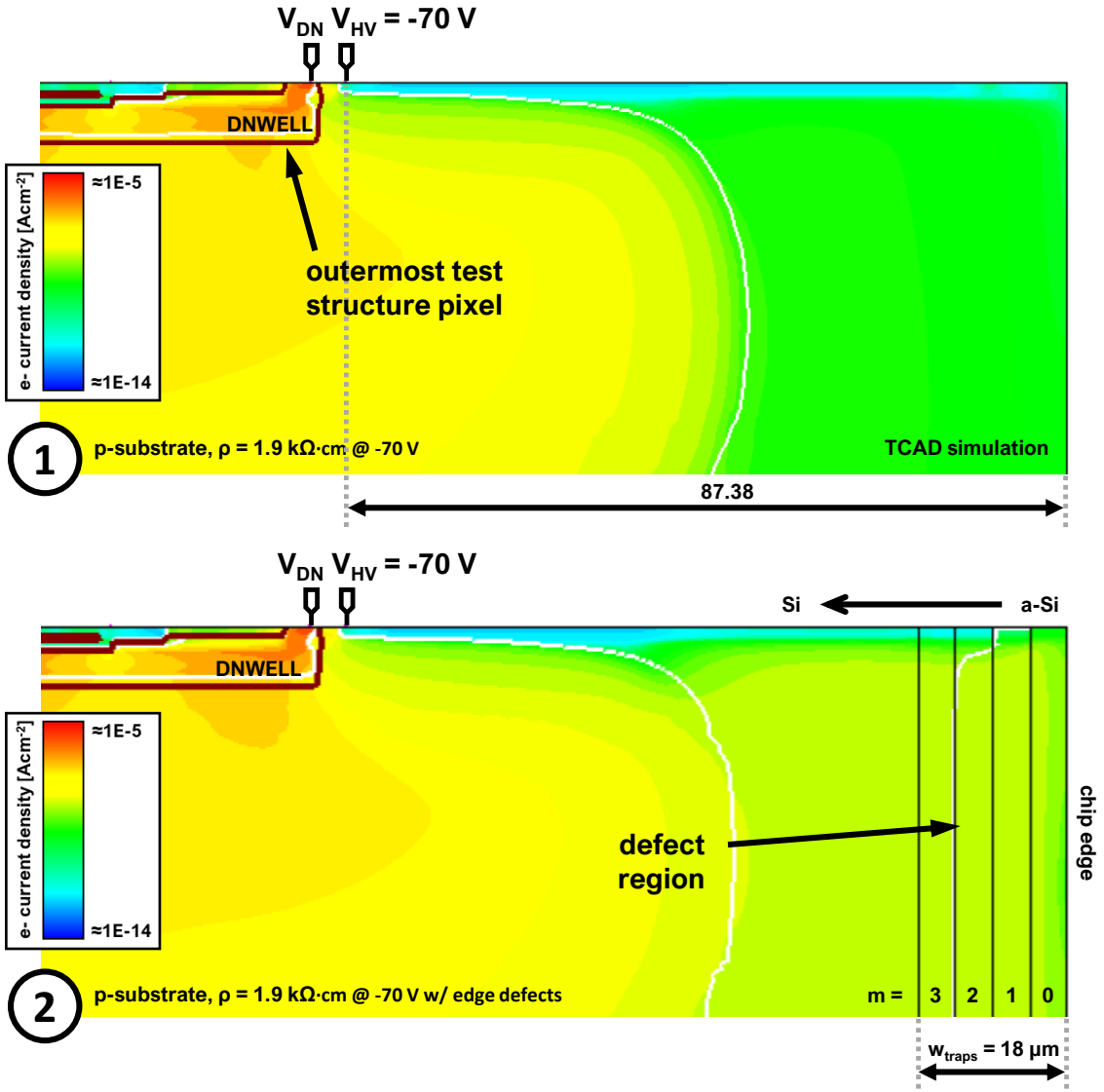
RD50-MPW2 guard rings



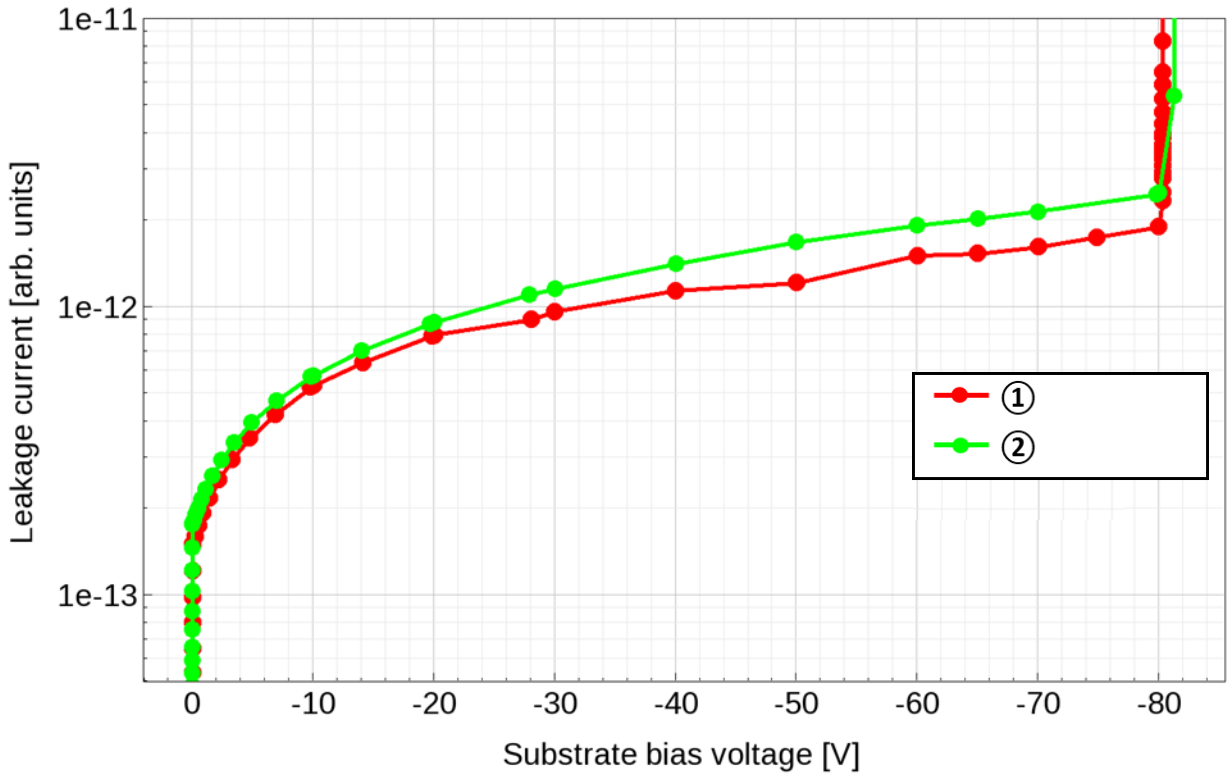
- PSUB layer can be added to further reduce lateral depletion



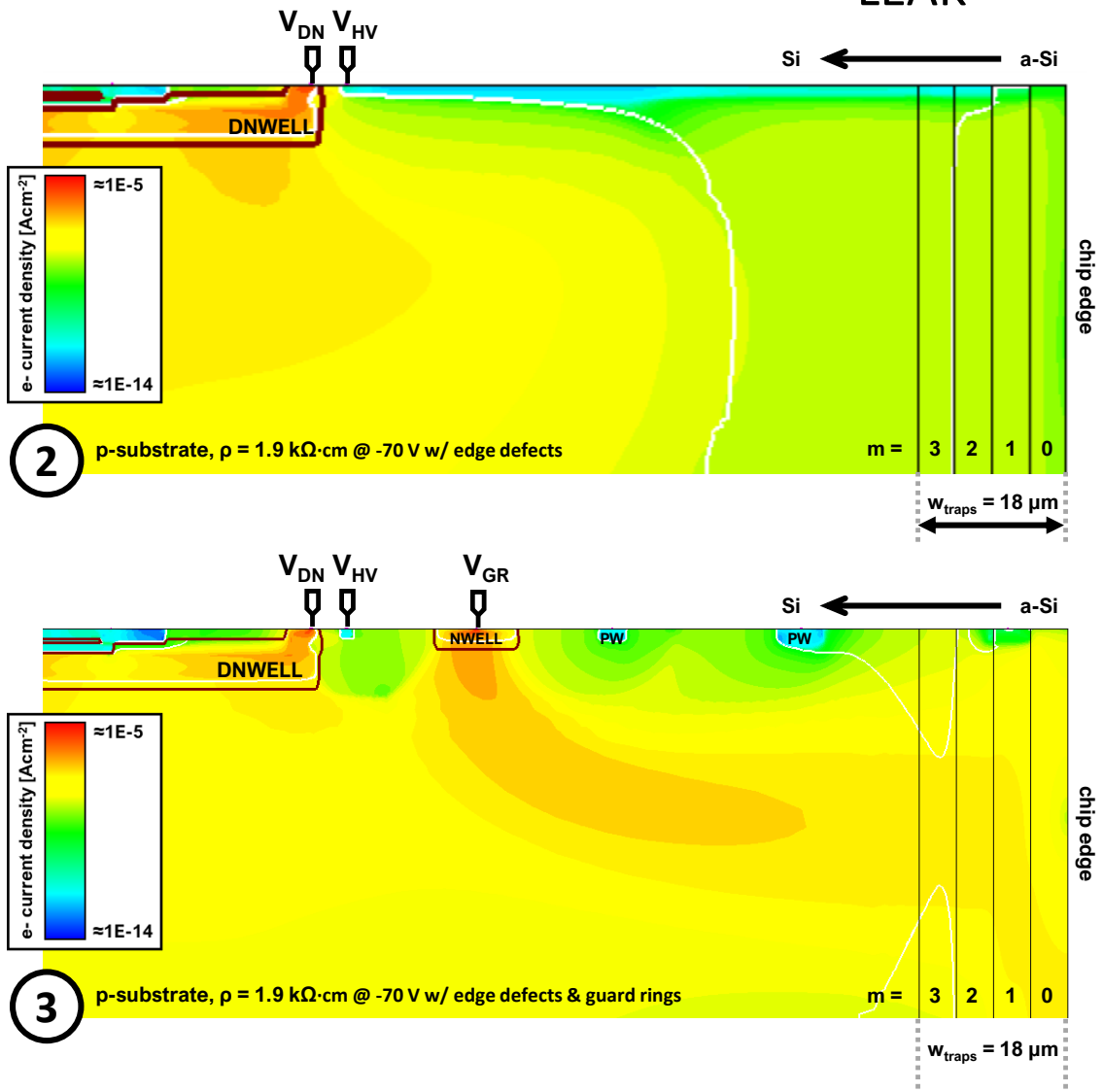
RD50-MPW1 leakage current due to edge defects



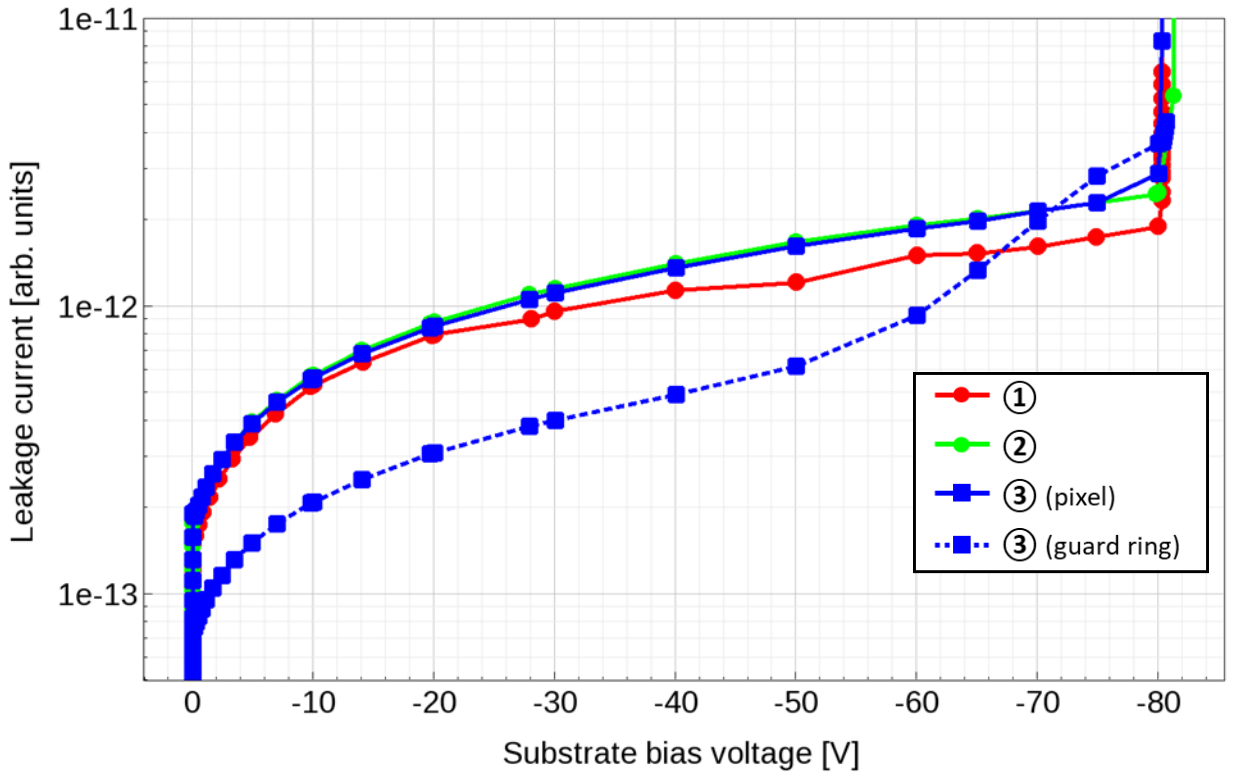
- Two simulations, with and without edge defects (Damage modelled as amorphous silicon (*Noschis et al. 2007*))
- Simulated I_{LEAK} higher when edge defects are present



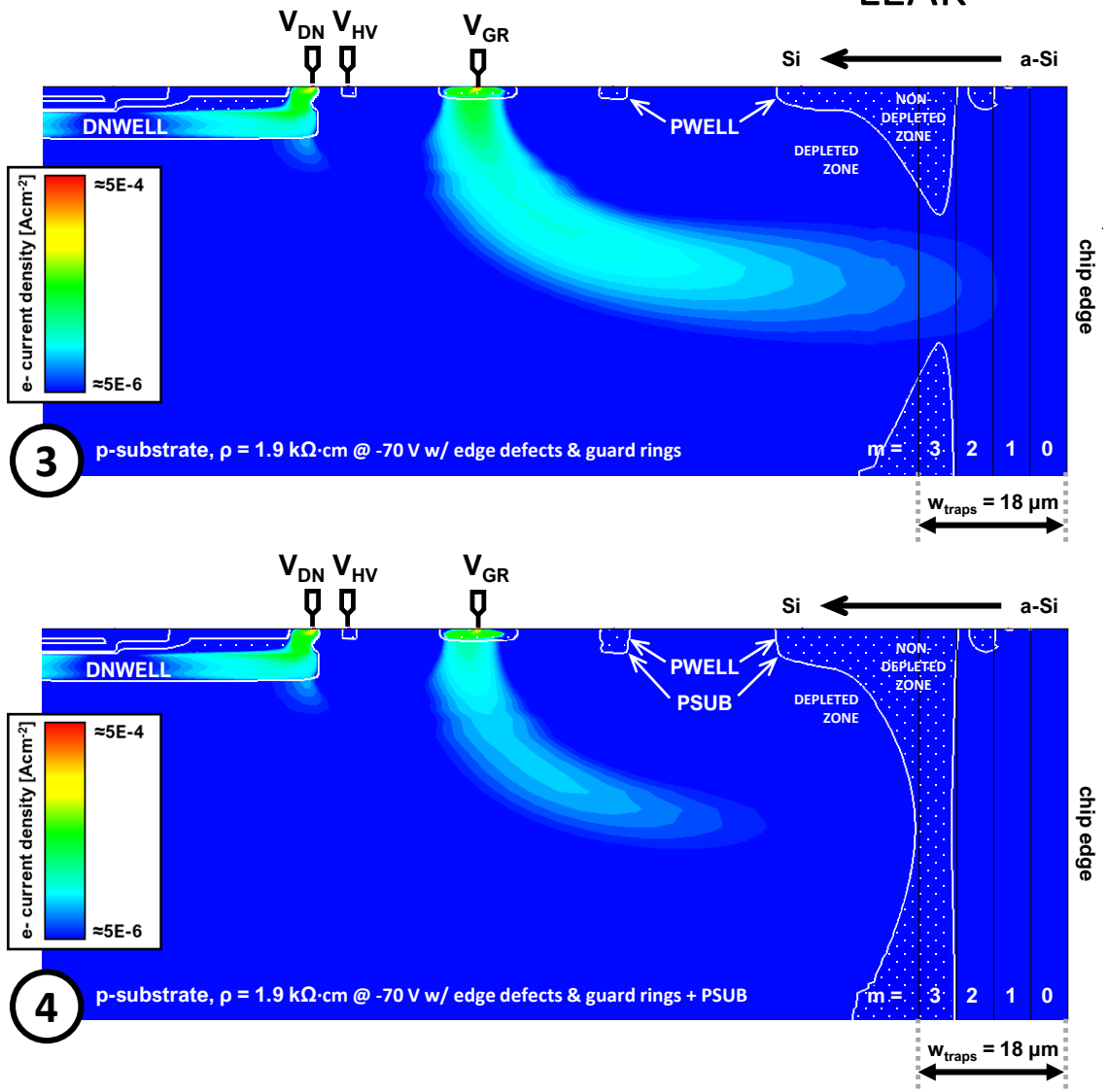
RD50-MPW2 reducing I_{LEAK} due to edge defects with guard rings



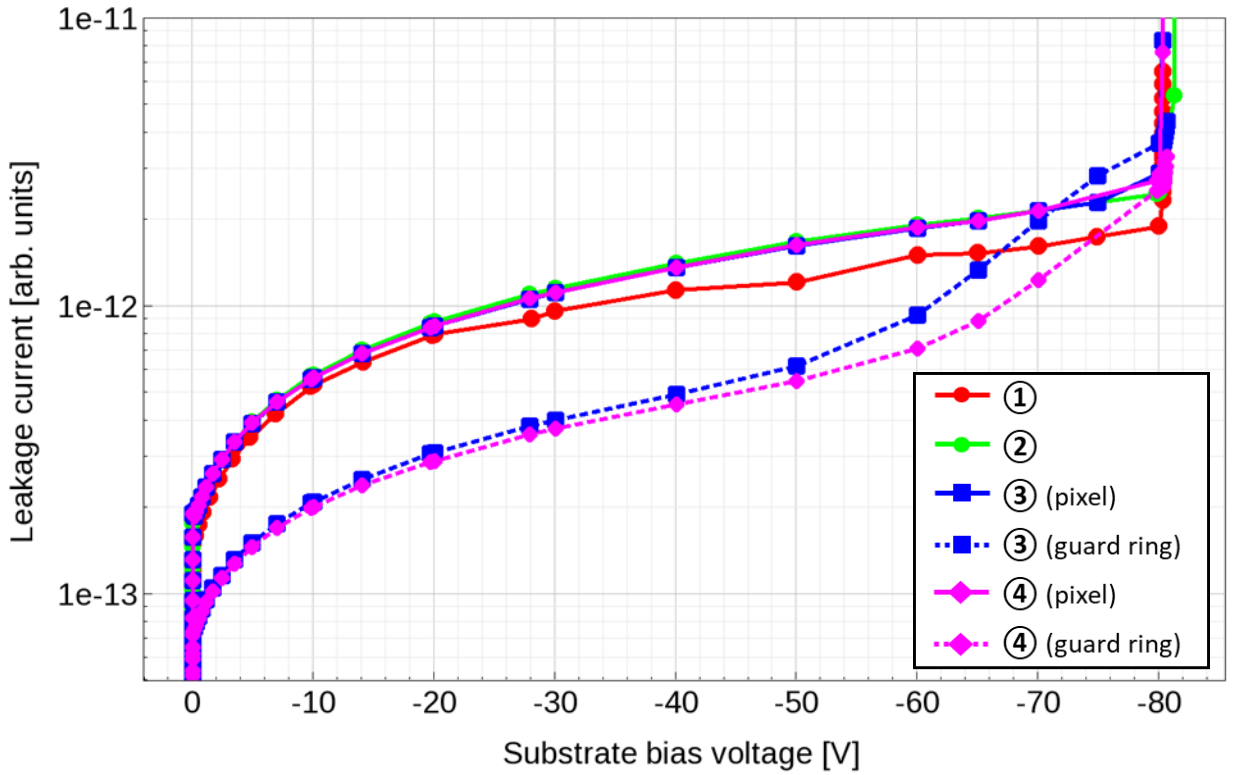
- Similar I_{LEAK} measured at both pixels
- n-type guard ring acts as another diode, increasing lateral depletion into defect region, but collects additional current



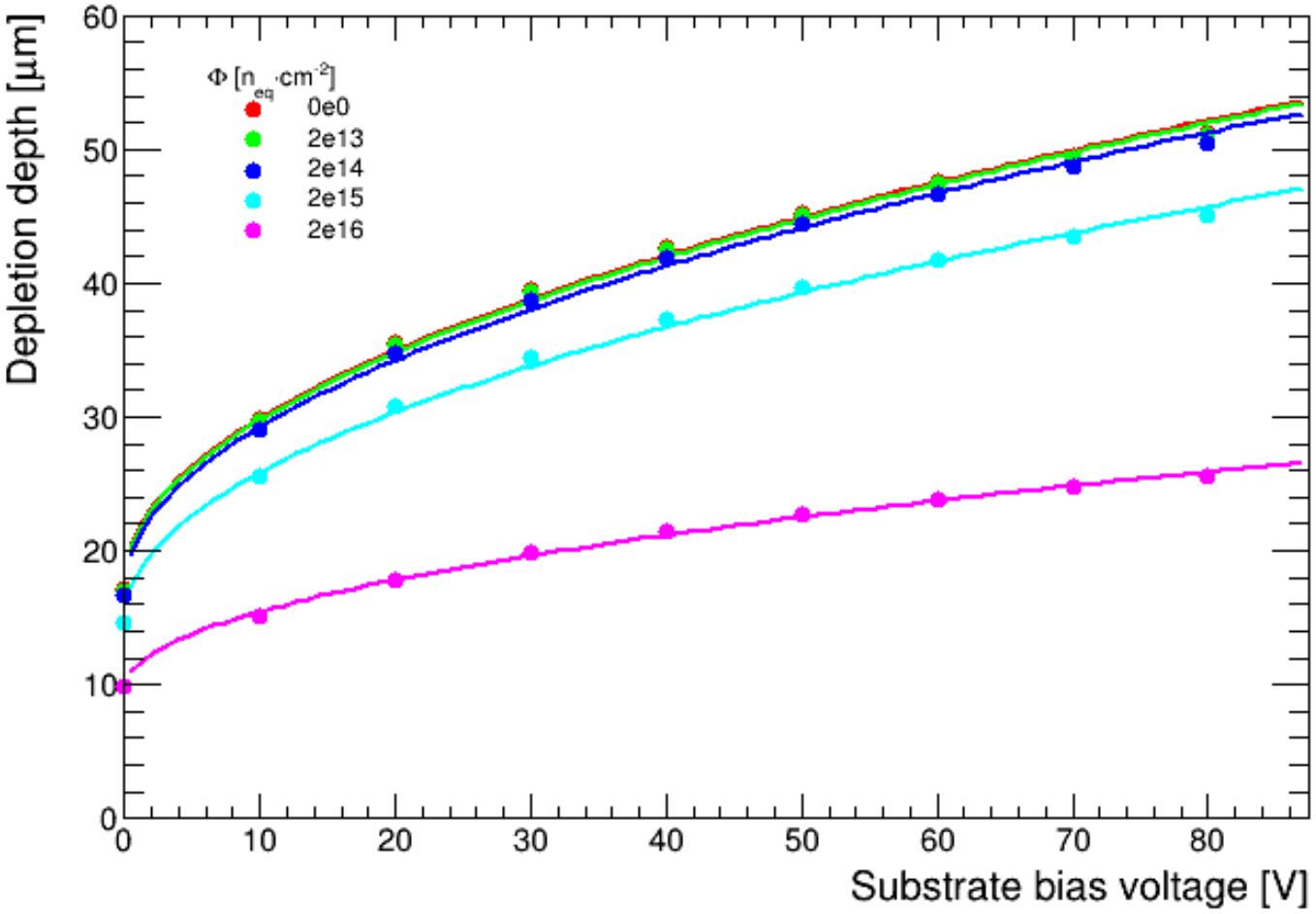
RD50-MPW2 reducing I_{LEAK} due to edge defects with guard rings



- Additional deep p-type well PSUB under guard rings reduces lateral depletion
- This reduces simulated I_{LEAK} further



RD50-MPW1 radiation damage simulation and analysis



Using **RD50-MPW1** pixel simulations:

- Simulations have been run for fluences 2E13, 2E14, and 2E15, and 2E16 [n_{eq}·cm^{-2}]
- Substrate resistivity ρ = 500 Ω·cm

Type	Energy (eV)	Trap	σ_e (cm^2)	σ_h (cm^2)	η (cm^{-1})
Acceptor	Ec-0.42	VV	$9.5*10^{-15}$	$9.5*10^{-14}$	1.613
Acceptor	Ec-0.46	VVV	$5.0*10^{-15}$	$5.0*10^{-14}$	0.9
Donor	Ec+0.36	CiOi	$3.23*10^{-13}$	$3.23*10^{-14}$	0.9

Table: (*D. Pennicard, UoGlasgow, PPT)* TCAD simulated "Modified Uni. of Perugia" model charge trapping levels defined within silicon bandgap