HV-CMOS Applications and R&D

E. Vilella, G. Casse, M. Franks, J. Gooding, J. Hammerich, S. Powell, J. Vossebeld, S. Wonsak, C. Zhang

University of Liverpool

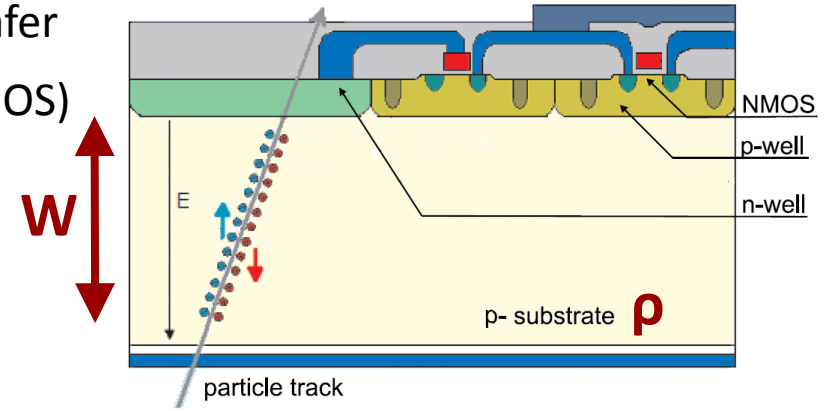
vilella@hep.ph.liv.ac.uk

Outline

- **HV-CMOS sensors**
  - Main features
- **Applications**
  - Mu3e
  - ATLAS
  - LHCb
  - pEDM
  - CERN-RD50
- **R&D**
  - Radiation tolerance
  - Leakage current
  - Pixel size
  - Response rate
- **Take-home messages**

HV-CMOS – Monolithic pixel detectors

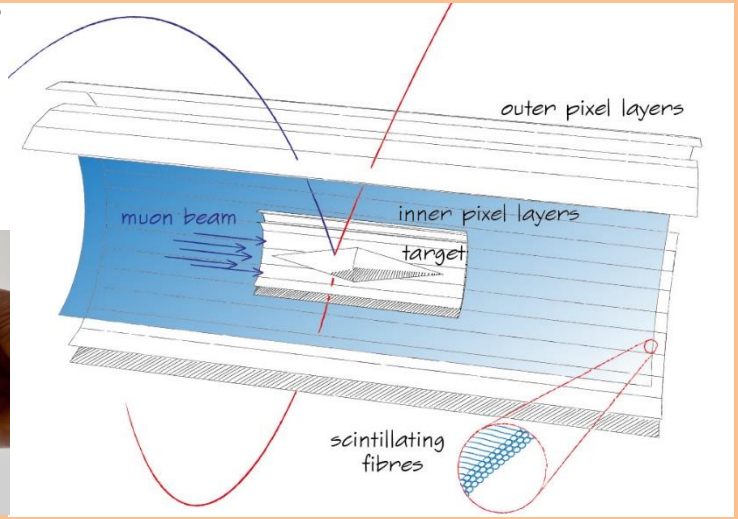
- Sensor and readout electronics on single wafer
- In conventional High Voltage-CMOS (HV-CMOS) processes
  - **No bump bonding is required**
    - Reduced material thickness (50 µm)
    - Small pixel size (50 µm x 50 µm)
    - Faster production
    - Higher yields
    - More cost effective (~£100k/m^2)
  - **Large bias voltage (V_{bias} ~100 V)**
    - Fast charge collection by drift (~200 ps charge collection and ~6 ns time resolution with time-walk correction)
    - Good radiation tolerance (~10^{15} 1 MeV n_{eq}/cm^2)
  - **High resistivity wafers (10 Ω·cm < ρ < 2-3 kΩ·cm)**
  - In-pixel amplification
  - High-volume production



➔ $W = \sqrt{\rho \cdot V_{bias}}$

Next generation of detector technology for physics experiments

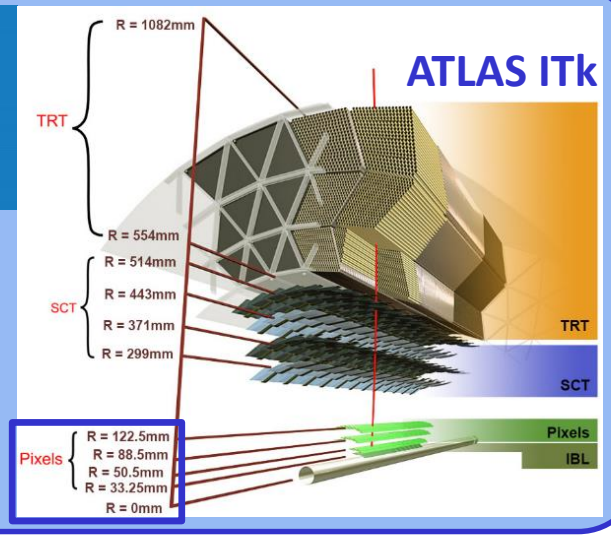
Applications



- **First HV-CMOS application in an experiment (2021+)**
- Requirements:
  - Low material
    50 µm
  - Good time resolution
    < 20 ns (for pixels)
  - Fine segmentation
    80 µm x 80 µm

ATLAS EXPERIMENT

Cancelled in 2019



LHCb

2024
2030

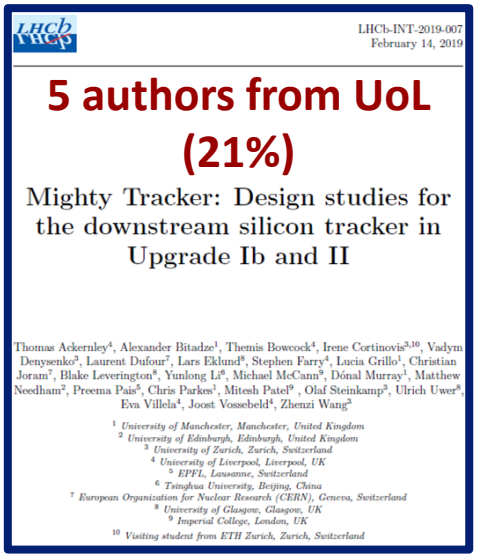
CLIC

2035+

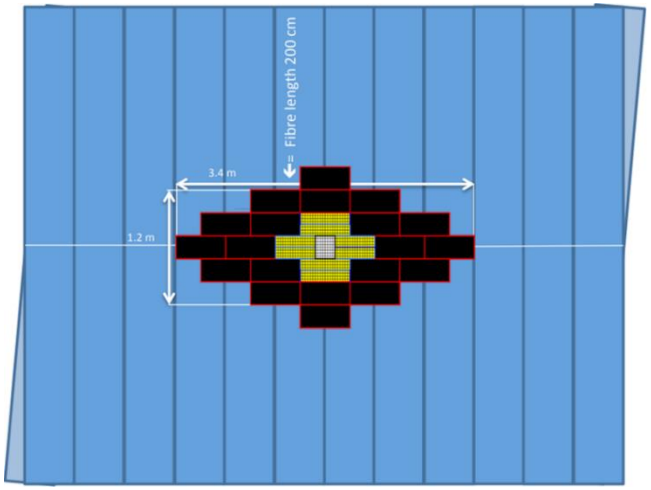
RD50

LHCb Upgrade Ib and II – Mighty Tracker

Technical note that describes initial studies for the LHCb Upgrade Ib and II



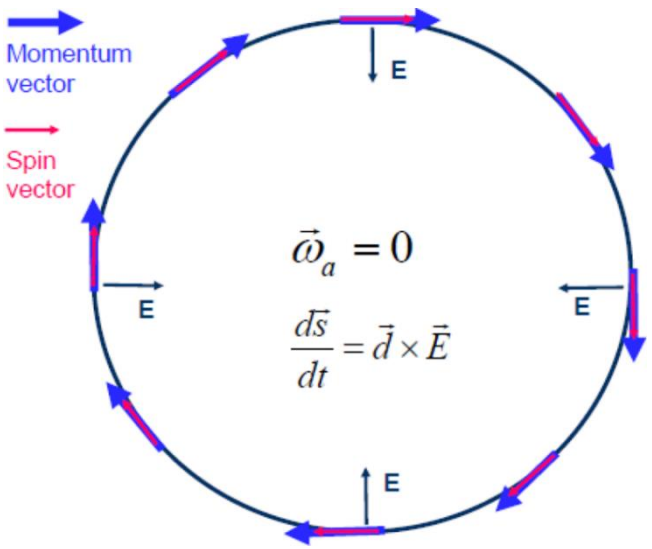
- **Downstream tracker (after the magnet)**
  - Inner tracker — Installed in LS3 (2024), Operation in Upgrade Ib
  - Middle tracker (Mighty Tracker) — Installed in LS4 (2030), Operation in Upgrade II
- **Key challenges**
  - Radiation tolerance
    - 6 x 10^{14} 1 MeV n_{eq}/cm^2 & 40 Mrad
    - Current SciFi tracker not able to cope
  - Large area
    - 3 stations with 4 layers each and 30 m^2 per layer in Upgrade I
- **HV-CMOS detectors being proposed for the Mighty Tracker**
  - Test chip in 2020 (MuPix/ATLASPix type chip)
  - With very small design effort from UoL



arXiv:1808.08865v4 [hep-ex] 2019

proton Electric Dipole Moment – pEDM

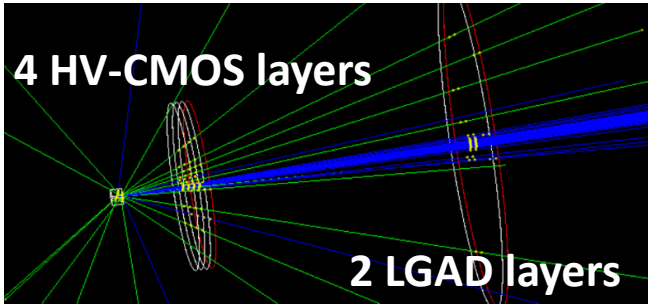
- **EDM = Distribution of + and – charge in a particle**
  - EDM ≅ 0 → Standard Model
  - EDM > 0 → New Physics
- **Proton EDM measurement**
  - Unprecedented precision of 10^{-29} e·cm
  - Experiment = Only possible using polarized protons at the so-called *magic* momentum of 0.7 GeV/c in an all electric storage-ring
  - Detector = Polarimeter measures particle rate as a function of the angle with the beam



Y. Semertzidis, 2016

- **Current detector technology = LYSO crystals**
  - Poor detection efficiency (70%)
  - Poor radiation tolerance
  - Very expensive
- **New detector technology = Time-of-Flight based**
  - Combination of **HV-CMOS sensors (spatial resolution)** with fast **LGADs (time resolution)**
  - > 90% detection efficiency (simulated)

Geant4 simulation



J. Gooding, 2019

Take-home message #1

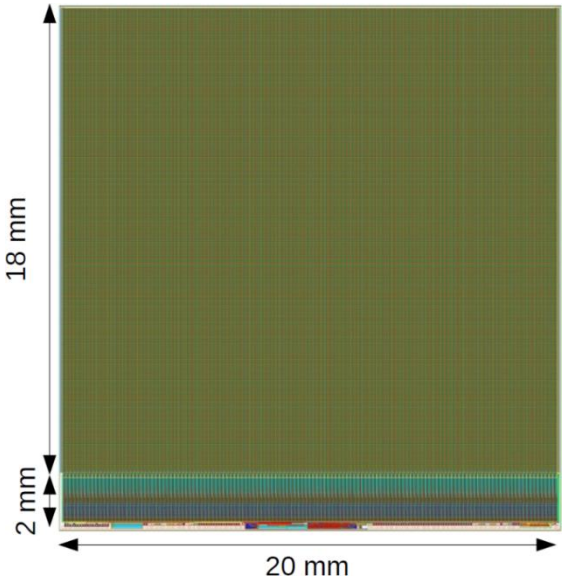
The depleted CMOS project for the ATLAS ITk Upgrade was cancelled in 2019, but this is not a problem for us as our funding is for doing generic R&D.

Take-home message #2

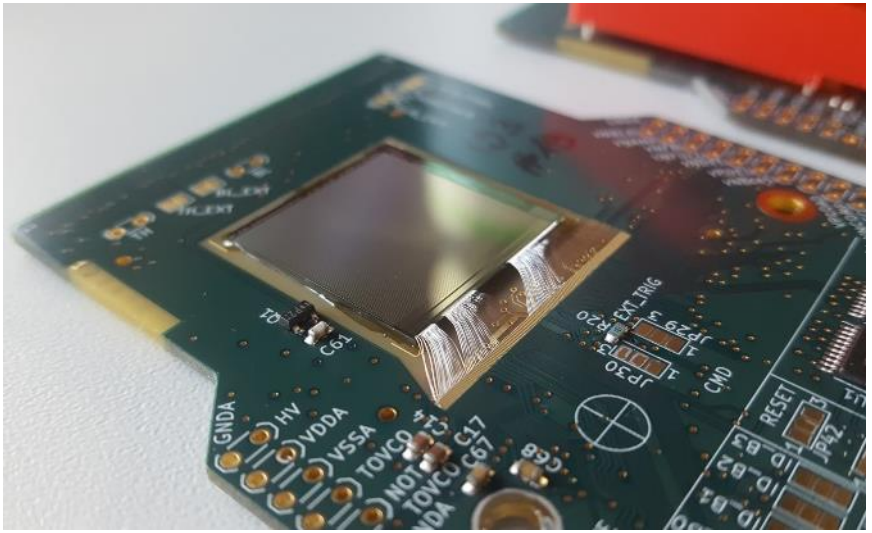
The interest in HV-CMOS detectors by planned and possible future experiments in physics is continuously growing.

We are part of the proposers for several of these experiments.

HV-CMOS – First full reticle detectors



R. Schimassek, 2019



J. Hammerich, 2019

ATLASPix3 – Some chip details

- Matrix with 132 columns x 372 rows
- 150 µm x 50 µm pixel size
- Trigger latency ≤ 25 µs
- Radiation hard design
- Serial powering (only one power supply needed)
- Data interface is very similar to ATLAS RD53 readout chip
- Power consumption is ~200 mW/cm^2 (with 25 ns time resolution)
- Very initial measured results available (fabricated in 2019)

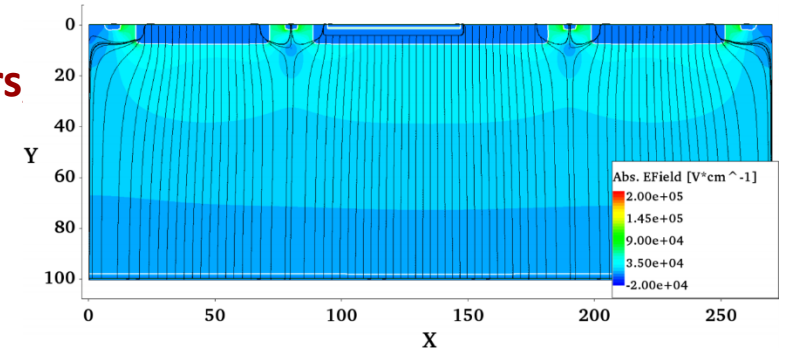
ATLASPix3 is the first full reticle pixel detector (2 cm x 2 cm) compatible with ATLAS ITk L4 requirements

Take-home message #3

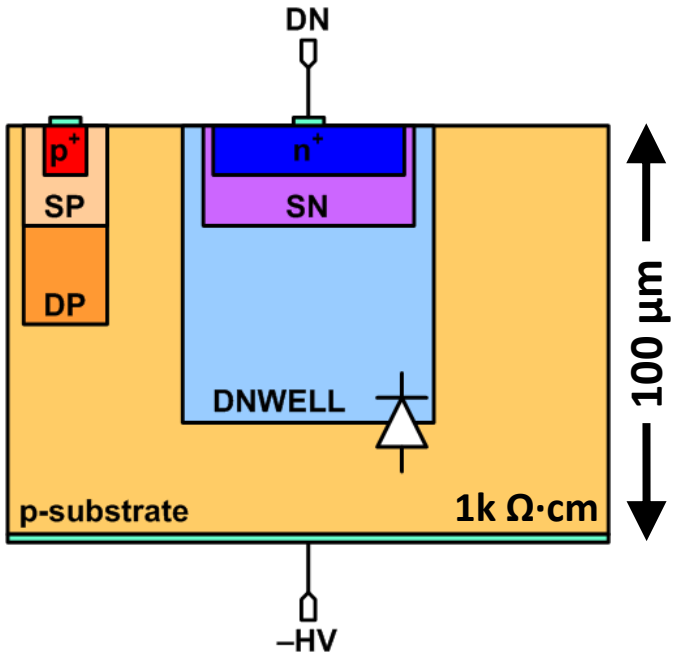
HV-CMOS sensors are making their way to final prototypes before entering production.

Radiation tolerance

- From TCAD simulations, we know
  - **Thin and high resistivity HV-CMOS sensors with backside biasing behave better**
    - Stronger electric field lines
    - Shorter charge collection times
    - Better radiation tolerance
- CMOS foundries tend to fabricate thick chips in low resistivity wafers, with topside biasing
- **We have done post-processing of some of our HV-CMOS prototypes in a 1 kΩ·cm bulk**
  - Thinned to 100 um
  - Added backside contacts for applying large bias voltages from the back
- **Performance evaluation of HV-CMOS sensors**
  - Before/after irradiation with **n-fluences ≤ 2 x 10^{16} 1 MeV n_{eq}/cm^2**
  - Test #1 → e-Transient Current Technique
  - Test #2 → Charge Collection Efficiency

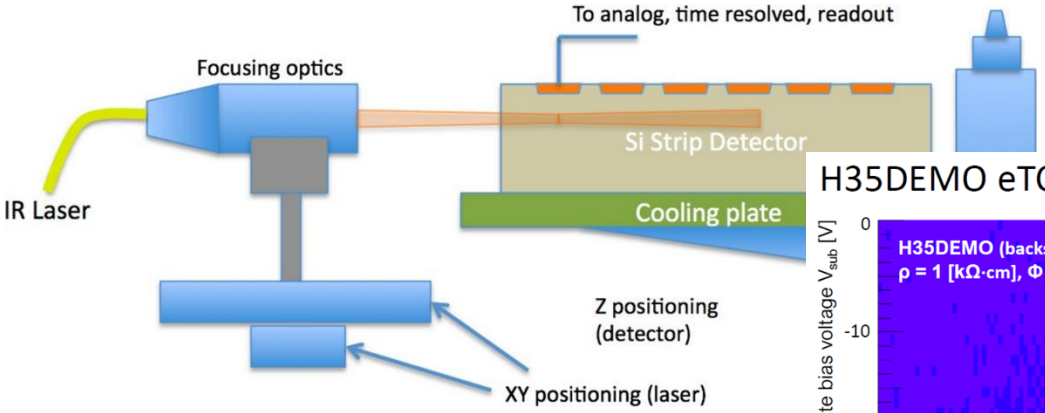


L. Meng, PhD thesis, 2018



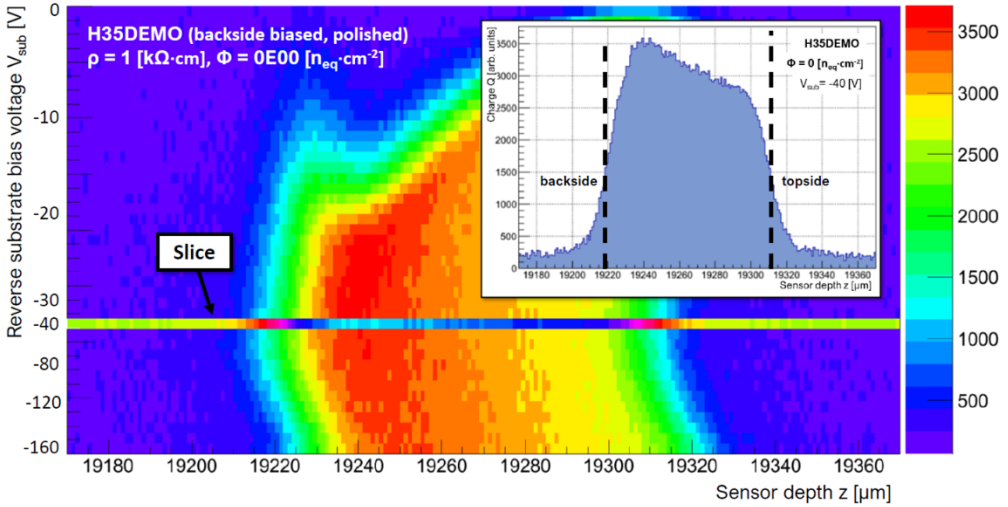
Radiation tolerance – eTCT

- **Test #1 → e-Transient Current Technique (eTCT)**
  - Measure the width of the depletion region
  - 3 x 3 matrix of passive pixels (H35DEMO)
  - Before irradiation → Sensor fully depleted at approx. 20 V of bias voltage
  - After irradiation → Sensor *alive* at 2 x 10^{16} 1 MeV n_{eq}/cm^2 n-fluences
- Publication in preparation



G. Kramberger, IEEE Trans. Nucl. Sci., 2010

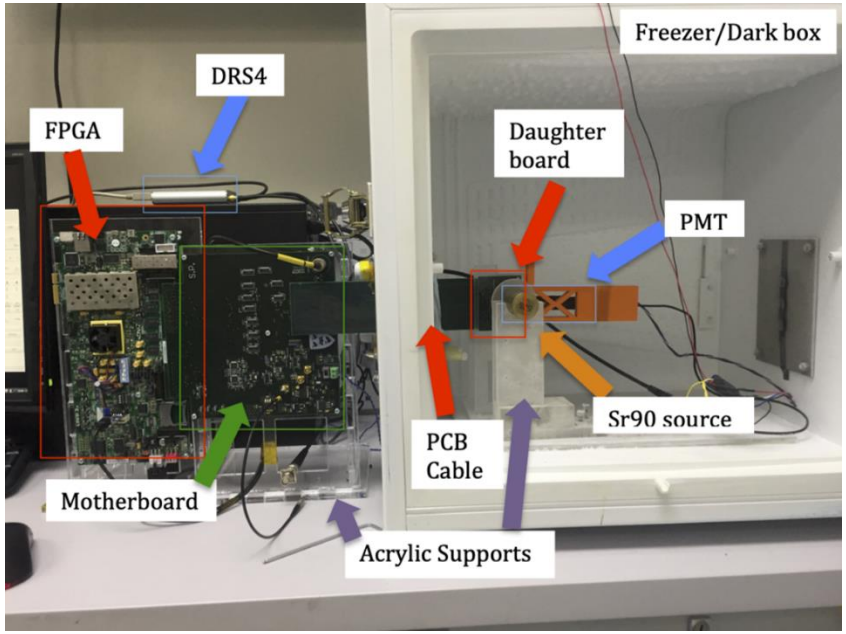
H35DEMO eTCT measurements – "z-voltage scan"



M. Franks, 2019

Radiation tolerance – CCE

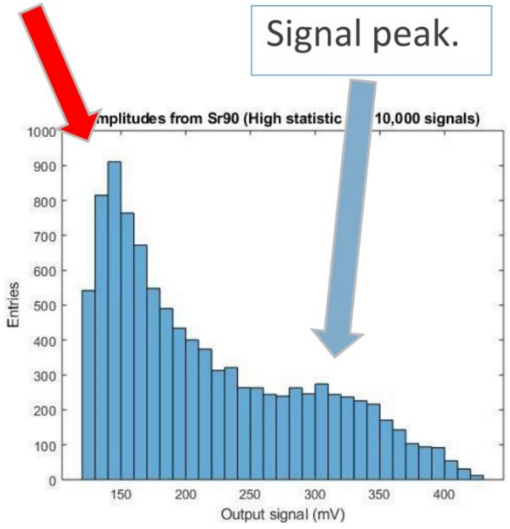
- **Test #2 → Charge Collection Efficiency (CCE)**
  - 16 x 1 active pixels (H35DEMO)
  - Radioactive source
  - We have encountered some difficulties
    - Charge sharing
    - No conclusive results so far
  - We will repeat the measurements using another matrix of the same chip
    - Different features → less charge sharing



J. Gooding, 2019

Charge sharing / noise peak.

Signal peak.



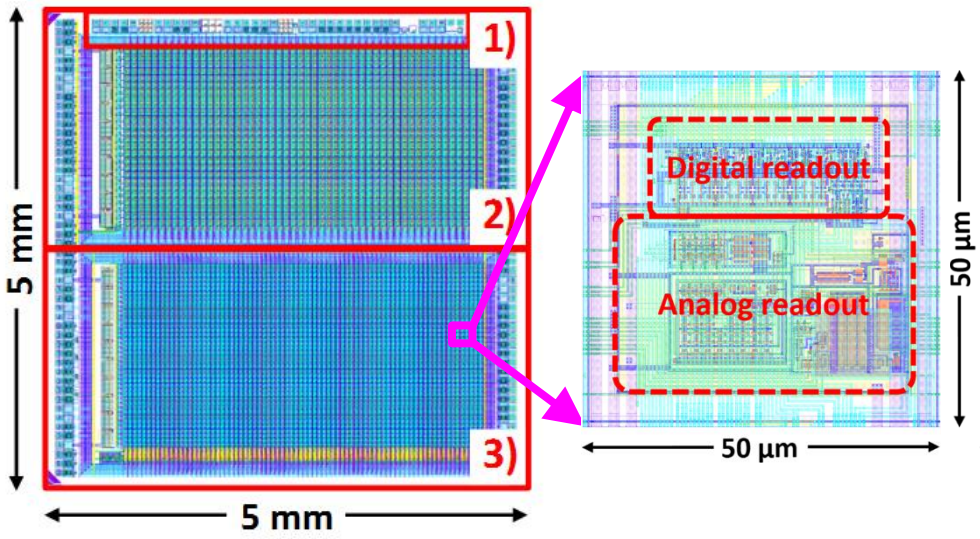
CERN-RD50 – Chip design

RD50-MPW1 (fab-out April 2018)

- 150 nm HV-CMOS LFoundry
- 600 and 1.1k Ω·cm wafers

3) Matrix of HV-CMOS pixels with

- 50 µm x 50 µm pixel size
- Analog + digital readout in sensing area of the pixel
- Continuous readout (FE-I3)
- 40 rows x 78 columns

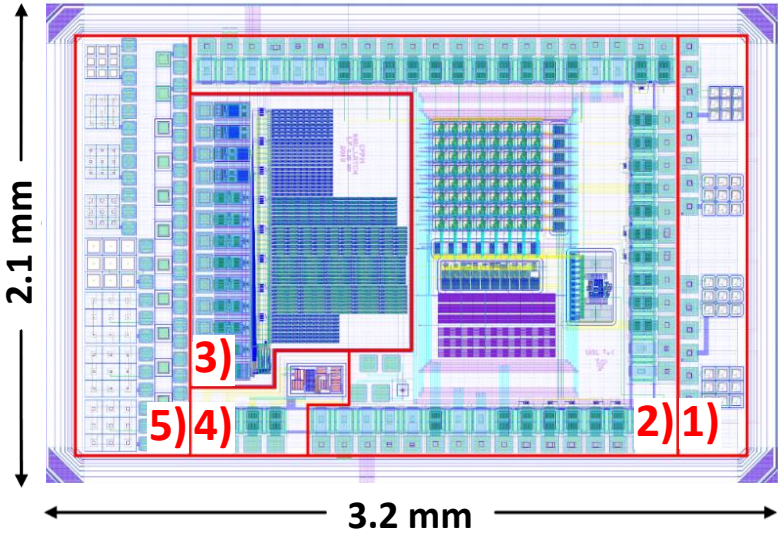


RD50-MPW2 (fab-out January 2020)

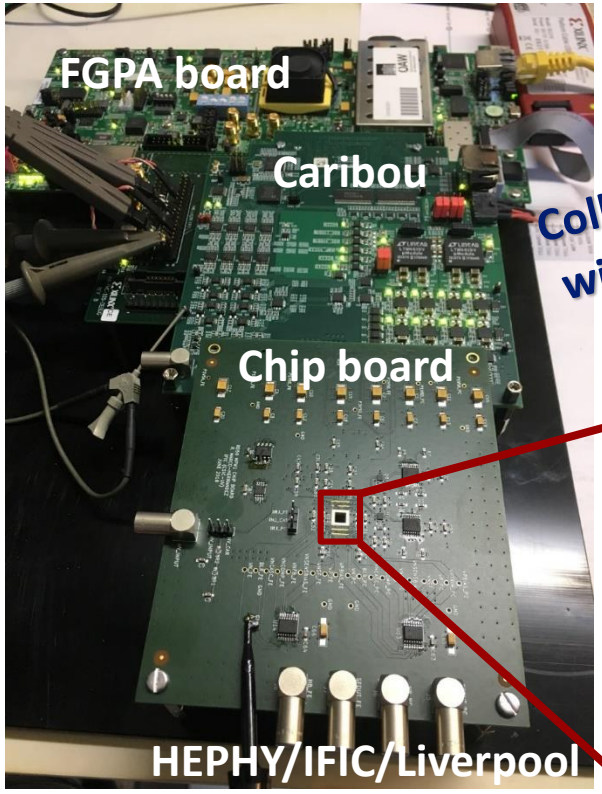
- 150 nm HV-CMOS LFoundry
- 10, 100, 1.9k and 3k Ω·cm wafers
- **Techniques to improve ILEAK and VBD**

2) Matrix of HV-CMOS pixels with

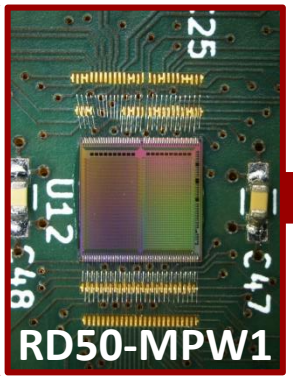
- 60 µm x 60 µm pixel size
- Analog readout in sensing area of the pixel
- Fast response rate
- 8 rows x 8 columns



RD50–MPW1 – DAQ and measurements

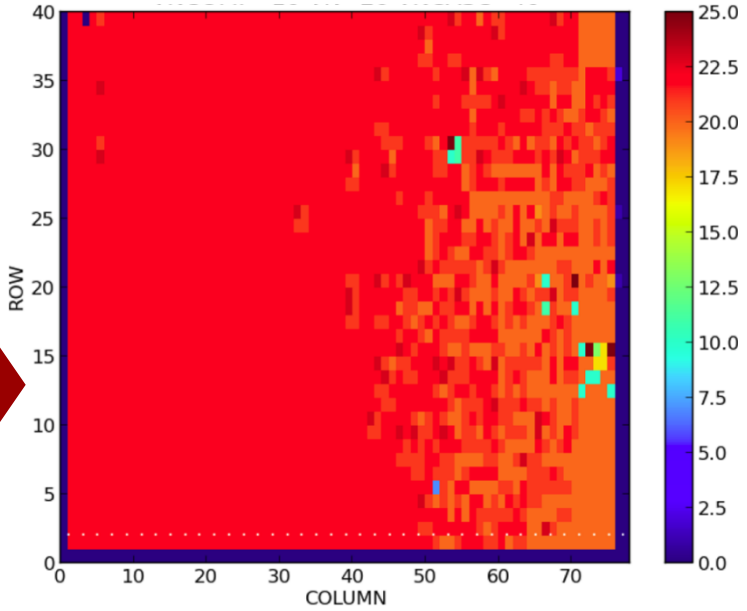


Collaborative effort within CERN-RD50



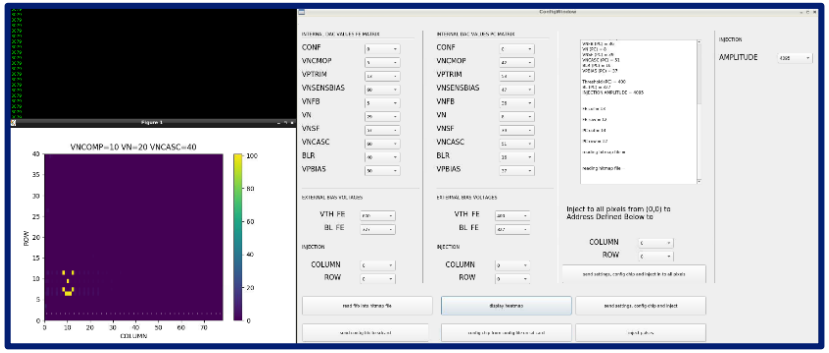
Hit map

- N-test pulses sent to each pixel
- Measure how many hits per pixel



S. Powell, 2019

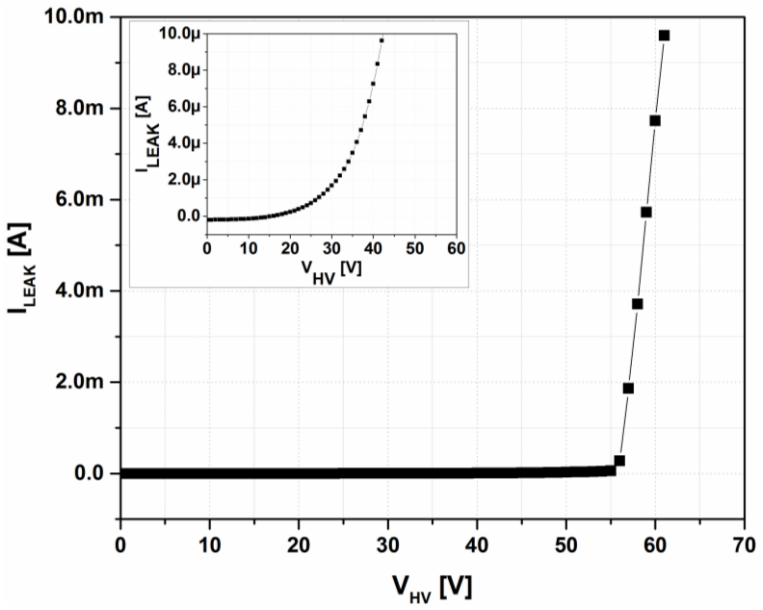
- The chip essentially works, but it has some issues



RD50-MPW1 – Measurements and TCAD

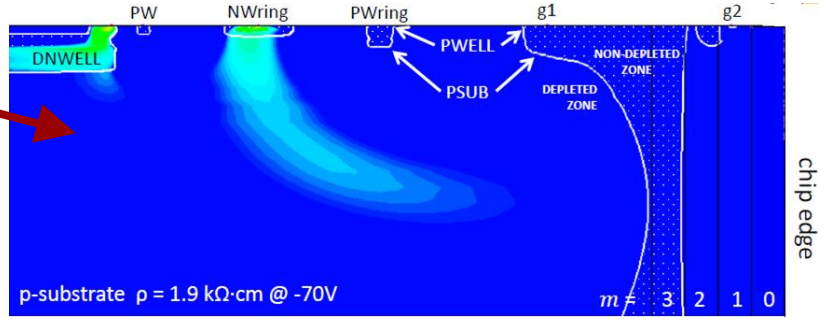
I-V of test pixel

- Probe station with 50 µm x 50 µm sensor
- **VBD ~55-60 V as expected from the design**
- **ILEAK ~µA order well before VBD (too high)**



TCAD simulations

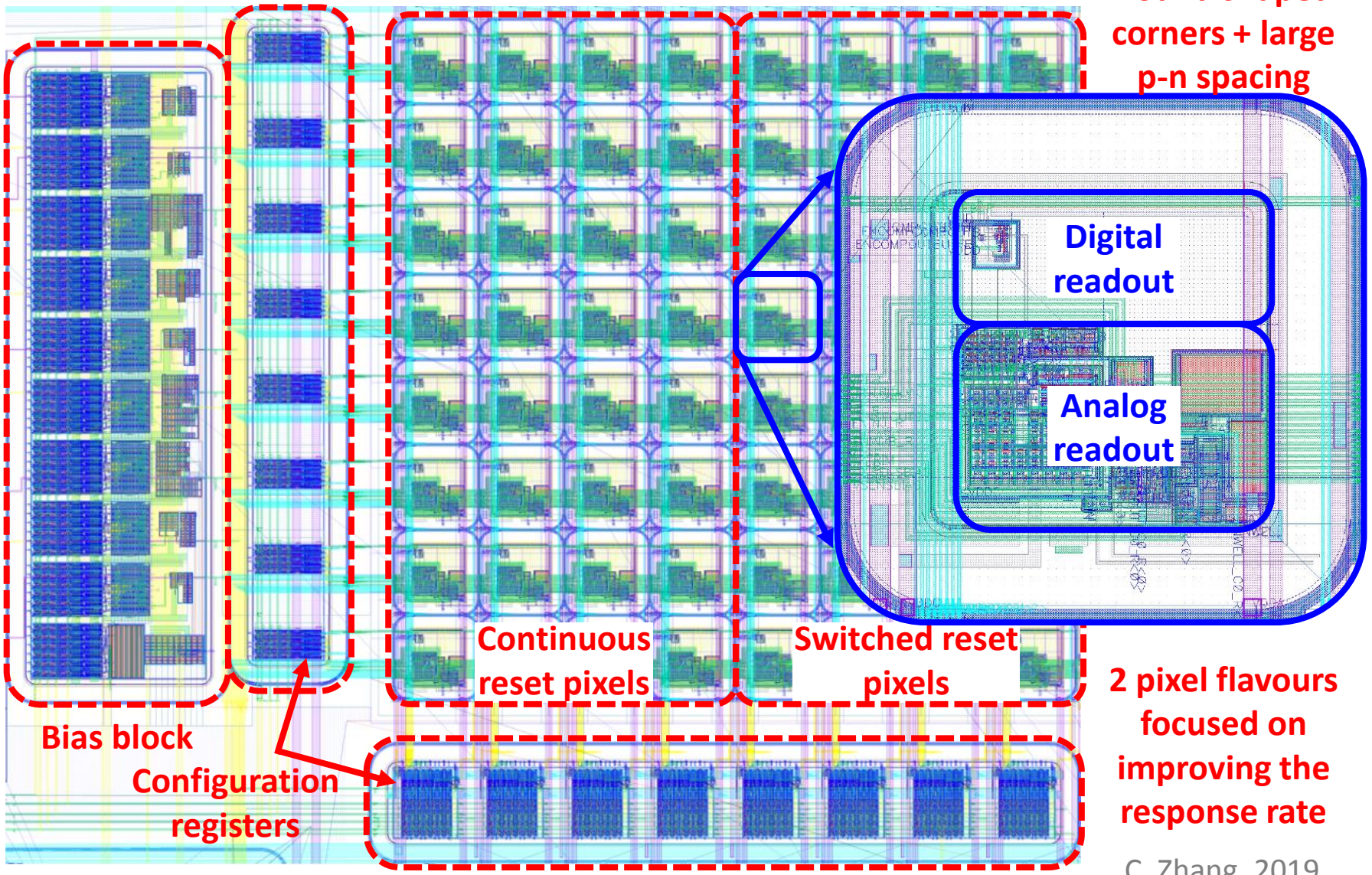
- **Pixel geometry**
  - P-n spacing → increase
  - Corners → round shaped
- **Edge of the chip**
  - Requires guard rings
- **Structures added by the foundry** to prepare the design files for fabrication
  - Prevent or minimize their presence



M. Franks, 2019

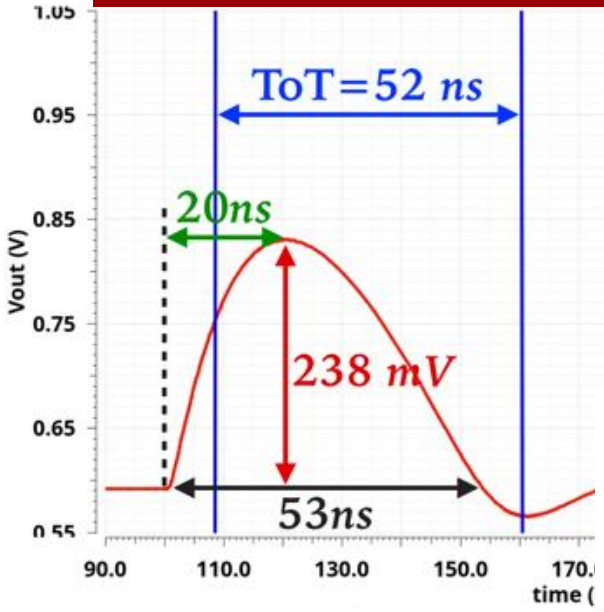
New techniques developed and implemented in RD50-MPW2

RD50-MPW2 – Pixel matrix



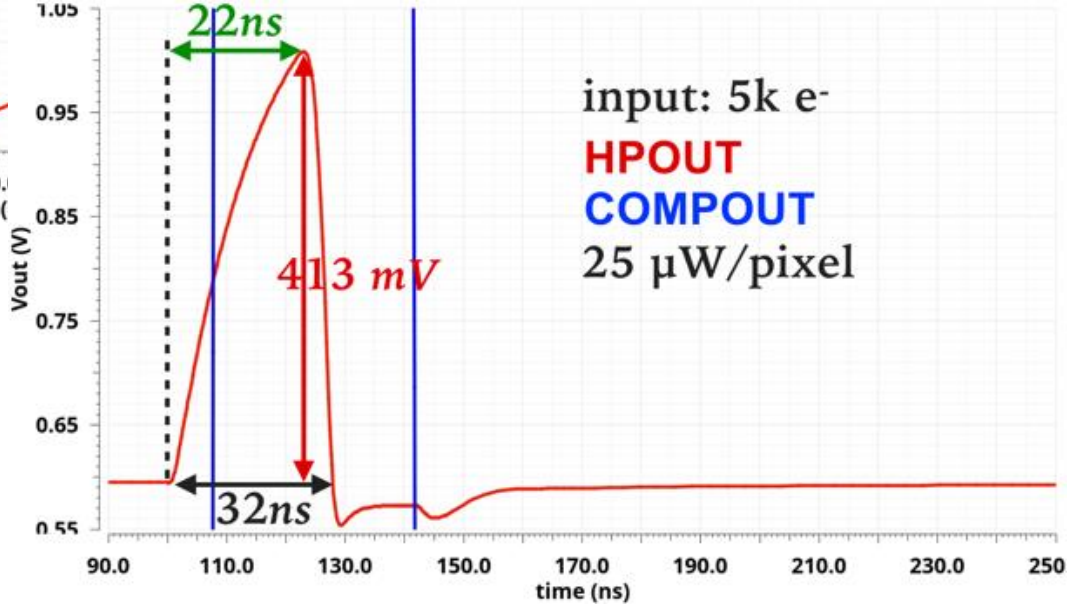
RD50-MPW2 – Fast response rate

Continuous reset pixel



input: 5k e-
HPOUT
COMPOUT
24 µW/pixel

Switched reset pixel



input: 5k e-
HPOUT
COMPOUT
25 µW/pixel

C. Zhang, 2019

Take-home message #4

We are doing R&D of HV-CMOS sensors to achieve better radiation tolerance, smaller pixel sizes and improved time resolution.

Take-home message #5

We are very active in RD50.

We lead the CMOS WP.

Thanks for listening.

Happy to answer your questions.

Back up slides

Commercial vendors (I)

GLOBALFOUNDRIES

TSI SEMICONDUCTORS

Commercial vendors (II)

Foundry → / Parameter ↓	LFOUNDRY A SMIC COMPANY	TOWERJAZZ The Global Specialty Foundry Leader	TSI SEMICONDUCTORS
Feature node	150 nm	180 nm	180 nm
HV	Yes	No	Yes
HR	Yes	Yes	Yes
Quadruple well	Yes	Yes	No (triple)
Metal layers	6	6	6
Backside processing	Yes	Yes	No
Stitching	Yes	Yes	Yes
TSV	No	No	–

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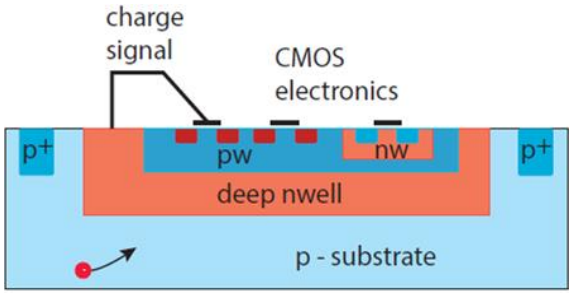
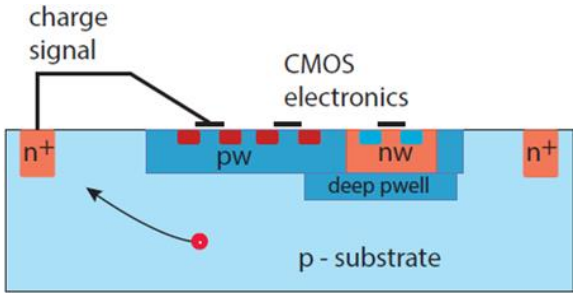
Large vs small fill-factor

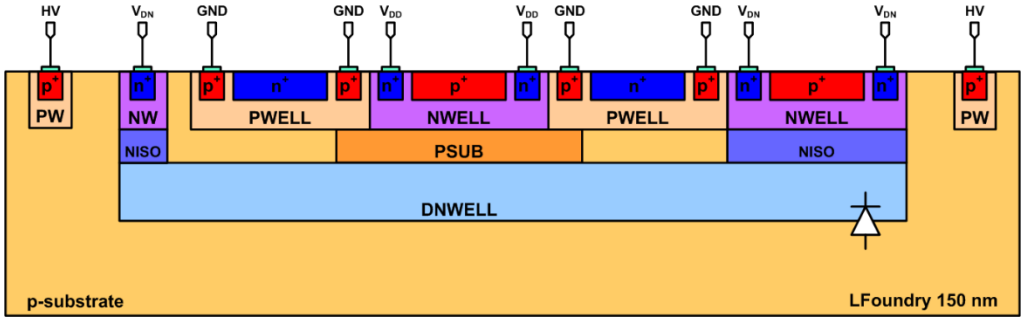
Sensor cross-section → Parameter ↓		
Name	Large fill-factor (HV/HR-CMOS)	Small fill-factor (HR-CMOS)
1) p/n junction	p-substrate/large deep n-well	p-substrate/small shallow n-well
2) Substrate biasing	High voltage	Low voltage
3) Substrate resistivity	< 2-3 kΩ·cm	< 8 kΩ·cm
1) + 2) + 3)	▪ No (little) low-field regions ▪ Shorter drift distances ▪ Higher radiation tolerance ▪ Larger sensor capacitance ▪ Larger noise & speed/power penalties ▪ RO in charge collection well	▪ Low-field regions ▪ Longer drift distances ▪ Lower radiation tolerance ▪ Very small sensor capacitance ▪ Reduced noise & power ▪ RO outside charge collection well
Process	AMS/TSI and LFoundry	TowerJazz

ATLAS – Depleted CMOS pixel review

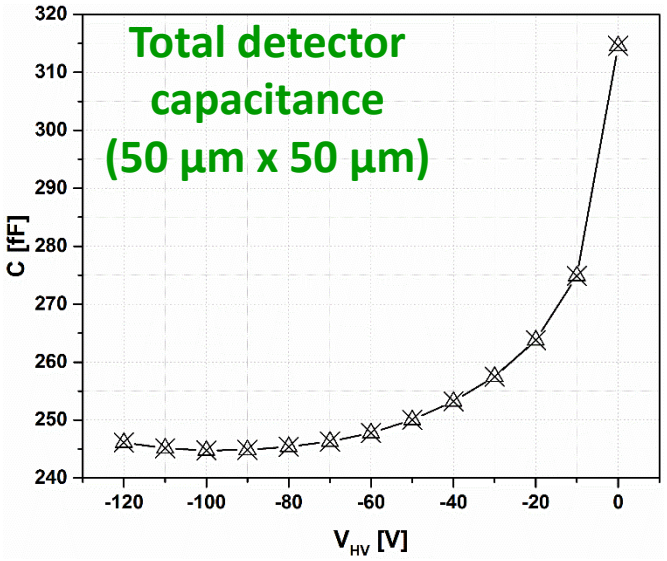
- **What for?**
  - To evaluate the costs/risks/benefits of using depleted monolithic CMOS detectors as a replacement of the baseline choice of hybrid pixel detectors in L4 of the ITk pixel barrel
  - Replacement = CMOS modules to be "plug-compatible" with hybrid modules
- **Who?** → Several ATLAS Upgrade coordinators and leaders
- **When?** → Several meetings in 2018-19 (final decision announced March 2019)
- **Observations**
  - Excellent R&D being done in CMOS land
  - Eliminates hybridization and can reduce production time of modules
  - Very tight time constraints
    - "Plug-compatible" module of CMOS detectors available and tested only in 2021 (too risky, no time for plan B if CMOS doesn't work well enough)
  - Not massive cost savings (with 70% yield, 6.5% savings relative to cost in TDR)
  - Hybrid pixel detectors making significant progress
- **Recommendation**
  - Advantages are too modest to justify potentially impacting the Pixel Upgrade
  - Use hybrid modules in L4, as planned in the baseline

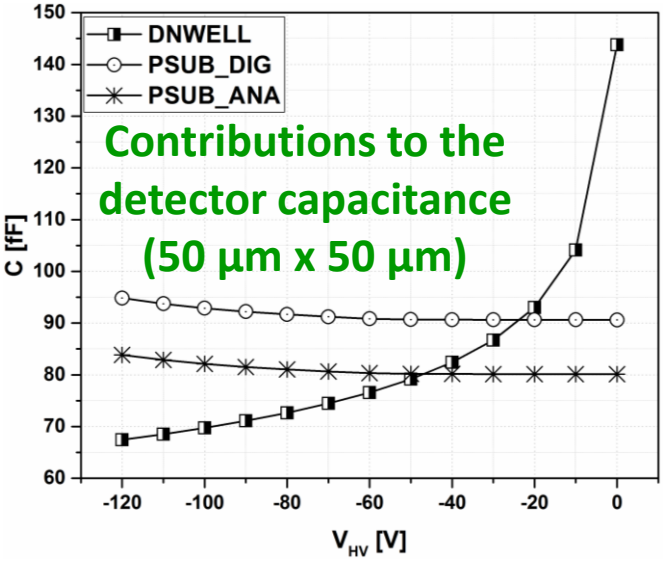
RD50-MPW1 – Sensor

Sensor cross-section

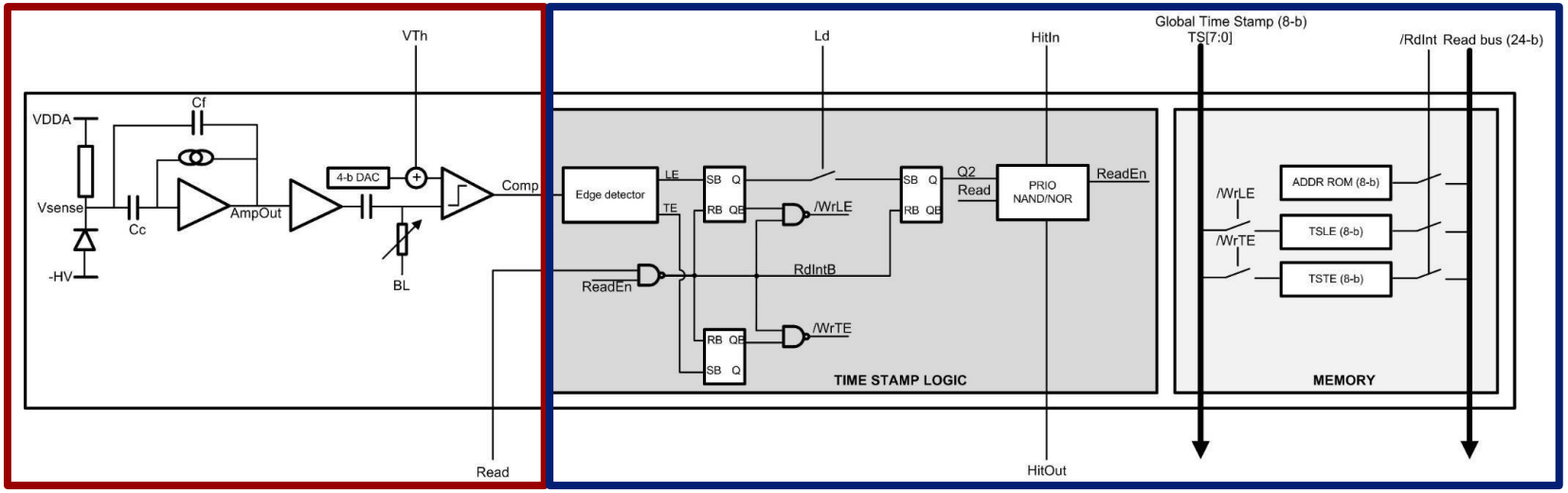


- Large fill-factor pixel
- PSUB layer isolates NWELL from DNWELL
  - CMOS electronics in pixel area are possible
- Detector capacitance has 2 contributions
  - P-substrate/DNWELL
  - PSUB/DNWELL
- Total pixel capacitance (50 µm x 50 µm) ~250 fF
- Equivalent Noise Charge (ENC) ~100 – 120 e^-





RD50-MPW1 – Readout electronics



Analog readout

- Sensor biasing circuit, CSA, RC-CR filters and CMOS comparator
- CSA with programmable discharging current
- CMOS comparator with global VTH and local 4-bit DAC for fine tuning

Digital readout

- Continuous readout (synchronous, triggerless, hit flag + priority encoding)
- Global 8-bit Gray encoded time-stamp (40 MHz)
- For each hit
  - ➔ Leading edge (LE): 8-bit DRAM memory
  - ➔ Trailing edge (TE): 8-bit DRAM memory
  - ➔ Address (ADDR): 6-bit ROM memory

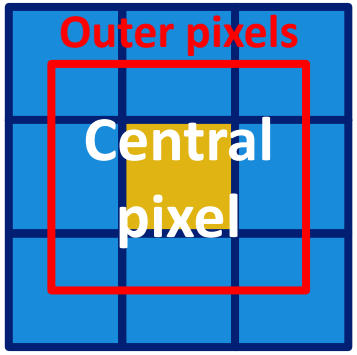
  } ➔ TOT = LE – TE (off-chip)

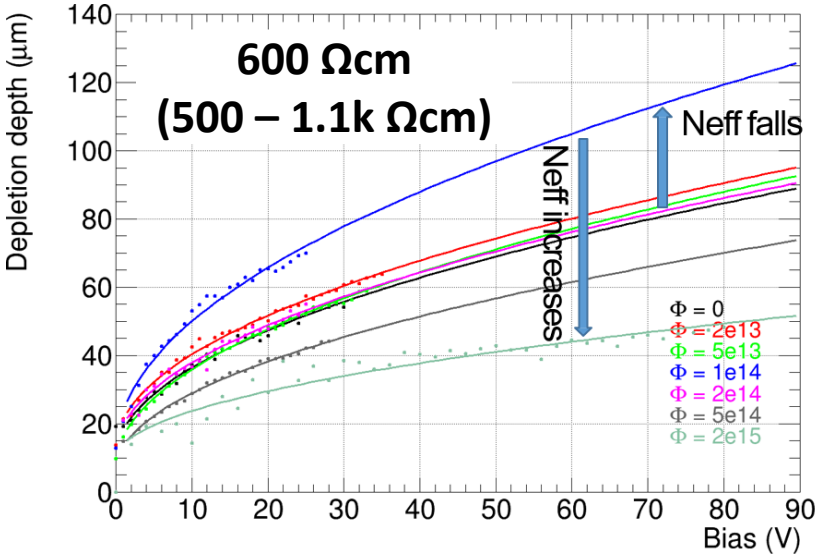
RD50-MPW1 – Measured results

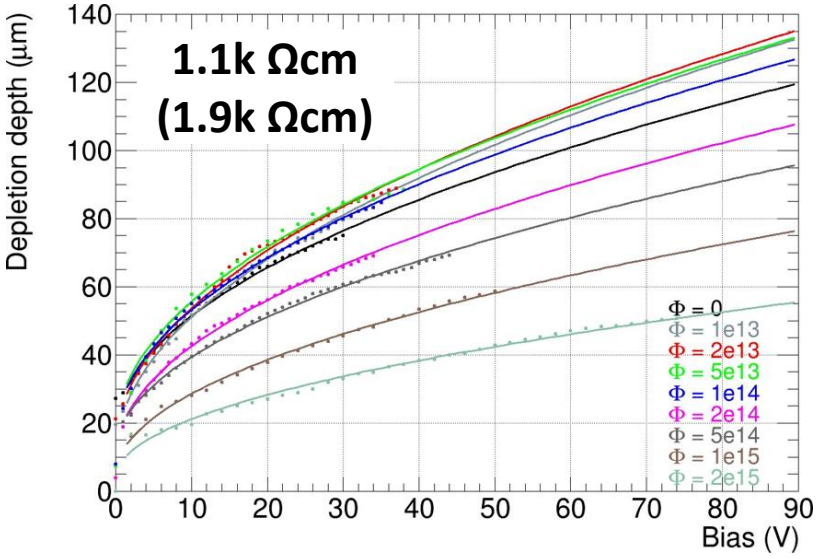
eTCT measurements to study sensor depletion region

I. Mandic, TREDI 2019

- Samples irradiated at TRIGA reactor in Ljubljana to several different n-fluences ranging from 1E13 to 2E15 n_{eq}/cm^2
- **Test structure**
  - ➔ 3 x 3 pixels matrix without readout electronics
  - ➔ Central pixel to read out
  - ➔ Outer pixels connected together
  - ➔ Pixel size is 50 µm x 50 µm







- Depletion depth changes with irradiation + acceptor removal effects seen