Design, Simulation, and Characterisation of Fast Timing Silicon Sensors for HEP applications

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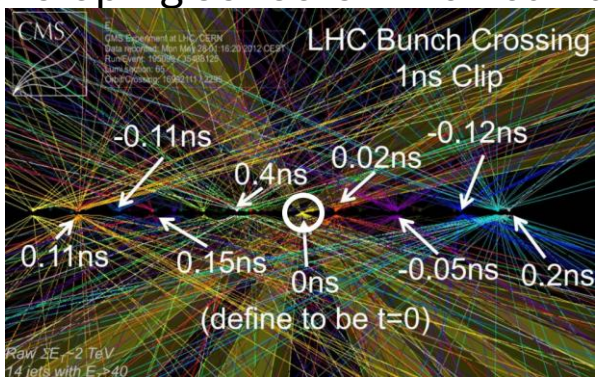
Requirements of Fast Timing

Anticipated ~200 pile-up events per bunch crossing at the HL-LHC, making vertex reconstruction complex

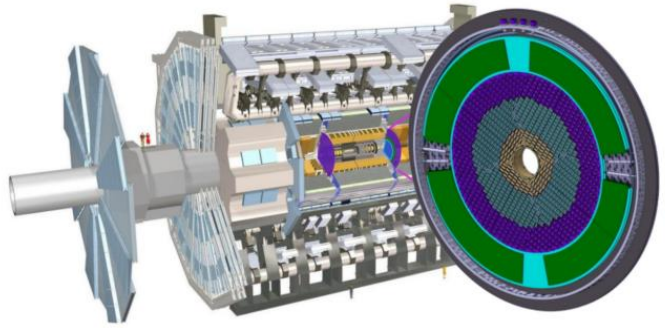
HL-LHC, and FCC-ee aim to achieve 4D particle reconstruction. Active R&D effort to developing sensors which can achieve



[1] Simulated collision at CMS in the HL-LHC

The ATLAS High Granularity Timing Detector (HGTD) aims to provide 4D reconstruction, to do this requires less than 30 ps timing resolution

Must withstand fluences up to 2.5×10^{15} n_eq/cm² over its operational lifetime.



[2] Diagram of the HGTD

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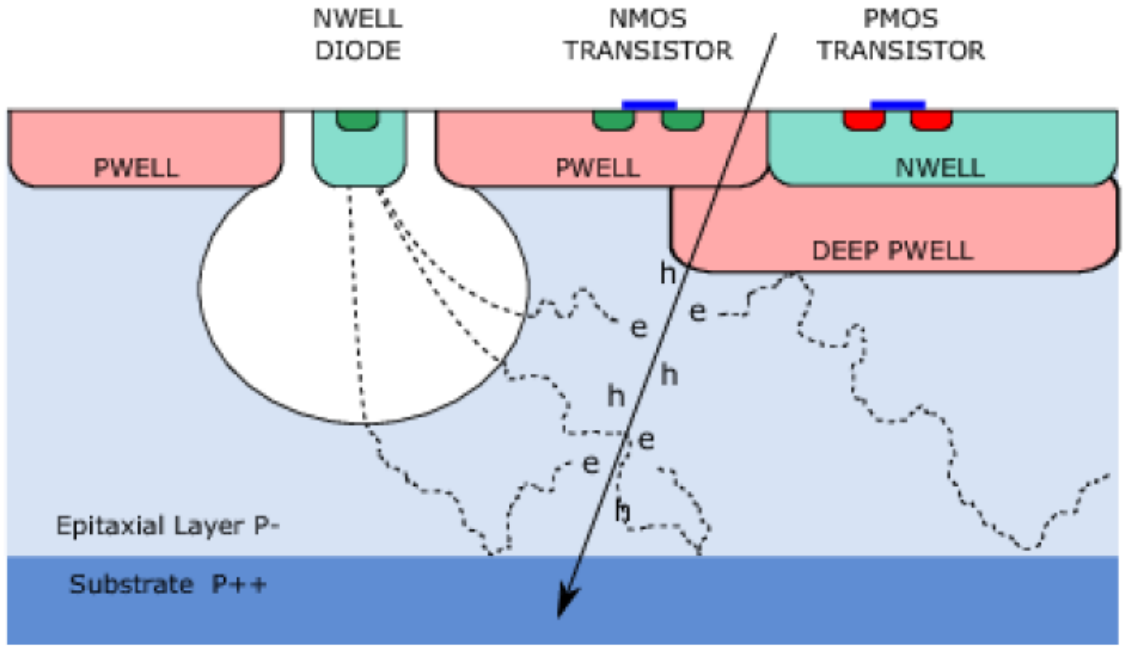
CMOS Sensors

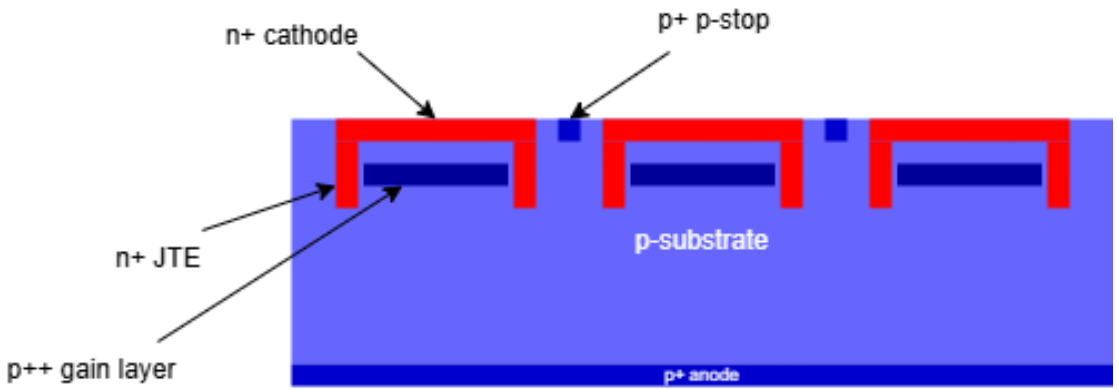
- Complimentary Metal-Oxide-Semiconductor (CMOS) is a silicon-based technology integrating sensing and readout onto one chip.
- Ionising particles generate electron hole pairs, in which the electrons drift or diffuse to the NWELL DIODE for collection.
- Has been used in the ITS upgrade at ALICE
- Cost effective, ease of manufacture, low material budget



[3] Diagram of CMOS used in ALICE

Low Gain Avalanche Detectors (LGADs)

- Modified n-on-p silicon sensor with internal gain, surrounded by a Junction Terminal Extention (JTE)
- High localised electric field generated within the gain layer, resulting in electron avalanche and ultimately an amplified signal
- Gain layer enables charge multiplication ~×10
- Time resolution: ~30–50 ps
- Hybrid technology: sensor + external ASIC
- Trade-offs: better timing vs. more material & scattering



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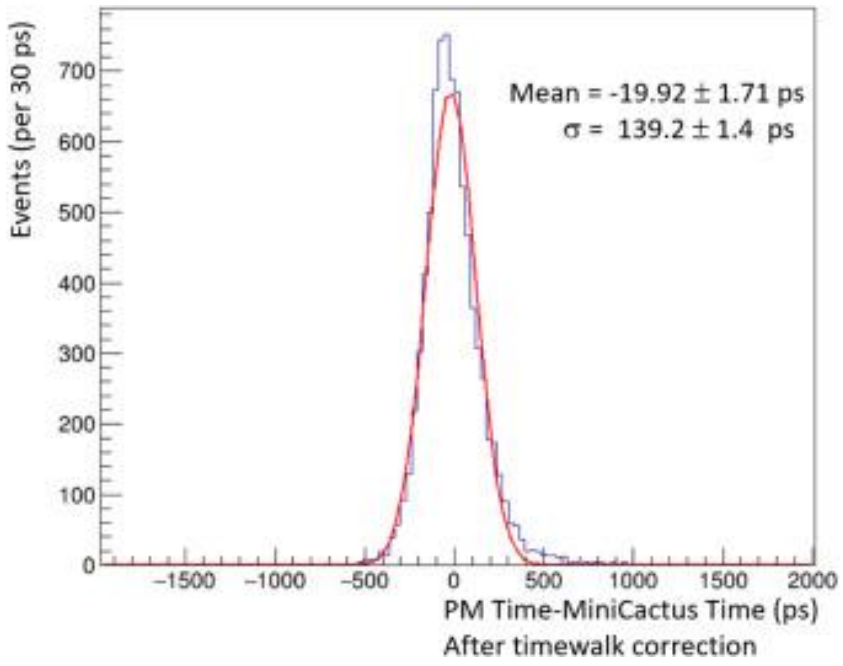
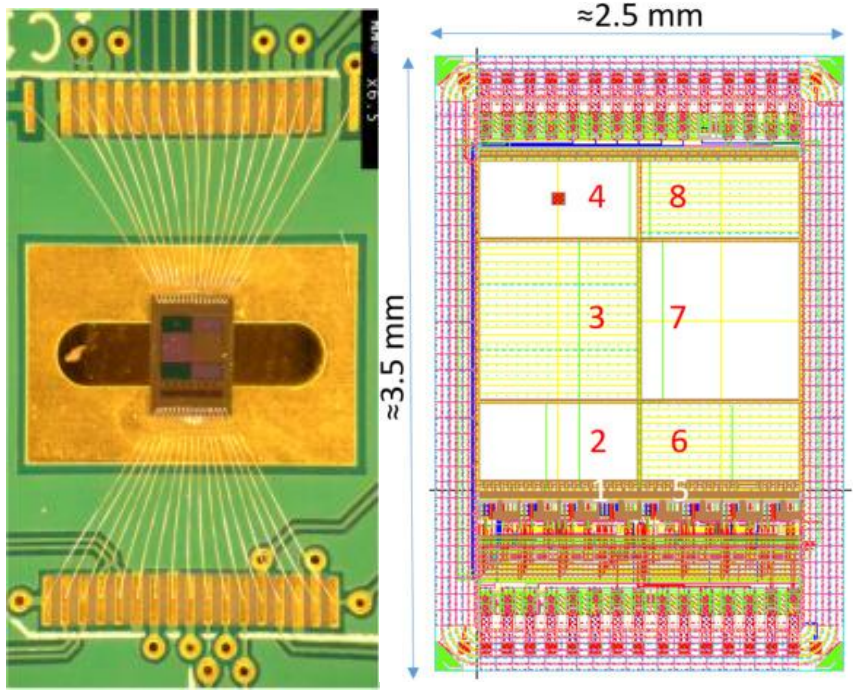
MiniCACTUS





[4] MiniCACTUS sensor

- Cmos ACtive pixel Timing Sensor (CACTUS).
- Analogue demonstrator with amplifier and comparator
- Time resolution of 80 ps observed in large pixels (3,7)
- Designed by IRFU, CEA, University Paris-Saclay and University of Bonn

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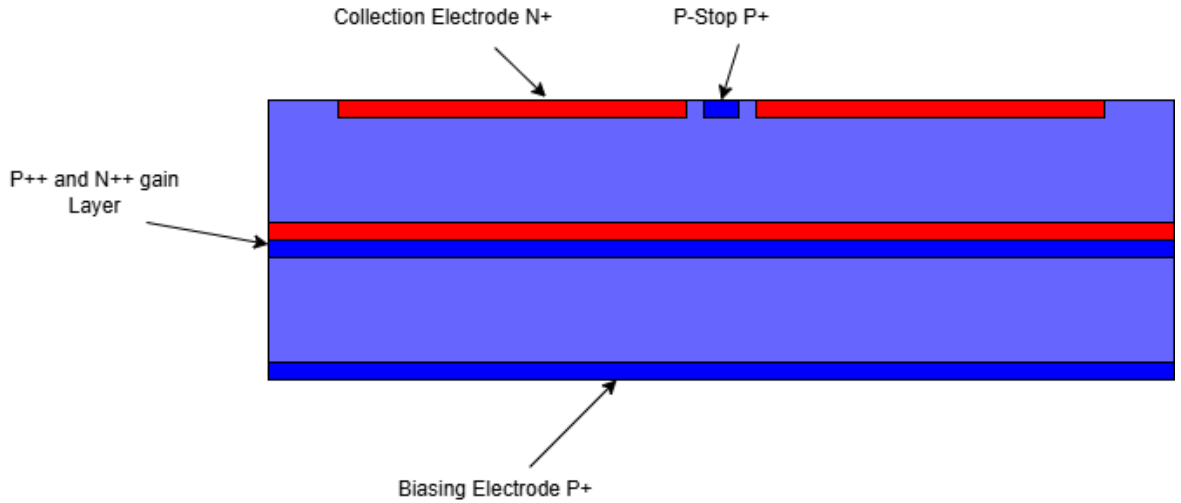
Cactus-GL

- Successor to miniCACTUS chip
- Monolithic Deep Junction LGAD (DJ-LGAD) fabricated in LFoundry 150nm process with custom gain layer implant. 150 microns thick
- same process used in Liverpool HV-CMOS group
- V0 chip, with aims to achieve 30ps timing



Cross section of typical structure within CactusGL

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Cactus-GL

- 6 different structures, each with two test diodes
- Been manufactures on two different high resistivity wafers, with different gain layer concentrations
- An epitaxial wafer has also been manufactured as a trial.

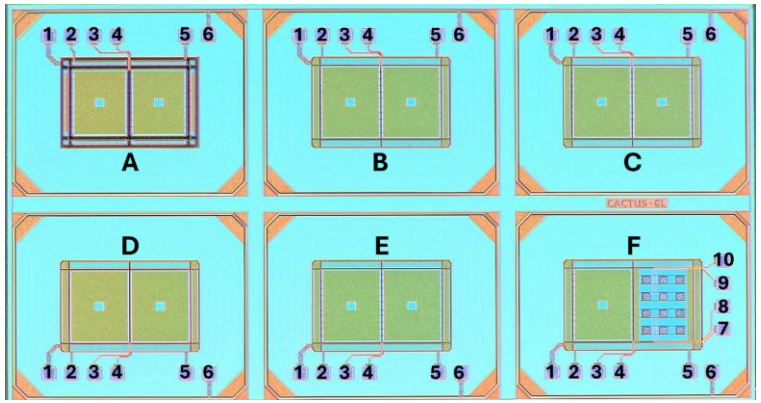

Image of the Cactus-GL Chip

Structure	Features
A	Reference Structure, no gain layer
B	Basic sensor with gain layer
C	Interpixel isolation handled by polysilicon ring rather than p-stop
D	Higher concentration n-well
E	Identical to structure B, with a different guard ring structure
F	AC LGAD – not currently being investigated

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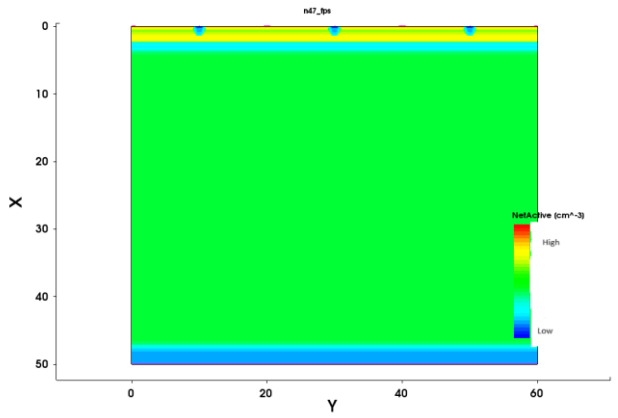
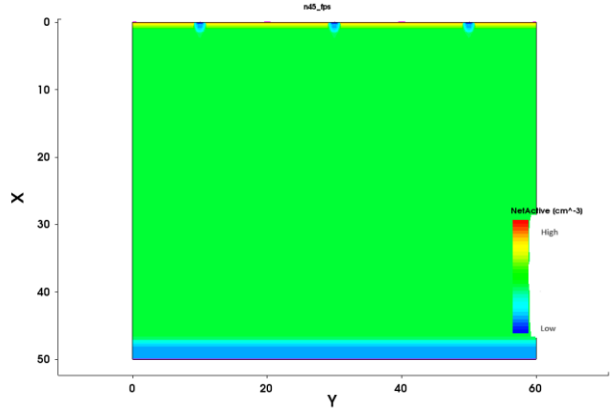
Technology Computer Aided Design (TCAD)

- Create a virtual sensor – enabling for design optimisation and testing
- Initially replicated the IRFU design for validation – observed consistent results
- Amplitude Gain factor of 4 is observed

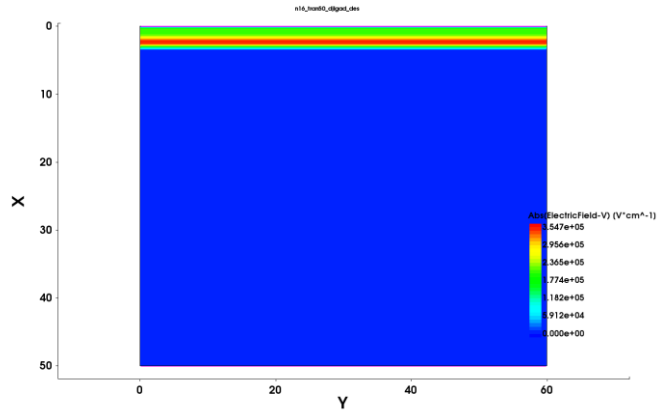
Doping profile of sensor with gain



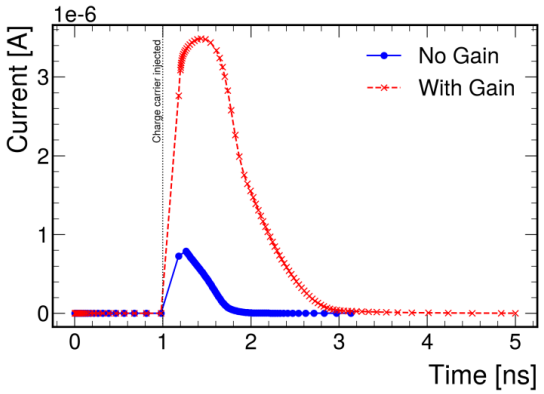
Doping profile of sensor without gain



Electric field in sensor with gain



Charge particle transient simulation



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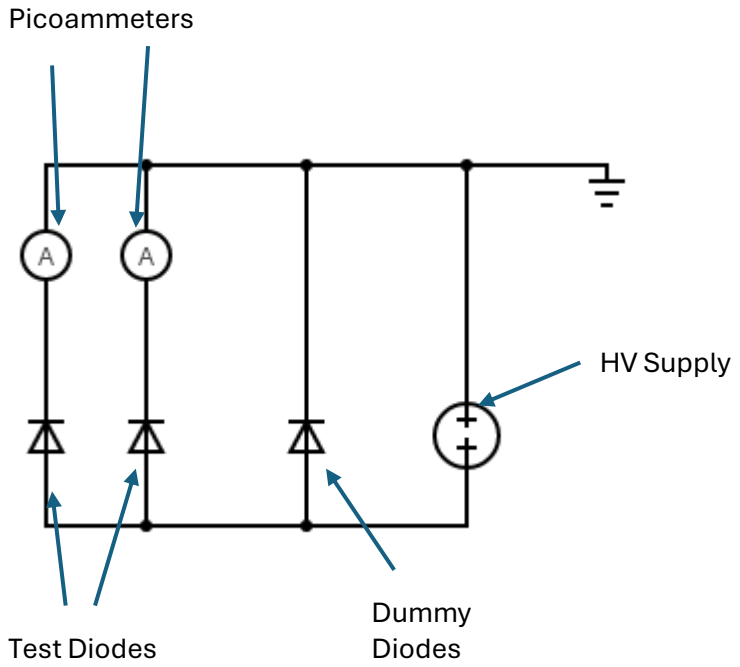
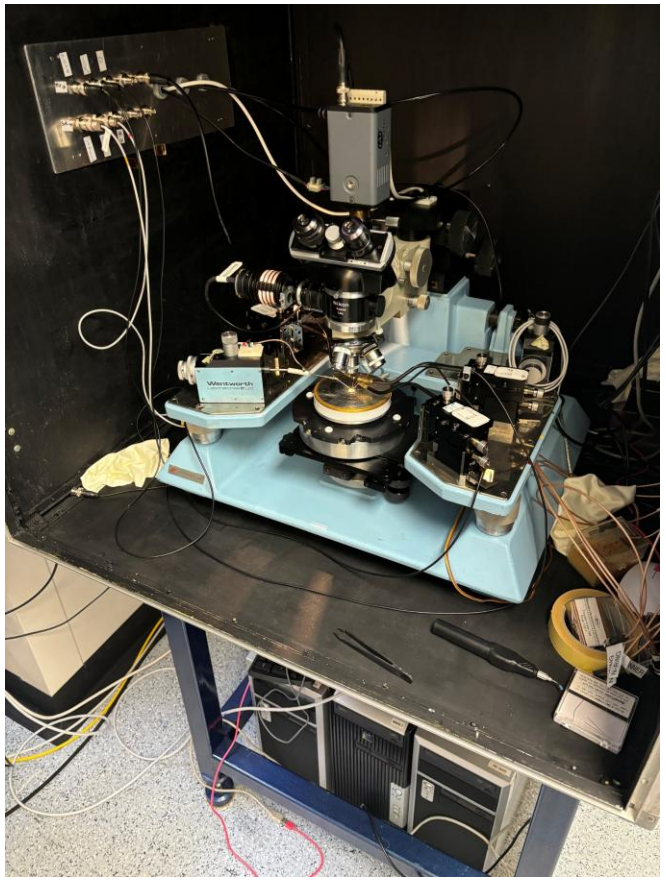
I-V Measurements

- Probe station within the clean room used to test the chips
- Needles placed on the pads, measuring both the left and right diodes, and grounding the dummy diodes.
- Multiple chips tested from each of the three manufactured wafers





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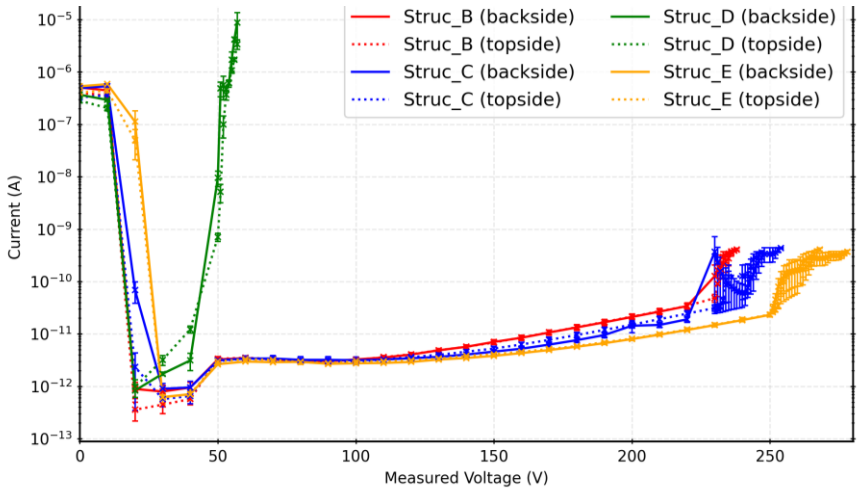
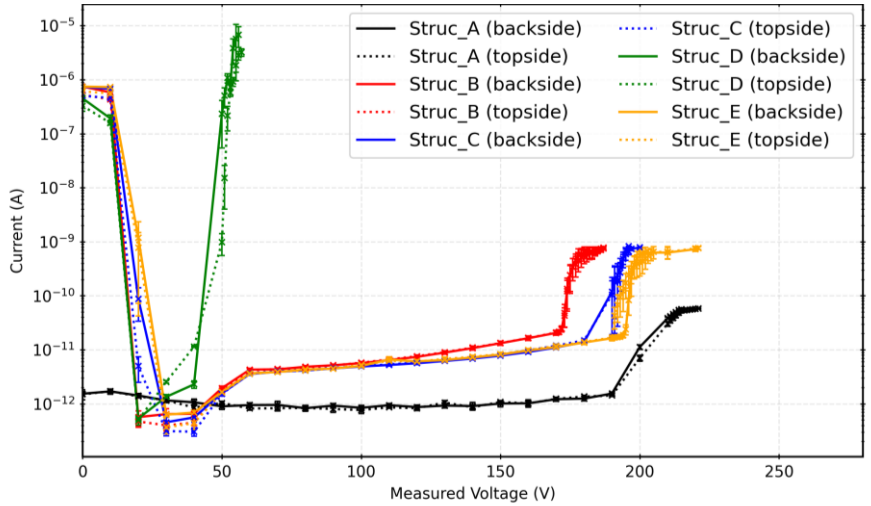
Lab Characterisation

HR wafer with low gain layer concentration



- Backside and topside biasing show similar breakdown behaviour
- Structure D breaks down at ~50 V, consistent across chip
- Structure A (reference) excluded – exhibited non-diode behaviour

HR wafer with high gain layer concentration



- Earliest breakdown seen in Structure D (~50 V)
- Higher gain implant increases field resulting in earlier breakdown

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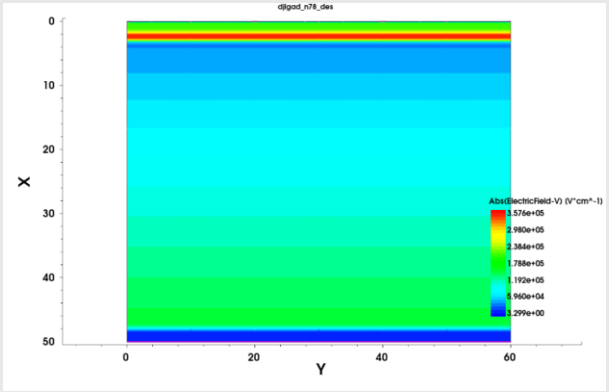
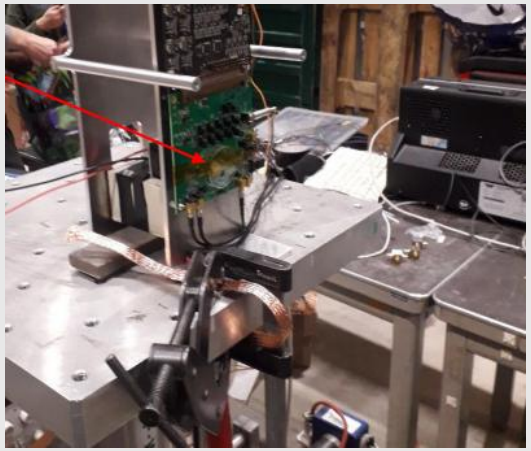
Future Work

TCAD Simulations

- Refine simulations to match measured data
- Sentaurus Calibration Workbench - ML-based surrogate models
- Enables efficient search of large design parameter spaces
- Will use to design future iterations of the Cactus-GL





Chip Characterisation

- Neutron irradiation of Cactus-GL samples (NIEL)
- Measure breakdown voltage, leakage current, gain degradation
- Simulate damage effects in TCAD prior to irradiation
- Partake in a test beam for the MiniCACTUS chip

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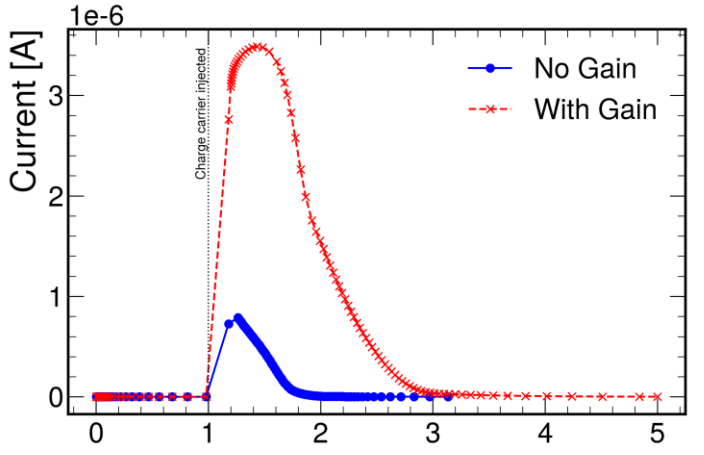
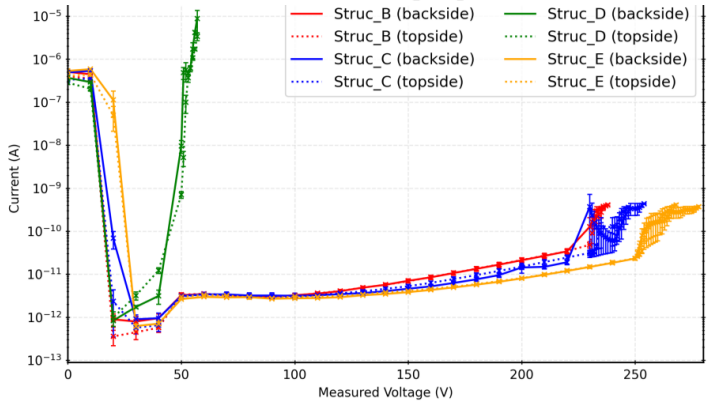
Conclusion

- Joined the CACTUS project
- Replicated simulations of the Cactus-GL chip
- Began lab characterisation of the performance of the Cactus-GL
- Refining simulations to match real data
- Began exploring Machine Learning methods to reduce computational expense of TCAD simulations





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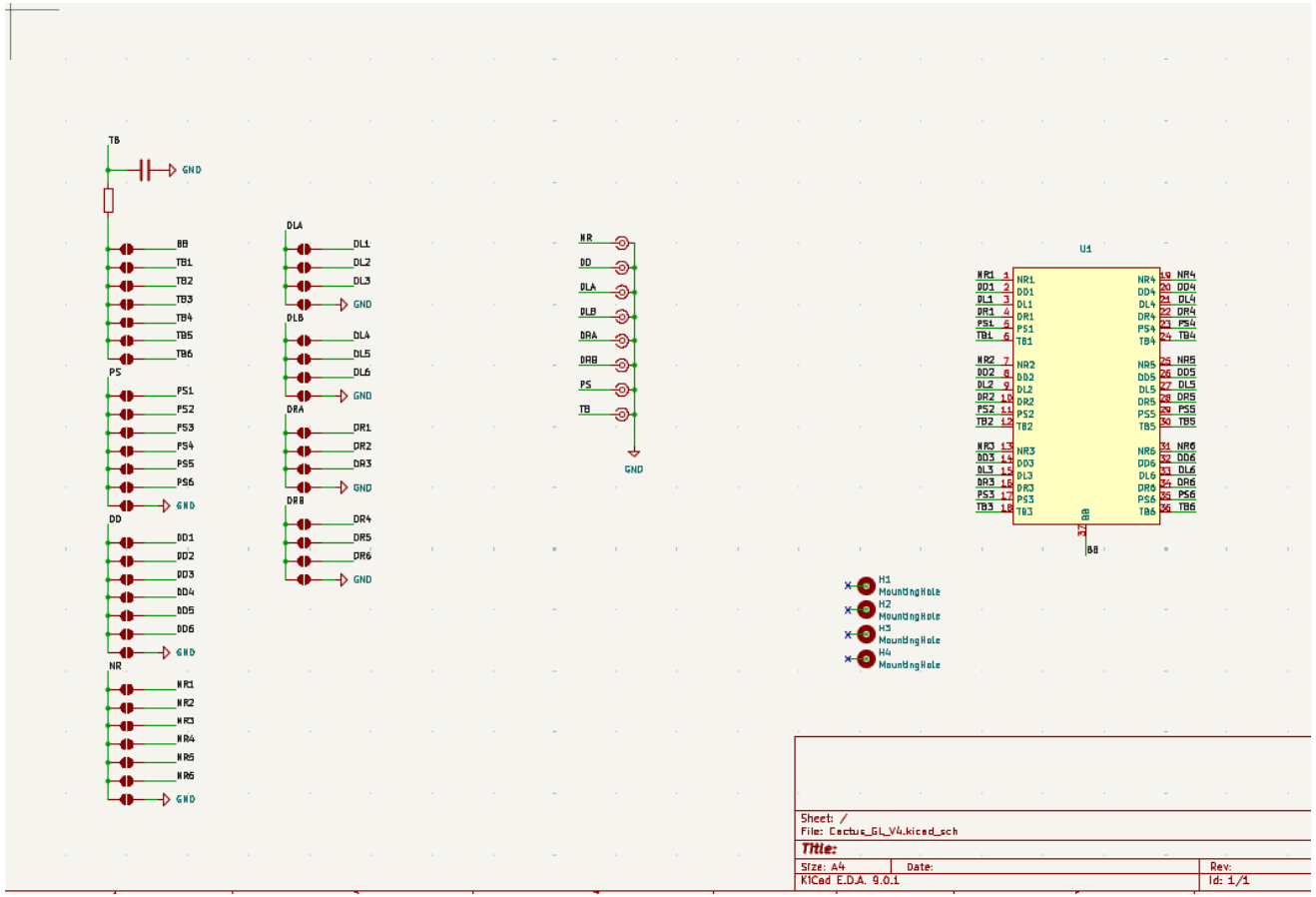
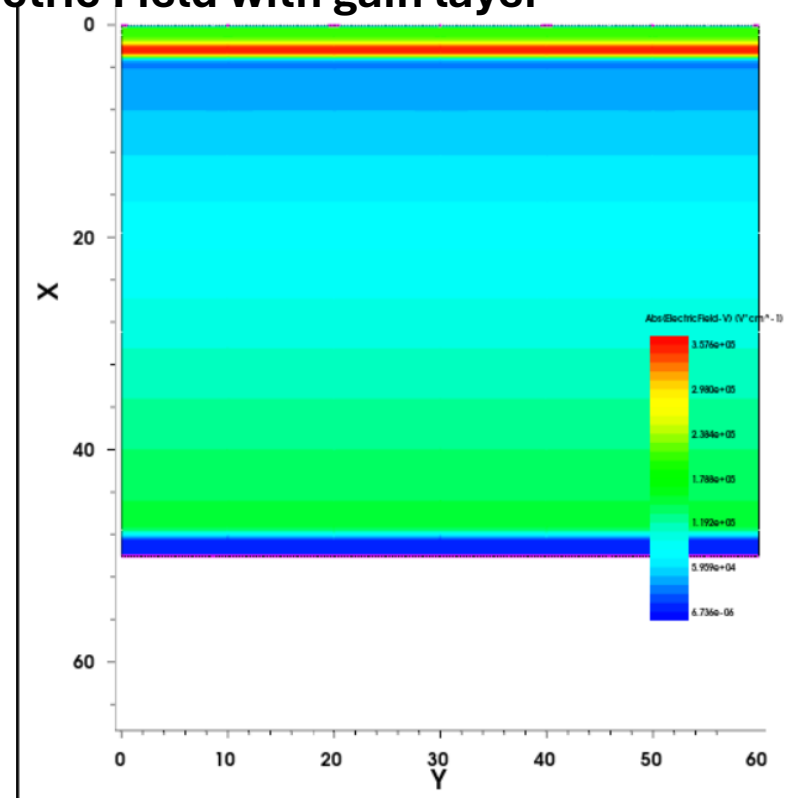
Backup: PCB Design

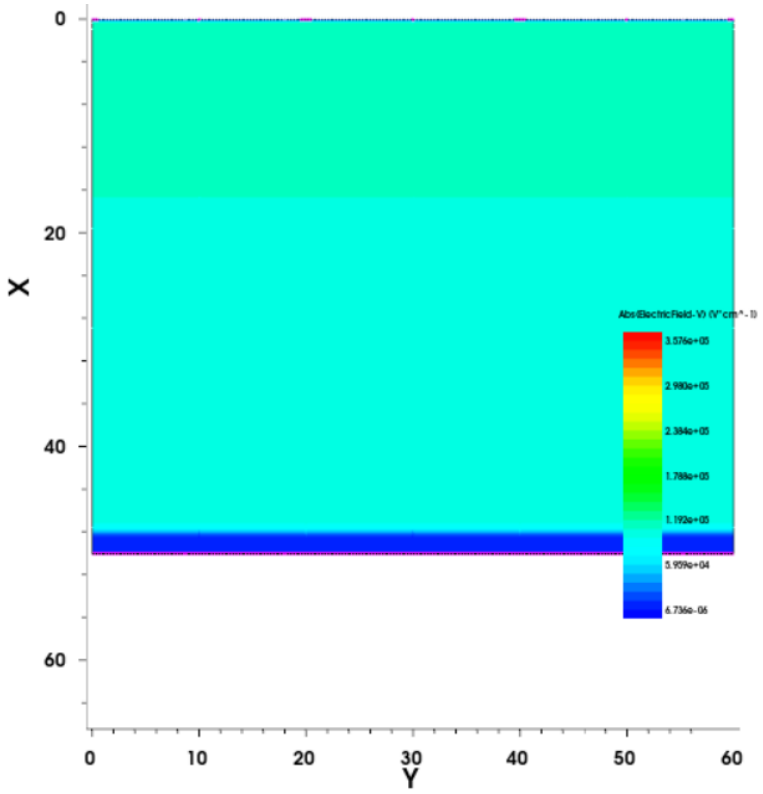


Backup: LGAD E-field

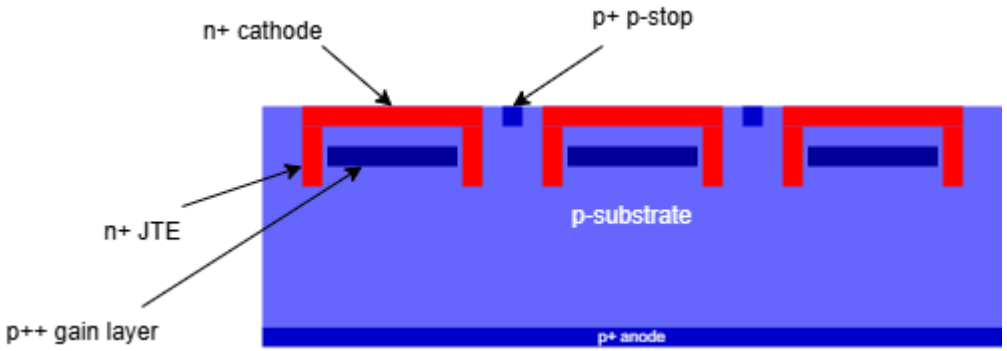
Electric Field with gain layer



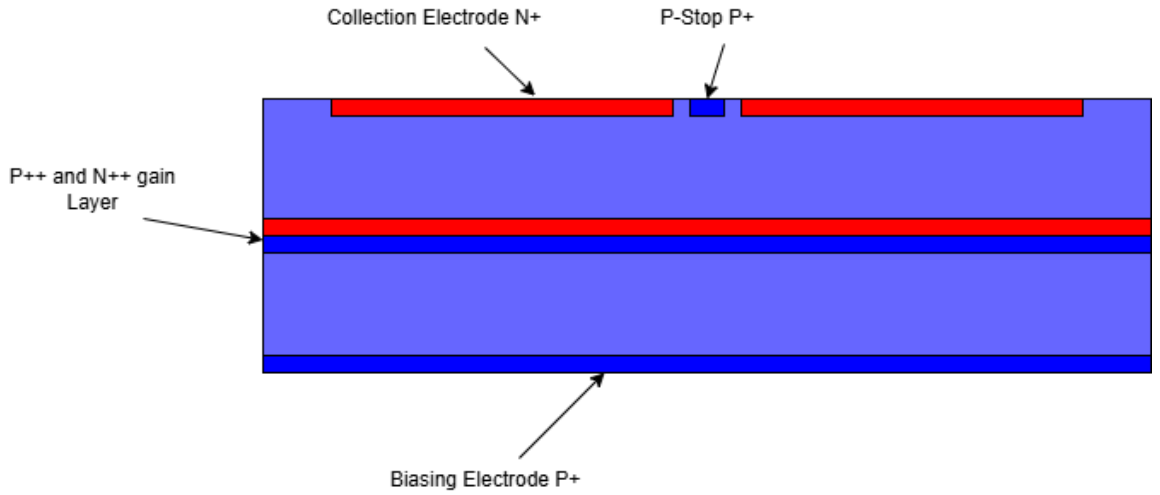
Electric Field without gain layer



Backup: Types of LGAD

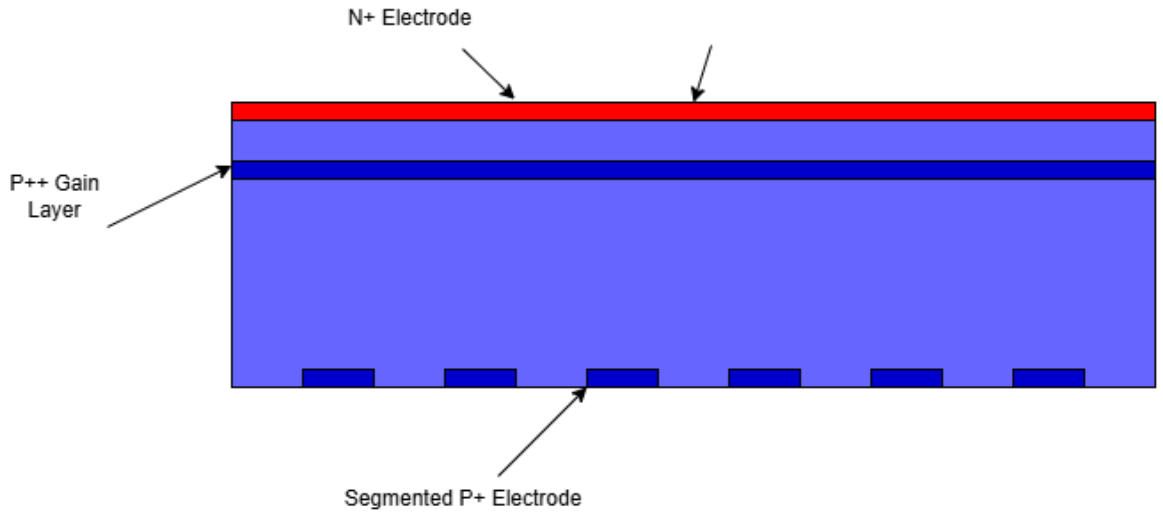


Standard LGAD



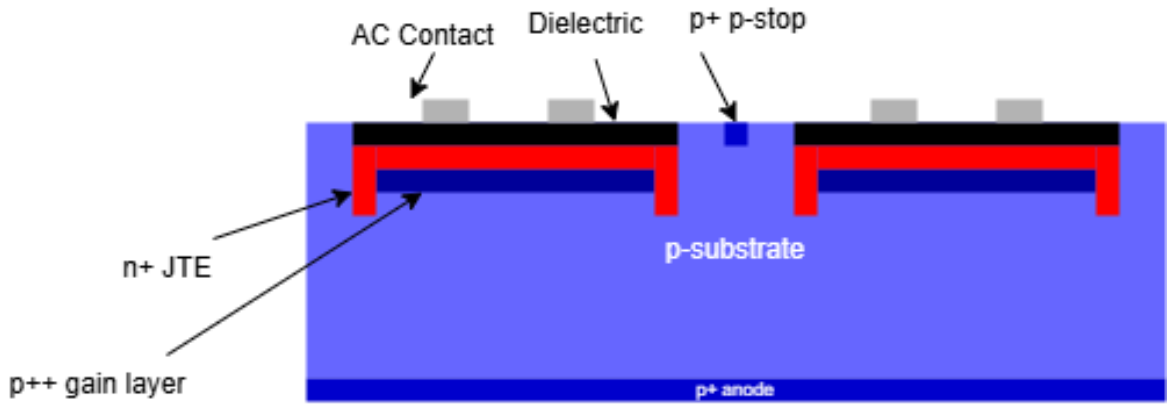
Deep Junction LGAD (DJ-LGAD)

Backup: Types of LGAD



AC-LGAD

Inverse LGAD (I-LGAD)



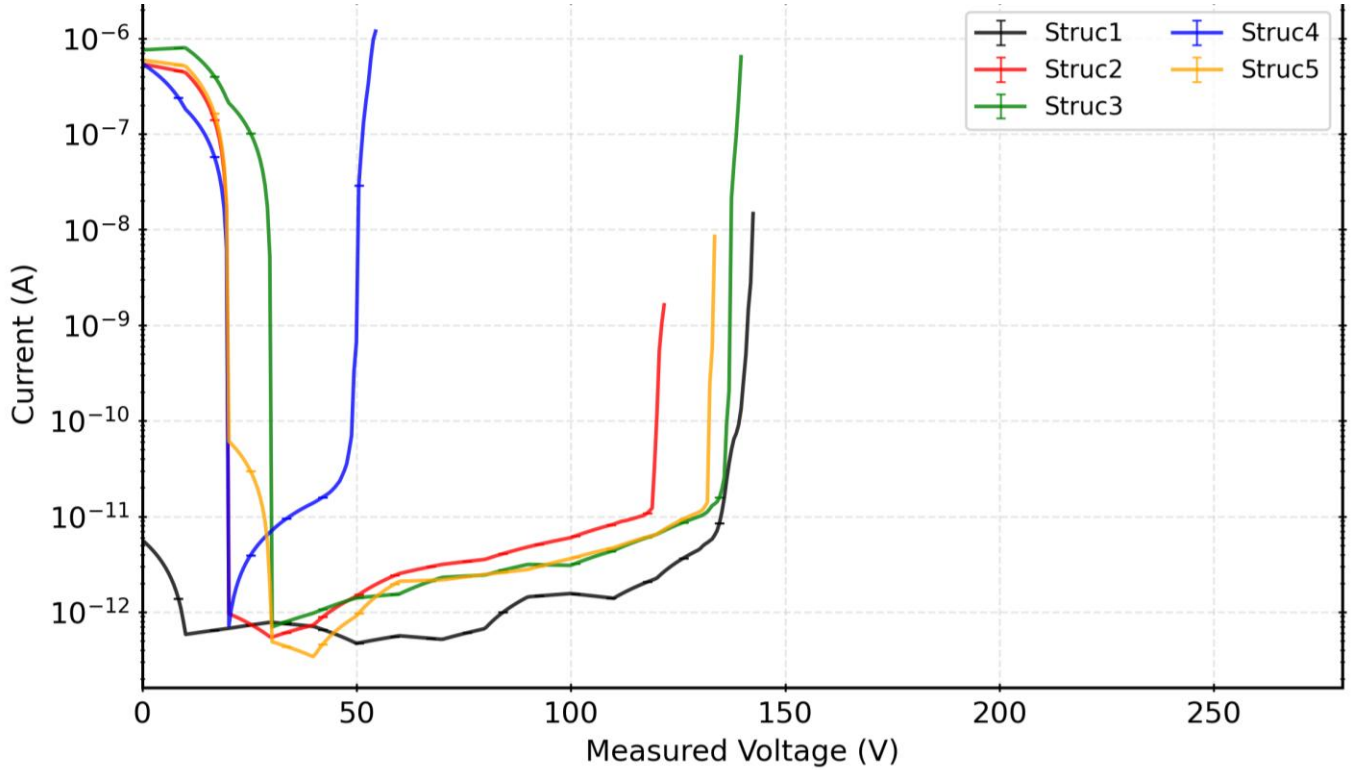
Backup: State of the Art Hybrid Detectors

Name	Sensor	Node [nm]	Pixel size [μm^2]	Temporal precision [ps]	Power [W/cm^2]
ETROC	LGAD	65	1300×1300	~40	0.3
ALTIROC	LGAD	130	1300×1300	~40	0.4
TDCpix	PIN	130	300×300	~120	0.32 matrix
TIMEPIX4	PIN, 3D	65	55×55	~200	0.3 digital
TimeSpot1	3D	28	55×55	~30	3–5

Backup: State of the Art Monolithic Detectors

Name	Sensor	Node [nm]	Pixel size [μm^2]	Temporal precision [ps]	Power [W/cm^2]
FASTPIX	MAPS	180	20×20	~130	5–10
miniCACTUS	MAPS	150	500×1000	~90	0.15–0.3
MonPicoAD	MAPS (SiGe)	130	100×100	~36	1.8
Monolith	MAPS (SiGe)	130	100×100	~25	0.9

Backup: Epitaxial Wafer



References

1. *Timing Detectors – v3"*, presented at **Fermilab Indico event 54596**, 2022, available at: *Precision Timing Detectors in Collider Experiments* (Timing Detectors – v3))
2. Image credit: ATLAS Collaboration, CERN (https://twiki.cern.ch/twiki/bin/view/AtlasPublic/UpgradeEventDisplays)
3. Reidt, F. (2022). *Upgrade of the ALICE ITS detector*. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 1032, 166632. https://doi.org/10.1016/j.nima.2022.166632
4. Y. Degerli, F. Guilloux, T. Hemperek, J.-P. Meyer, P. Schwemling. MiniCACTUS: Sub-100 ps timing with depleted MAPS; Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 2022, *1039*, 167022. Available online: https://www.sciencedirect.com/science/article/pii/S0168900222004478 (accessed on 17 June 2025).