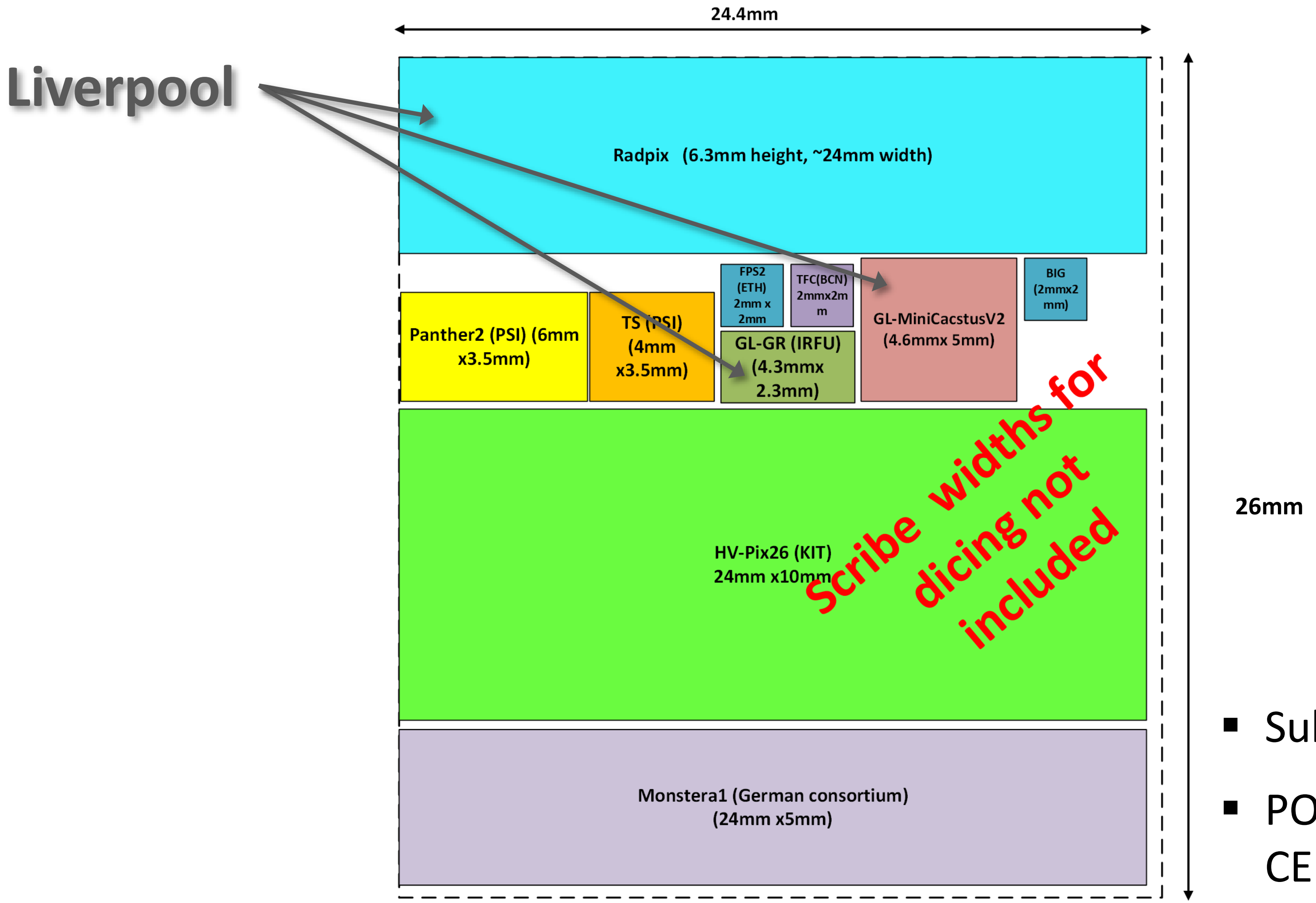
DRD3 Community Shared Submission in LF15A Technology

Eva Vilella, University of Liverpool

- For more details, please see presentation during last DRD3 Collaboration Week (here).

Full mask-set run

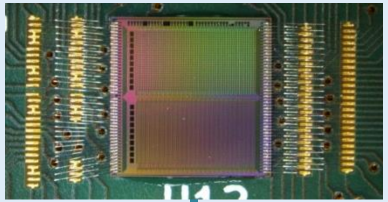
Preliminary



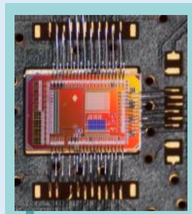
- Submission in Q2 2026
- PO being rised through CERN

Liverpool LFoundry HV-CMOS R&D

CERN-RD50

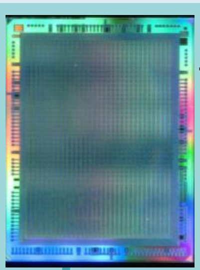


RD50-MPW1
- 50 µm x 50 µm pixels
- Digital RO in sensing diode
- Topside HV biasing
- V_{BD} = 56 V, large I_{LEAK}

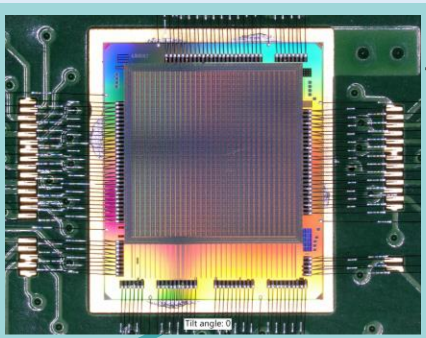


RD50-MPW2
- 60 µm x 60 µm pixels
- Analogue RO only
- Topside HV biasing
- V_{BD} = 120 V, small I_{LEAK}

AIDAinnova

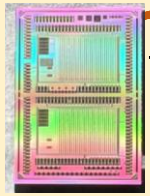


RD50-MPW3
- 62 µm x 62 µm pixels
- 64 x 64 pixels matrix
- Digital RO in sensing diode
- Digital periphery
- In-pixel high-noise due to power & grounding issue
- Topside HV biasing
- V_{BD} = 120 V, small I_{LEAK}

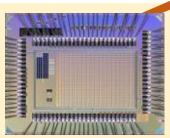


RD50-MPW4
- 62 µm x 62 µm pixels
- 64 x 64 pixels matrix
- Digital RO in sensing diode
- Digital periphery
- In-pixel low-noise
- **Improved chip rings**
- **Backside HV biasing**
- **V_{BD} > 600 V, small I_{LEAK}**

2017 – 2018 – 2019 – 2020 – 2021 – 2022 – 2023 – 2024 – 2025 – 2026 – +



UKRI-MPW0
- 60 µm x 60 µm pixels
- Analogue RO only
- **Alternative sensor cross-section** (w/o p-isolation between pixels) **and chip rings** (current terminating type)
- **Backside HV biasing**
- **V_{BD} > 600 V (thermal runaway), large I_{LEAK}**



UKRI-MPW1
- 60 µm x 60 µm pixels
- Analogue RO only
- **Improved alternative sensor cross-section** (w/ p-shield style isolation between pixels) **and chip rings** (as in RD50-MPW4)
- **Backside HV biasing**
- **V_{BD} > 600 V, small I_{LEAK}**

RadPix

RadPix
- Being designed
- DRD3/LHCb UG2

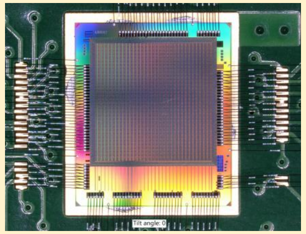
Liverpool line
- Market survey completed in 2023 (nuclear, medical & space)
- Patents filed in the US and Europe
- Commercial flyer

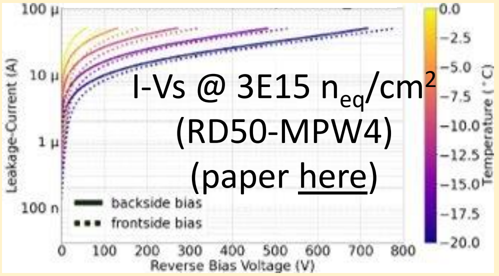
More in Stephen's talk

All chips thinned to 280 µm

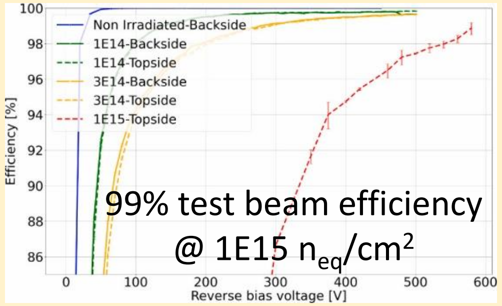
RadPix

Previous R&D

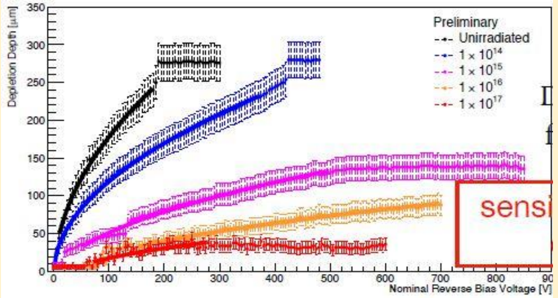




I-Vs @ 3E15 n_{eq}/cm^2 (RD50-MPW4) (paper here)



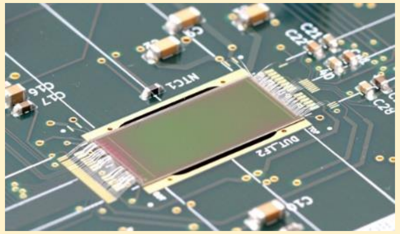
99% test beam efficiency @ 1E15 n_{eq}/cm^2



Depletion depth ≤ 1E17 n_{eq}/cm^2 (UKRI-MPW1=RD50-MPW4's brother)

RD50-MPW4

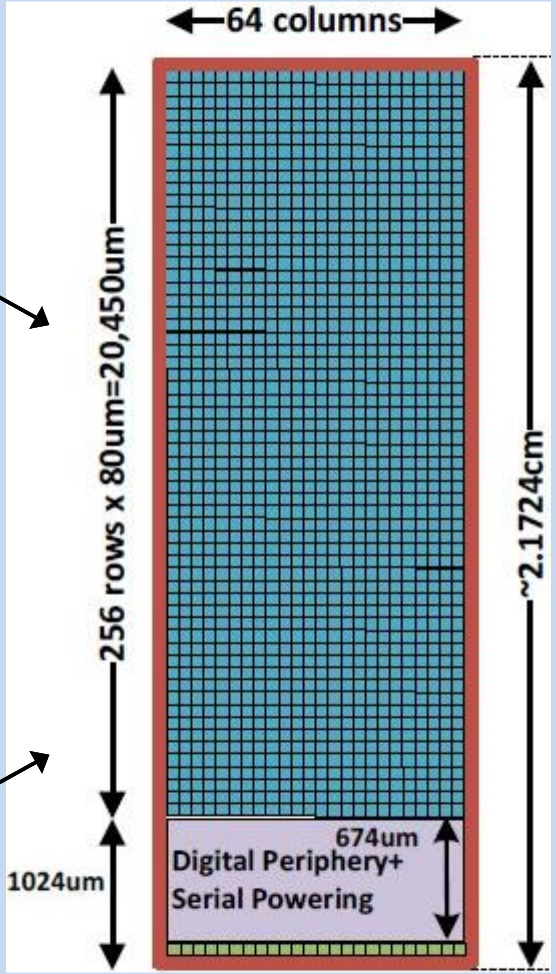
- 62 µm x 62 µm pixels
- 64 x 64 pixels matrix
- Digital RO in sensing diode
- In-pixel low-noise
- Large digital periphery
- Large power consumption
- Improved (wide) chip rings
- V_{BD} > 600 V, small I_{LEAK}
- Backside HV biasing
- 280 µm thickness
- 2 kΩ·cm HR substrate



LF-MonoPix2

- 150 µm x 50 µm pixels
- 340 x 56 pixels matrix
- Digital RO in sensing diode
- Large sensor capacitance (noise)

Design team: S. Benhammadi[a], R. Casanova[b], Y. Degerli[c], H. Elnashari[d], N. Guerrini[a], T. Gao[e], F. Guilloux[c], K. Hennessy[f], S. Powell[f], E. Vilella[f], C. Zhang[f]
STFC TD[a], UAB[b], IRFU-CEA[c], Uni. Glasgow[d], Uni. Cambridge[e], Uni. Liverpool[f]



RadPix1

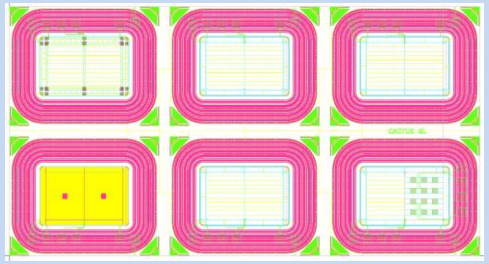
- 80 µm x 80 µm pixels
- 256 x 64 pixels matrix
- Digital RO in sensing diode
- In-pixel low-noise
- Optimised digital periphery
- 1.28 Gb/s serial link
- Serial powering
- 150 mW/cm^2 power consumption
- Optimised (narrow) chip rings
- Large V_{BD}, small I_{LEAK}
- Backside HV biasing
- 100-200 µm thickness
- 5E15 n_{eq}/cm^2 target

Evaluation plans

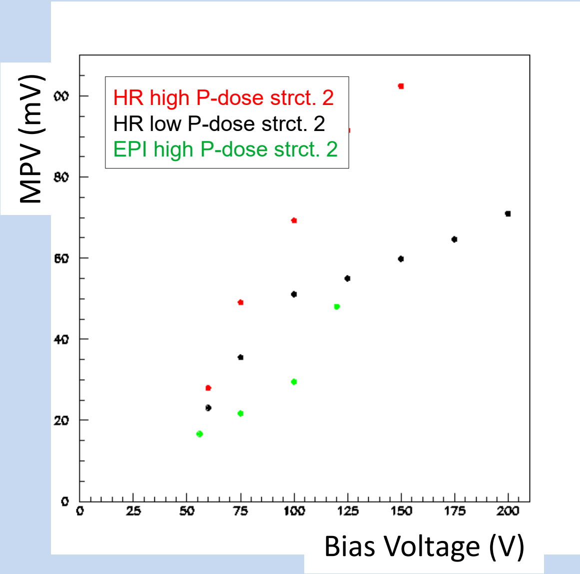
- I-V curves
- Pixel matrix with test pulses and radioactive sources
- Chip periphery
- Serial powering with >1 chip
- Irradiation studies and test beam evaluation

GL-GR

Design team: Yavuz Degerli[a], Fabrice Guilloux[a], Raimon Casanova[b], Pablo Fernandez[c], Juan Ignacio Drovandi[c], Archie Hanlon[d], Eva Vilella[d]
IRFU[a], IFAE[b], IMB-CNM[c], Uni. Liverpool[d]



4.3 mm x 2.3 mm



GL GR

- Improved Gain Layer test structures
- Need two customer reserved layers for gain layer implementation
- 6 diodes, each split in half diode
- Precision timing

Evaluation plans

- In lab: 90-Sr and IR laser
- IV
- Measurements of amplitude vs HV

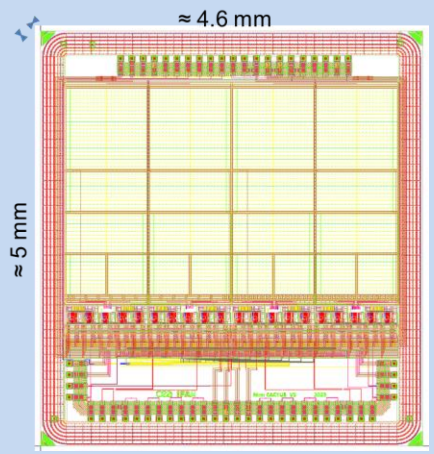
See two DRD3 presentations:

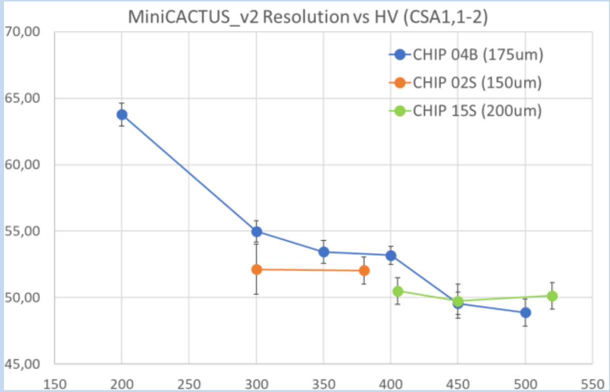
- "Testbeam results of the MiniCactus V2 timing demonstrator", J. Pinol
- "Development of sensors with intrinsic gain in LFoundry 150 nm technology", P. Schwemling

Interested chips

GL-MiniCactusV2

Design team: Yavuz Degerli[a], Fabrice Guilloux[a], Raimon Casanova[b]
IRFU[a], IFAE[b]





GL-MiniCactusV2

- Study of diodes with intrinsic amplification and integrated FE
- 4.6 mm x 5 mm chip
- Integrated slow control
- Programmable FE
- Two customer-layers needed for gain layer
- Special passivation also needed (use of MT layer)
- Two columns of pixels, organised in half columns
- Precision timing (< 50 ps)

Evaluation plans

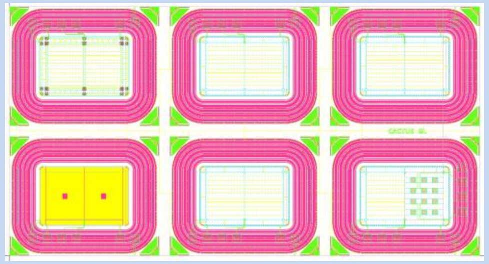
- In lab: 90-Sr and IR laser
- Test beam
- Signal amplitude and time resolution measurements

See two next presentations:

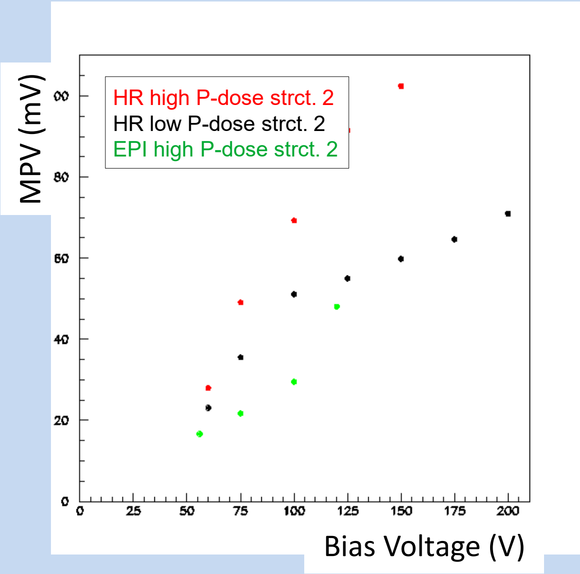
- "Testbeam results of the MiniCactus V2 timing demonstrator", J. Pinol
- "Development of sensors with intrinsic gain in LFoundry 150 nm technology", P. Schwemling

GL-GR

Design team: Yavuz Degerli[a], Fabrice Guilloux[a], Raimon Casanova[b], Pablo Fernandez[c], Juan Ignacio Drovandi[c], Archie Hanlon[d], Eva Vilella[d]
IRFU[a], IFAE[b], IMB-CNM[c], Uni. Liverpool[d]



4.3 mm x 2.3 mm



GL GR

- Improved Gain Layer test structures
- Need two customer reserved layers for gain layer implementation
- 6 diodes, each split in half diode
- Precision timing

Evaluation plans

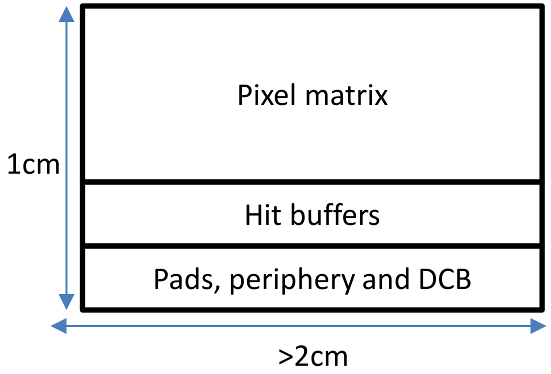
- In lab: 90-Sr and IR laser
- IV
- Measurements of amplitude vs HV

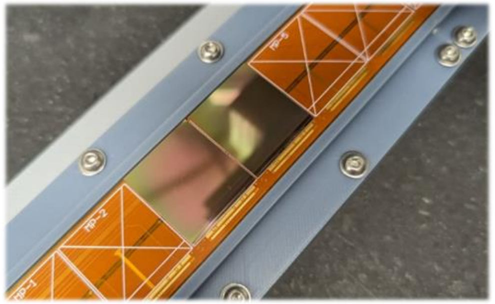
See two next presentations:

- "Testbeam results of the MiniCactus V2 timing demonstrator", J. Pinol
- "Development of sensors with intrinsic gain in LFoundry 150 nm technology", P. Schwemling

HV-Pix26

Design team: Nicolas Striebig, Alexander Elsenhans, Christian Krämer, Richard Leys, Ilona Münnich, Miaoran Sun, Yue Su, Bowen Xu, Ivan Peric (KIT, Karlsruhe, Germany)





HVCMOS Sensor MuPix for Mu3e

HVCMOS Sensor AstroPix for Compton telescope

Motivation:

HV-CMOS sensors are being developed for use in several cutting-edge applications, including particle physics experiments, a planned Compton telescope, and ion beam therapy.

The **LFoundry** technology provides several key advantages:

Use of substrates with resistivity > 2 kΩ, capability for full substrate depletion, integration of CMOS electronics within a deep n-well, availability of a deep p-well.

These features enable high performance and flexibility, making the technology well-suited for a range of demanding detector applications

Specifications:

- Low-power operation
- Fully depleted thick substrate – essential for Compton telescope applications
- Daisy-chain readout, serial powering, module compatibility

Chip components:

- Pixel matrix, digital hit buffers, digital control block (DC B)

Applications:

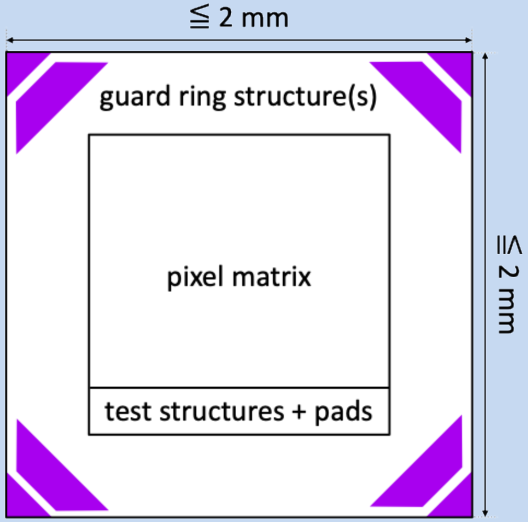
- Use in particle physics experiments, gamma space telescope, beam monitoring for ion therapy

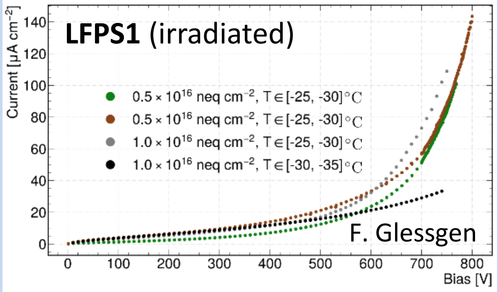
Evaluation plans:

- Performance will be characterised through laboratory measurements and test beam studies, including activities within the DRD project: “HV-CMOS Pixel Detector Demonstrator with Serial Powering.”

LFPS2

Design team: M. Franks, B. Ristic, M. Backhaus
ETH Zurich





LFPS2

- **Motivation:** Exploration of CMOS chips with AC-coupled pixels as passive sensors in hybrids
- **Specifications:** Minimum 2 mm × 2 mm area (flexible), 1 or more substrate resistivities
- **Description:** Passive sensor with AC-coupled pixels, compatible with 28 nm readout chips for hybridisation
- **Research goals:** Evaluate alternate hybridisation methods, demonstrate a radiation tolerance suitable for CMS L2 after LS4, or FCC-ee

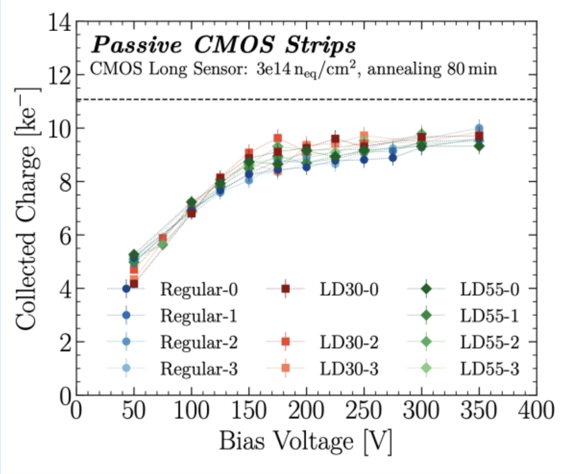
Evaluation plans

- I-V measurements
- Hybridisation
- ROC + sensor characterisation
- Irradiation campaign
- Test beams

Monstera1

Design team: Ivan Peric, KIT, NN, Bonn

Depending on availability
5mm x 10 mm would be nice



Monstera1

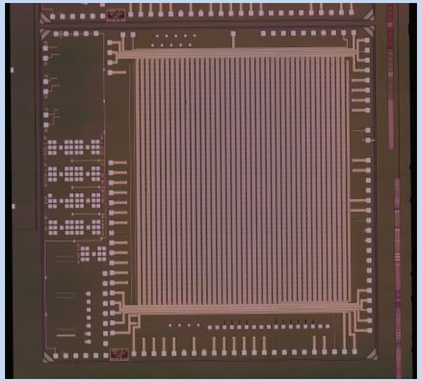
- MONolithic STrip Extended Readout Architecture
- Existing (passive) CMOS strip sensors extensively studied, results well published (e.g. NIM A 1061 (2024) 169132, NIM A 1064 (2024) 169407)
- Up to 60 strips with 75 µm width based on an existing CMOS strips design
- Each strip will have a front-end directly implemented making this an “active strips sensor”
- Front-end design will be based on the Telepix2 design with implemented amplifier and comparator.

Evaluation plans

- Testing in the lab with the usual techniques (incl. source measurements)
- Test beam studies

Panther2 + TS

Design team: A. Ebrahimi[a], A. Ghimouz[a], H. Kästli[a], B. Meier[a], E. Monteil[a], T. Rohe[a], P. Sander[b]
PSI[a] ,ETHZ[a]



Previous R&D – Panther1
- First prototype submitted 2024
- Currently under test
- **Panther2** will be similar in size, improved sensor/front-end performance

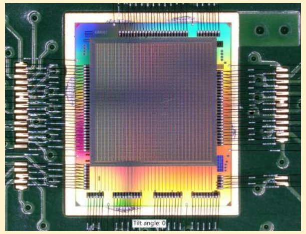
Panther2
- DMAPS with time of arrival measurement
- σ(t)<1ns
- PSI experiments
- Low rate, low radiation
- Test structures
  - GRs
  - Edge TCT

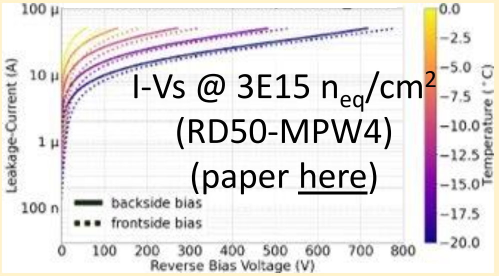
Evaluation plans
- Characterization with newly commissioned DAQ system in lab and test beam
- Measurement of σ(t) versus
  - Frontend flavour (3)
  - Chip settings
  - Position of track

RadPix

Design team: S. Benhammadi[a], R. Casanova[b], Y. Degerli[c], H. Elnashari[d], N. Guerrini[a], T. Gao[e], F. Guilloux[c], K. Hennessy[f], S. Powell[f], E. Vilella[f], C. Zhang[f]
STFC TD[a], UAB[b], IRFU-CEA[c], Uni. Glasgow[d], Uni. Cambridge[e], Uni. Liverpool[f]

Previous R&D

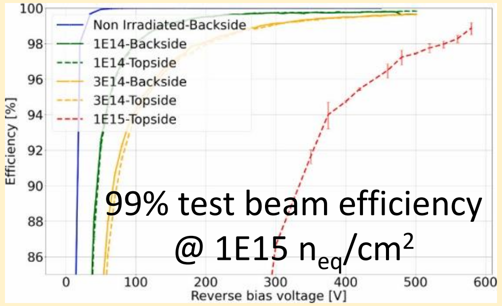




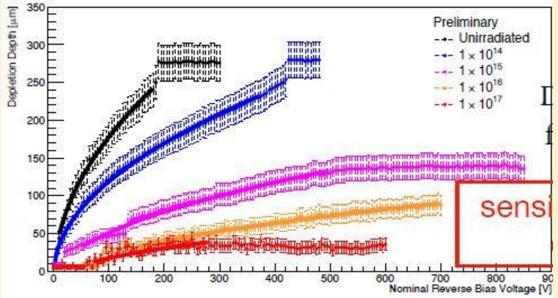
I-Vs @ 3E15 n_{eq}/cm^2 (RD50-MPW4) (paper here)

RD50-MPW4

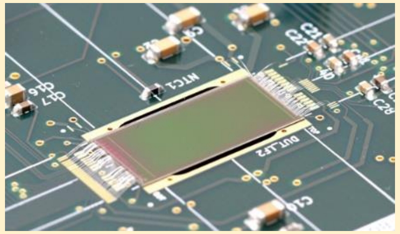
- 62 µm x 62 µm pixels
- 64 x 64 pixels matrix
- Digital RO in sensing diode
- In-pixel low-noise
- Large digital periphery
- Large power consumption
- Improved (wide) chip rings
- V_{BD} > 600 V, small I_{LEAK}
- Backside HV biasing
- 280 µm thickness
- 2 kΩ·cm HR substrate



99% test beam efficiency @ 1E15 n_{eq}/cm^2

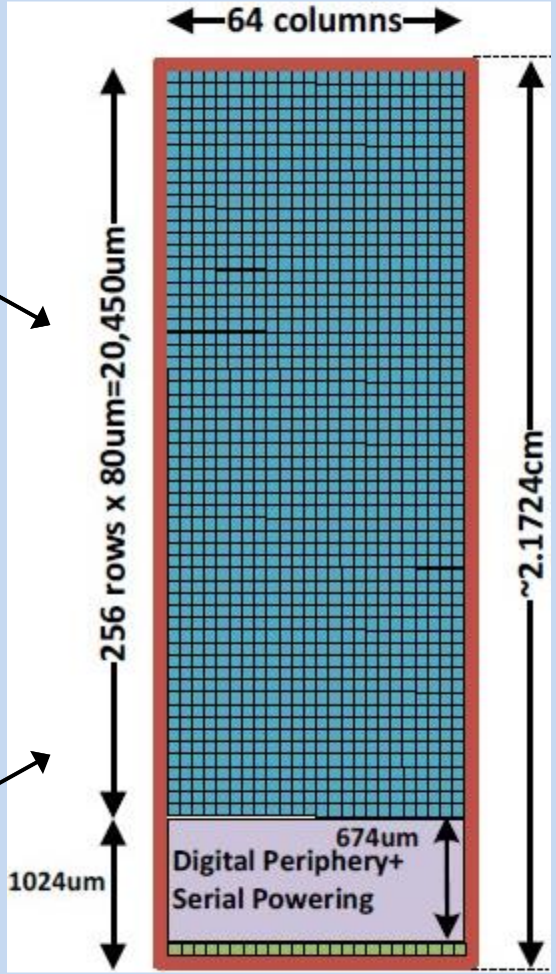


Depletion depth ≤ 1E17 n_{eq}/cm^2 (UKRI-MPW1=RD50-MPW4's brother)



LF-MonoPix2

- 150 µm x 50 µm pixels
- 340 x 56 pixels matrix
- Digital RO in sensing diode
- Large sensor capacitance (noise)



RadPix1

- 80 µm x 80 µm pixels
- 256 x 64 pixels matrix
- Digital RO in sensing diode
- In-pixel low-noise
- Optimised digital periphery
- 1.28 Gb/s serial link
- Serial powering
- 150 mW/cm^2 power consumption
- Optimised (narrow) chip rings
- Large V_{BD}, small I_{LEAK}
- Backside HV biasing
- 100-200 µm thickness
- 5E15 n_{eq}/cm^2 target

Evaluation plans

- I-V curves
- Pixel matrix with test pulses and radioactive sources
- Chip periphery
- Serial powering with >1 chip
- Irradiation studies and test beam evaluation

Summary

- We are organising a DRD3 community shared submission in the 150 nm High Voltage CMOS process (LF15A) from LFoundry.
- This joint submission will include several chips designed by the DRD3 community.
- We are discussing with LFoundry the submission details, including the submission area.
- The chip design work is currently ongoing and the tape-out is tentatively planned for spring 2026.