MT chips and DAQ

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Overview

- RadPix1 design objectives
- Top level block diagram
- Matrix and pixel optimisation
- Readout periphery
- Voltage regulators for serial powering and LVDS

RadPix1 design objectives

Main objectives of RadPix1

1- Meet power density:

- Power optimization of the pixel (150 mW/cm^2), while keeping 99% in-time efficiency within 25ns.

2- Meet 95% of sensitive area on the full sensor scale:

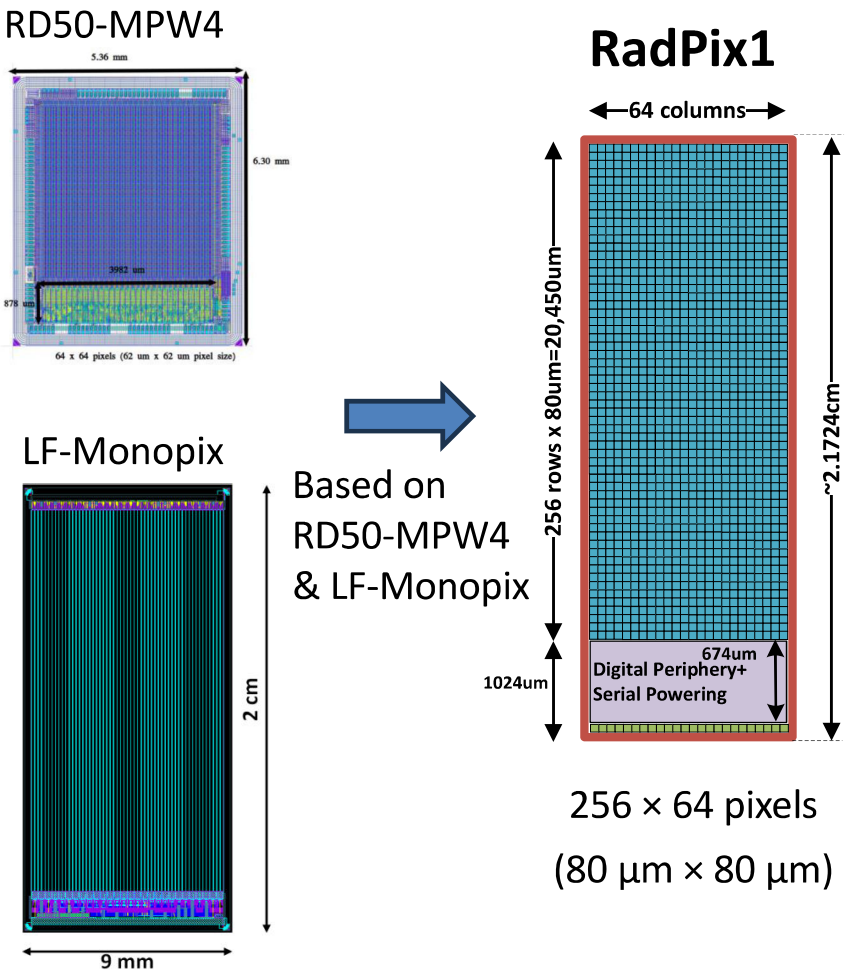
- Careful floor planning of the pixel array and the periphery circuits (Digital Readout + Serial Powering)

3- Upgrade the digital periphery:

- Align to LHCb communication protocols.
- Follow a sensible approach to reduce power consumption.
- Follow a sensible radiation tolerance design strategy.

4- Porting and developing necessary IPs:

- Serial powering, LVDS drivers and receivers, Power-on-Reset.



Top level block diagram

The RadPix sensor design is divided into a few work packages:

WP1) Pixel Matrix:

- Optimisation of the Pixel array size and power consumption.

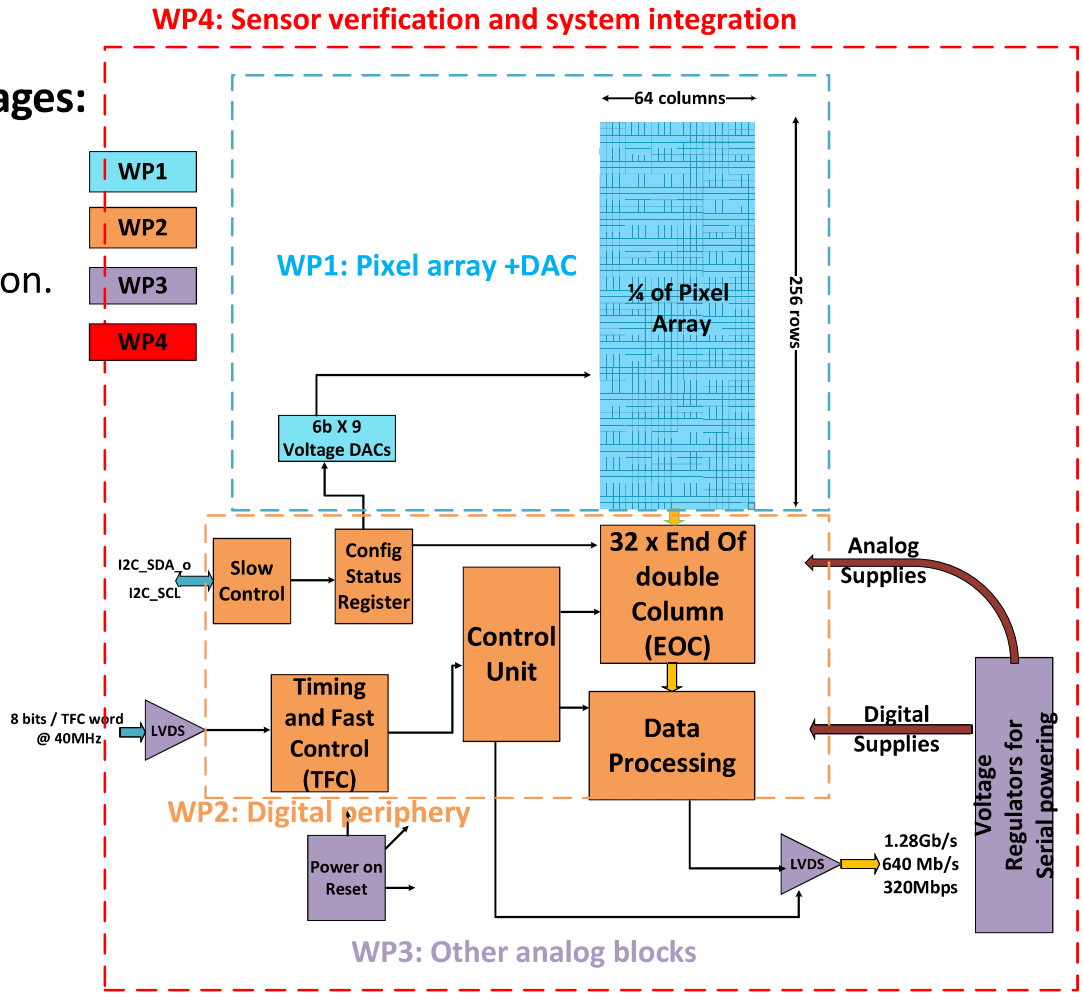
WP2) Readout Periphery

- RTL description of the digital readout periphery + P&R

WP3) Other needed analogue blocks

- Design of Shunt LDOs for serial powering
- LVDS transmitter and receiver
- Power On Reset

WP4) Sensor verification and top-level integration



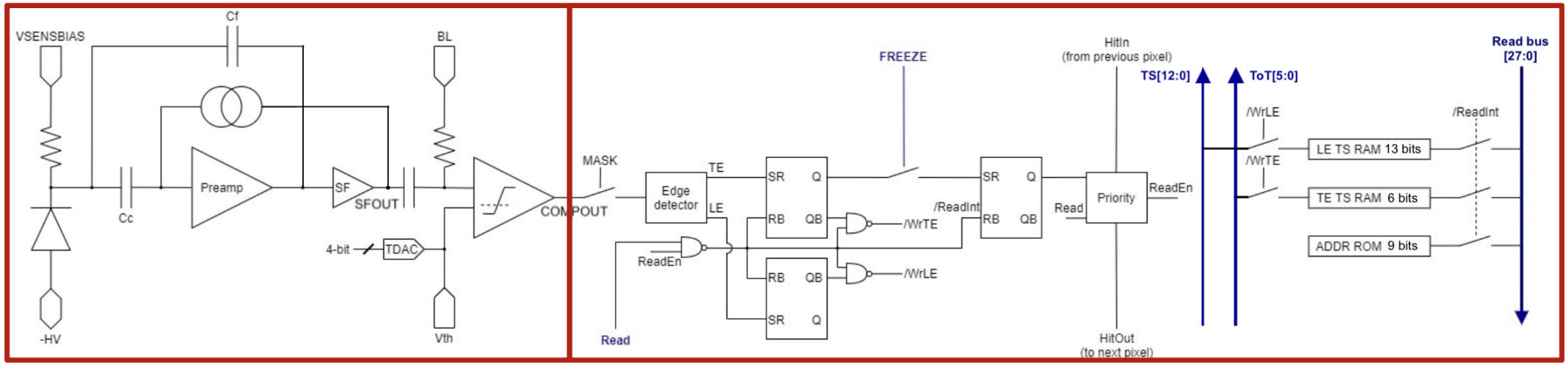
Pixel Array Design

WP1 - Pixel matrix

- Pixel size 80 µm × 80 µm, Matrix size 256 rows × 64 columns (¼ of full size)
- Each pixel includes
  - **Analogue readout**:
    - Charge Sensitive Amplifier (CSA)
    - Discriminator with a 4-bit trim-DAC for threshold tuning
  - **Digital readout**:
    - Column-drain readout
    - ToA @ 40 MHz, ToT @ 20 MHz

	ToA	ToT	Address	Total
# bits	12+1	5	9+5	32

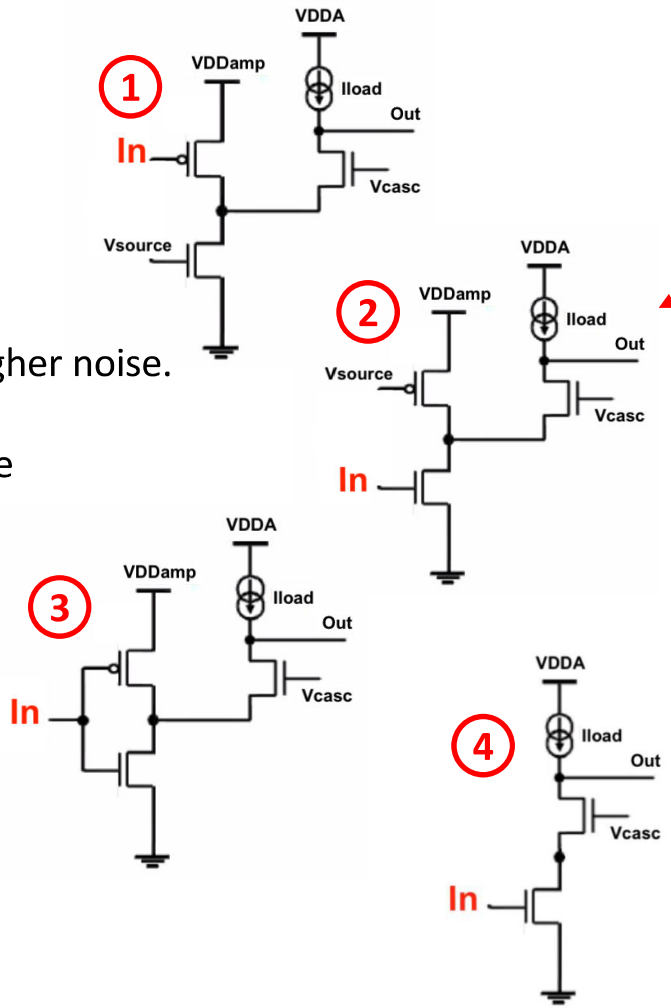
Analogue readout **Digital readout**

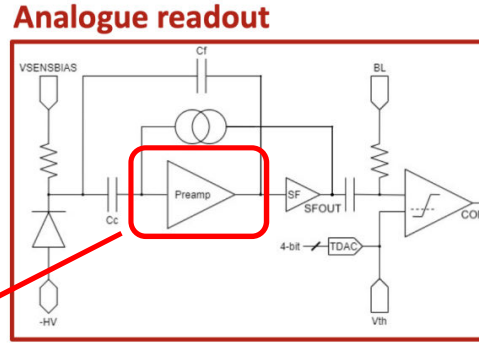


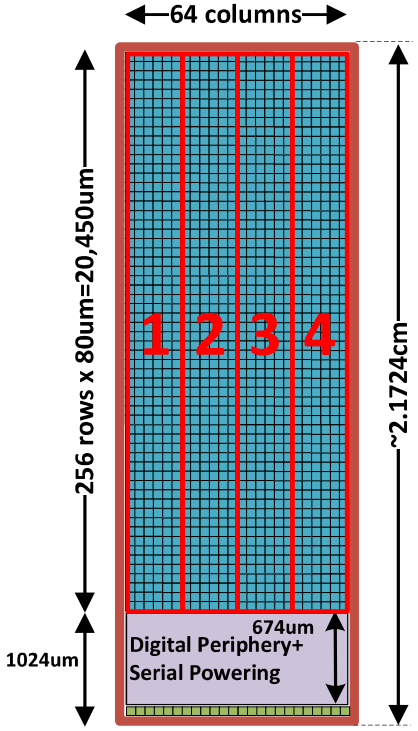
WP1 - Pixel matrix

- Four Pixel flavours with different analogue front-end:
  1. **PMOS-in CSA**
     - based on RD50-MPW4 pixel
  2. **NMOS-in CSA**
     - based on Monopix pixel, higher gain and higher noise.
  3. **CMOS-in CSA**
     - self-biased, from Monopix, faster rising edge
  4. **Trans-impedance amplifier**
     - no need of feedback cap Cf, faster speed

- All pixel flavours are optimised to meet
  - 150 mW/cm^2 power consumption;
  - 99% in-time efficiency.



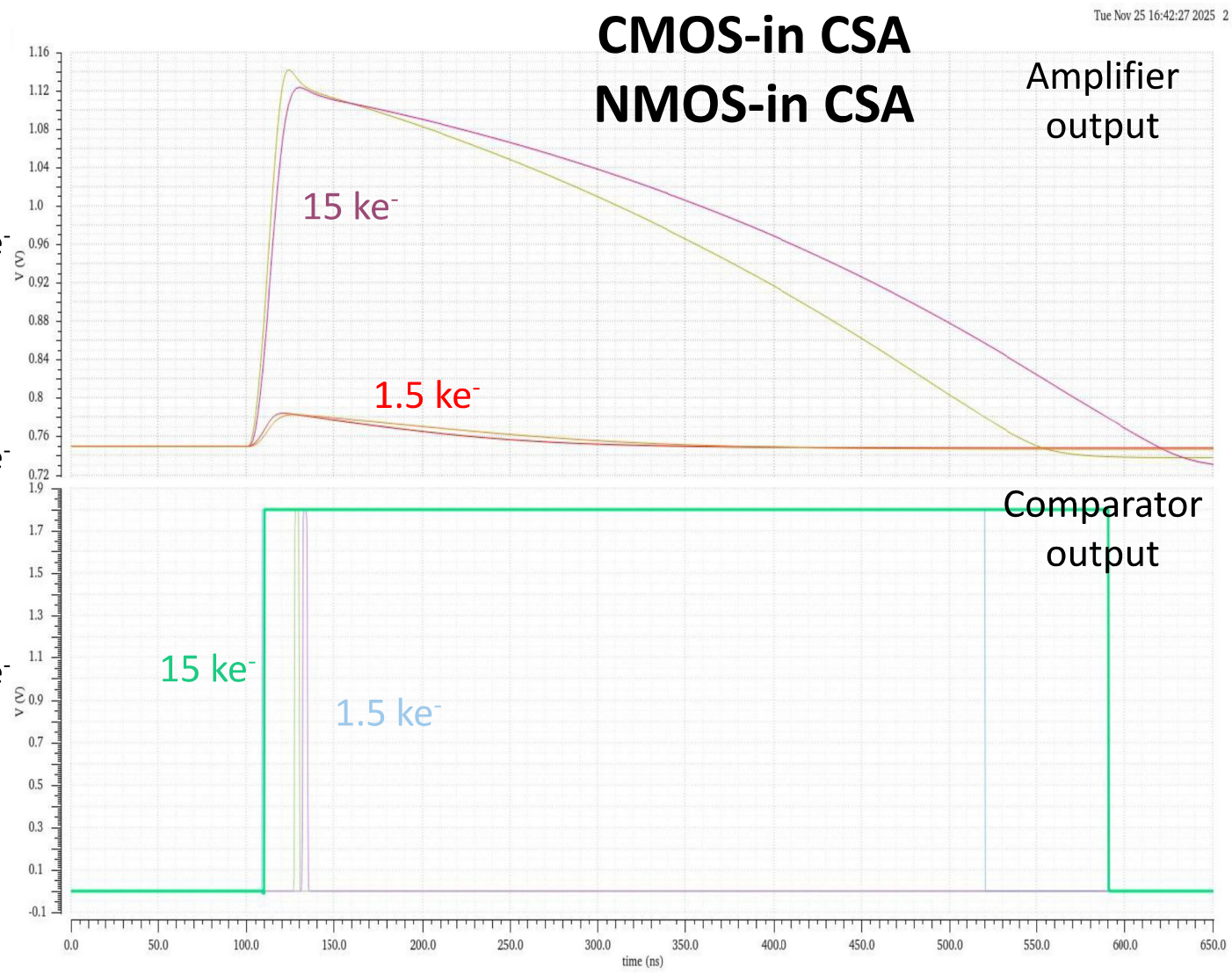




WP1 - Pixel matrix

2. Pixel with **NMOS-in CSA**:
   - Rise time: 13 ns
   - Time walk between 1.5 ke$^-$ and 15 ke$^-$ input signals: 21.8 ns (Vth -> 1.5 ke$^-$)
3. Pixel with **CMOS-in CSA**:
   - Rise time: 11 ns
   - Time walk between 1.5 ke$^-$ and 15 ke$^-$ input signals 18.5 ns (Vth -> 1.5 ke$^-$)
4. Pixel with **Trans-impedance amplifier**:
   - Rise time: 12 ns
   - Time walk between 1.5 ke$^-$ and 15 ke$^-$ input signals: 8 ns (Vth -> 5 x ENC)

- **Status:**
  - pixel schematic & simulations **Done**
  - pixel layout & extraction **Finishing**



Digital Readout design

WP2 - Digital periphery

- **Status:**

I. Verilog design **Done**

II. Block Verification: **Done**/**On-going**

1) Digital periphery configuration with slow control

2) TFC operations

3) Hit injection in pixel array

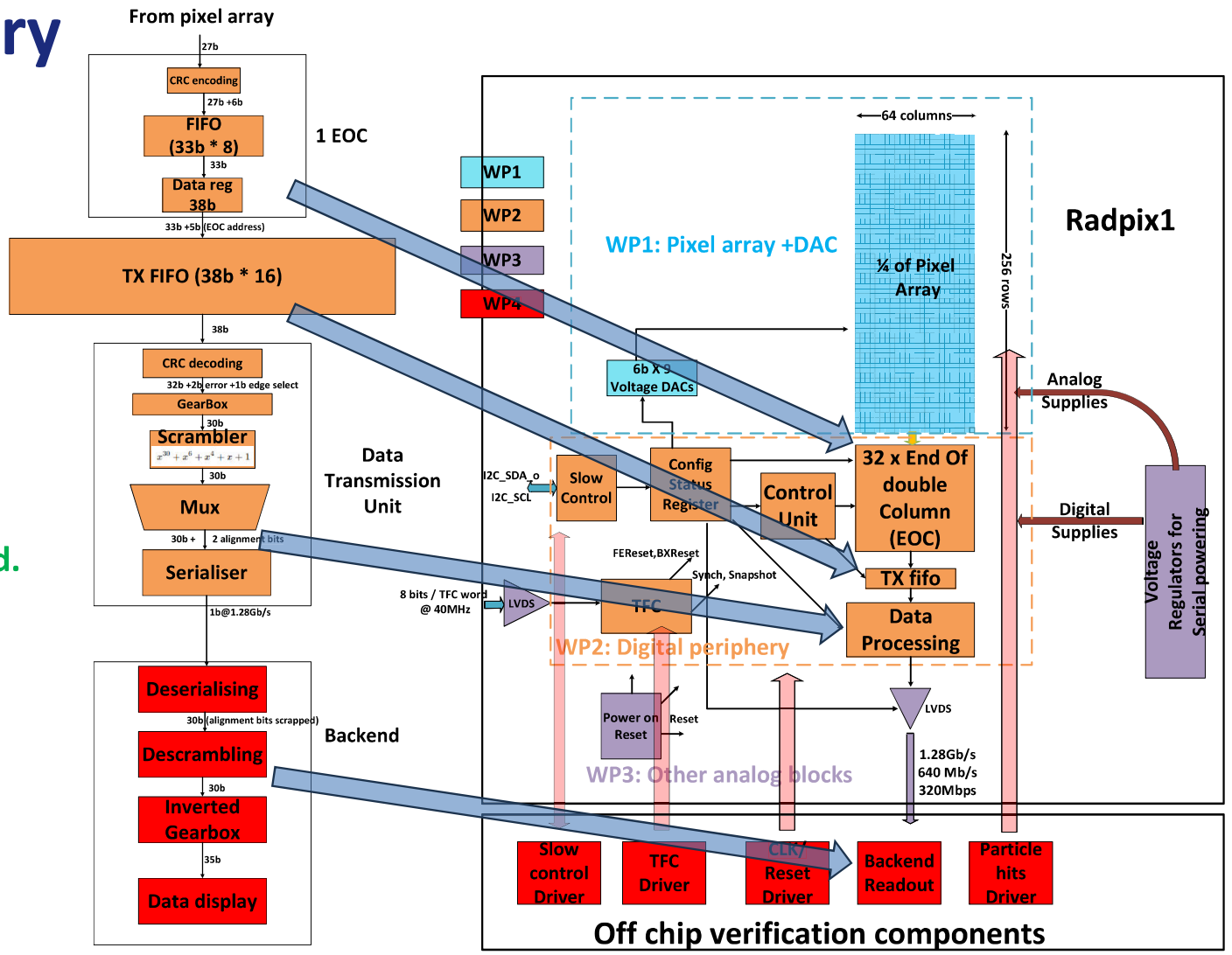
4) Data path from pixel array to backend.

5) Automated verification

III. Integration: **Next steps**

6) Synthesis and Place & Route

7) Top level virtuoso integration



Progress in other analogue blocks

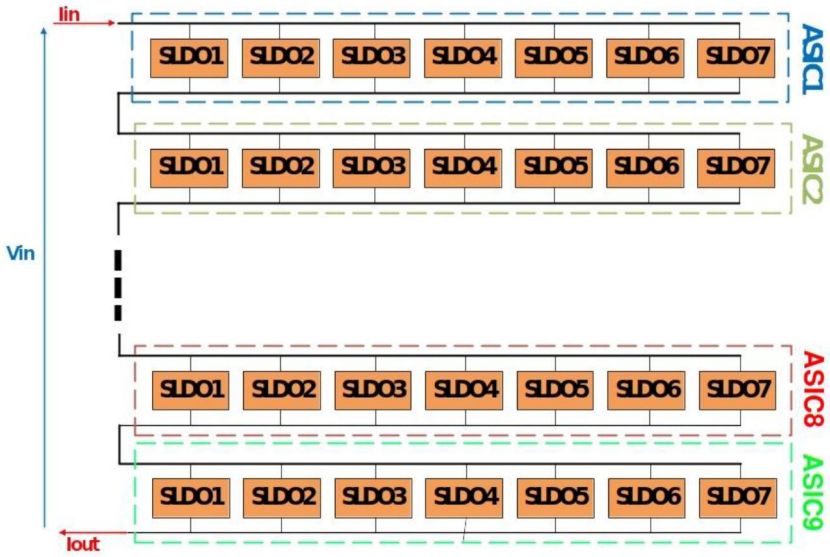
WP3 - Serial powering

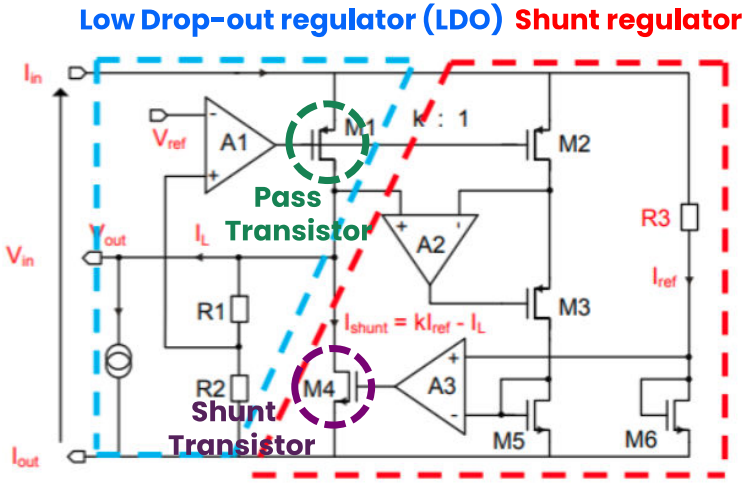
- 9 ASICs per serial grouping

- 7 x SLDOs per ASIC:

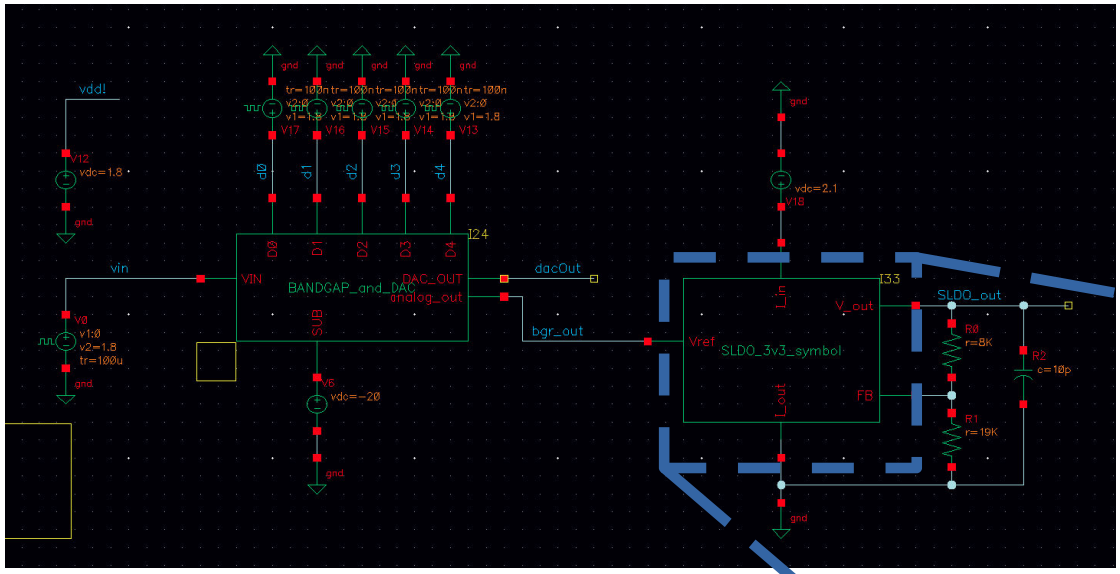
SLDO1: VDDD	=>1.8V
SLDO2: VDDC	=>1.8V
SLDO3: VDDP	=>1.8V
SLDO4: VDDA	=>1.8V
SLOD5:VNSENSBIAS	=>1.8V
SLDO6: VSSA	=>1.3V
SLDO7: VDD_1v0	=>1V

- Based on proven voltage regulators designs in chips beyond LHCb (RD53, EIC...)
- Reference voltage V_{ref} provided by a bandgap with DAC to adjust V_{out}
- I_{in} determined by R3 and M6



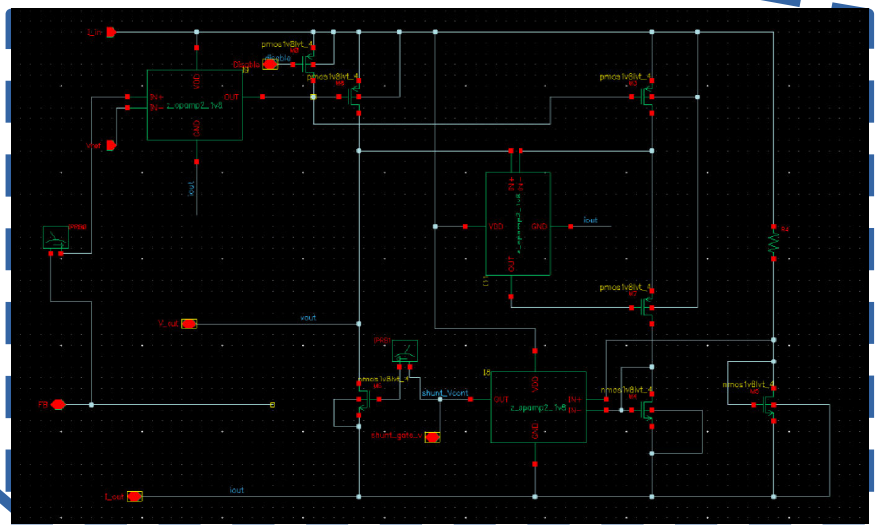


WP3 - Serial powering



- Each SLDO provides output currents up to 200mA
- Each SLDO includes overvoltage protection and overcurrent protection circuits
- SLDOs simulated for various failure conditions including over-voltage, over-current and voltage domain short-circuit conditions

SLDO



- Status:
  - Schematic & simulations **Done**
  - layout & extraction **On-going**

DAQ development and evaluation plan

- Use **MARS** as the DAQ system to maximise compatibility between institutes

- **Lab measurements**
  - I-V curves, with controlled temperature
  - Standalone chip block performance against chip specifications
    - Pixel matrix with test pulses and with radioactive sources (analogue output, S-curves, in-pixel trimming DAC optimisation)
    - Chip periphery functionality (TFC, LVDS at required speed)
    - Voltage regulators (as a function of temperature, VDD and process variations)
  - Full chip (pixel matrix + digital periphery powered with voltage regulators)
    - Time resolution (with scintillator setup)
    - Power consumption
    - Hit rate
  - Serial powering with > 1 RadPix chip

Chip thickness [µm]	100, 200
NIEL [n_{eq}/cm^2] at Ljubljana	Several steps until 4E15
TID [Mrad] at Oxford or RAL	Several steps until 250 MRad

- **Irradiation studies and test beam evaluation**
  - NIEL, TID, SEEs and test beams (efficiency, time resolution as a function of HV, comparator threshold…)

- **Multi-chip operation (*e.g.* RadPix on on-module hybrids/flexes)**

Mighty Pixel DAQ

- Electronics and Backed Architecture document
- Developing an overall **DAQ plan**
  - List of tasks detailed; task allocation in progress (i.e., who does what)
- Refining **data formats** with chip designers for prototype and final chips
  - Studies needed to identify FPGA resource needs
  - Brainstorming workshop
- Defined systems for prototyping and system integration
  - Smaller items (wafer, chip, module) - MARS (see next slide)
  - Larger items (full stave and greater) - MiniDAQ (support from Online)
  - **Reproducibility is key to successful production - all sites will have same hardware/software/firmware.**
- Readout testing
  - A. Modak testing full readout chain (lpGBT to/from Backend)
  - To be integrated with FE developments for full end-to-end characterisation
  - More in Atanu's slides from UK production meeting


LHCb Technical Note
EDMS 3321981 v.2
November 18, 2025

MightyPixel Tracker Back-end Architecture

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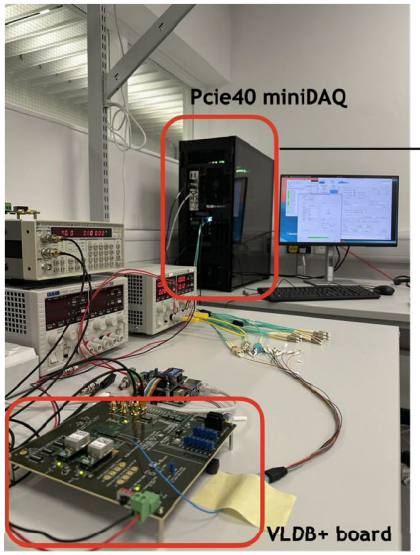
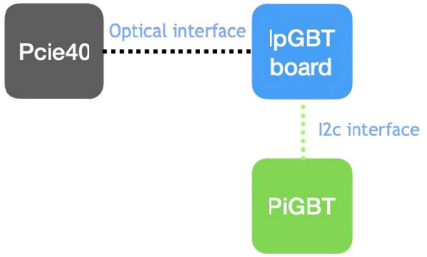
Abstract

This documentation is aimed at serving providing requirements to the Front-end ASIC MightyPix and the supporting electronics, and the architecture in which it will exist. It describes the dataflow, constraints on the expected data format, the configuration data, the timing and fast control signals and the expected rates for each.



- Low cost, workstation based miniDAQ solution
- Interfaced miniDAQ with lpGBT board



MARS Workshop (24-25 Nov)

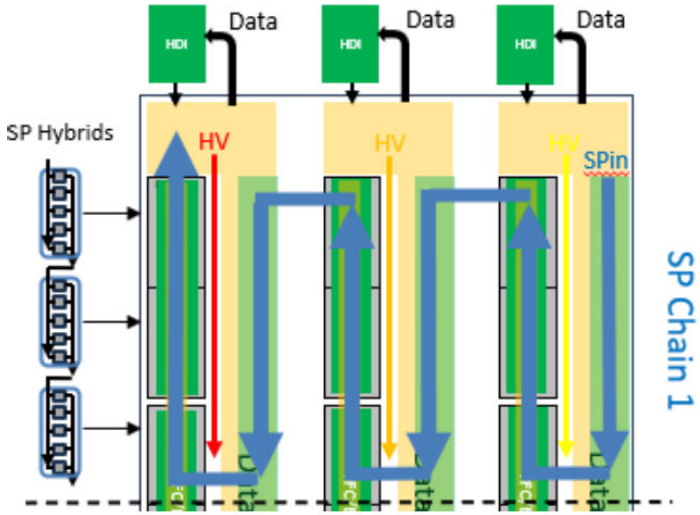
Goals:

- Demonstrate the system
  - Get hands-on experience with experts
  - Great demos, exercises
  - Documentation in good state
- Train new developers
  - Firmware, software, documentation
- Establish a roll-out plan and timeline
- Discuss future evolution
  - Result: roll out plan of systems for institutes Mar 2026

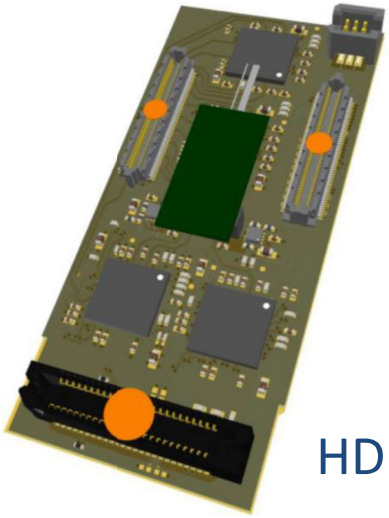
Off-chip Electronics

- Serial Powering (A. Greenall, Y. Gao)
  - Challenging
  - Design advancing but large scale prototypes needed early (supported by reviewers)
- High Voltage (A. Greenall)
  - Design linked to Serial Powering scheme
- HDI (M. Perry)
  - Very dense electronics
  - Well advanced
  - First prototype expected soon

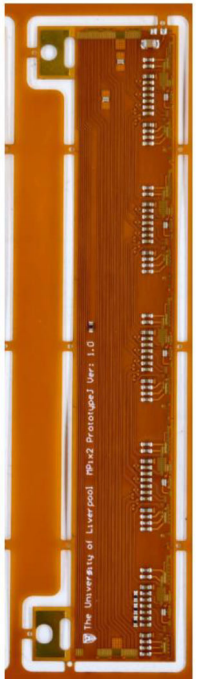
Starting to see real prototypes being produced!



Quadrant SP Chain



HDI



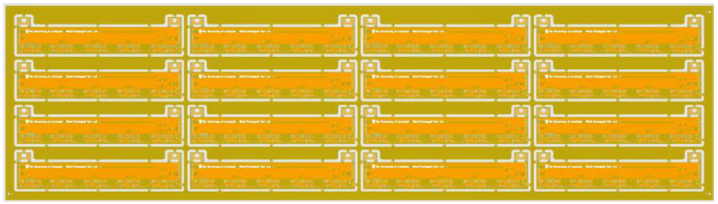
Hybrid Flex

Hybrid Flex for Full Size Mock-up - Status

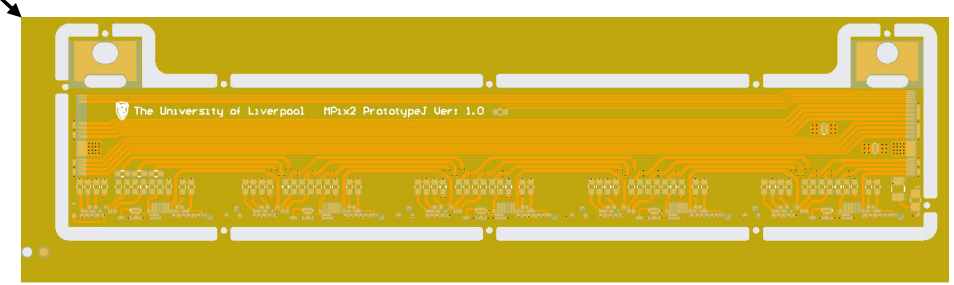
- Circuits readied for manufacture and part (SMD) assembly
  - Targeting 160 circuits – aligned to MPix2
- Panelised to facilitate their assembly – 16 circuits per panel in a 4 x 4 matrix
  - 10 panels total

- Stack-up utilises 25µm Polyimide dielectrics, Build thickness: approx. 300µm
  - 3 Cu-layers, Designed for Z_{DIFF} of 100Ω excluding loading

- Circuits already received at Liverpool

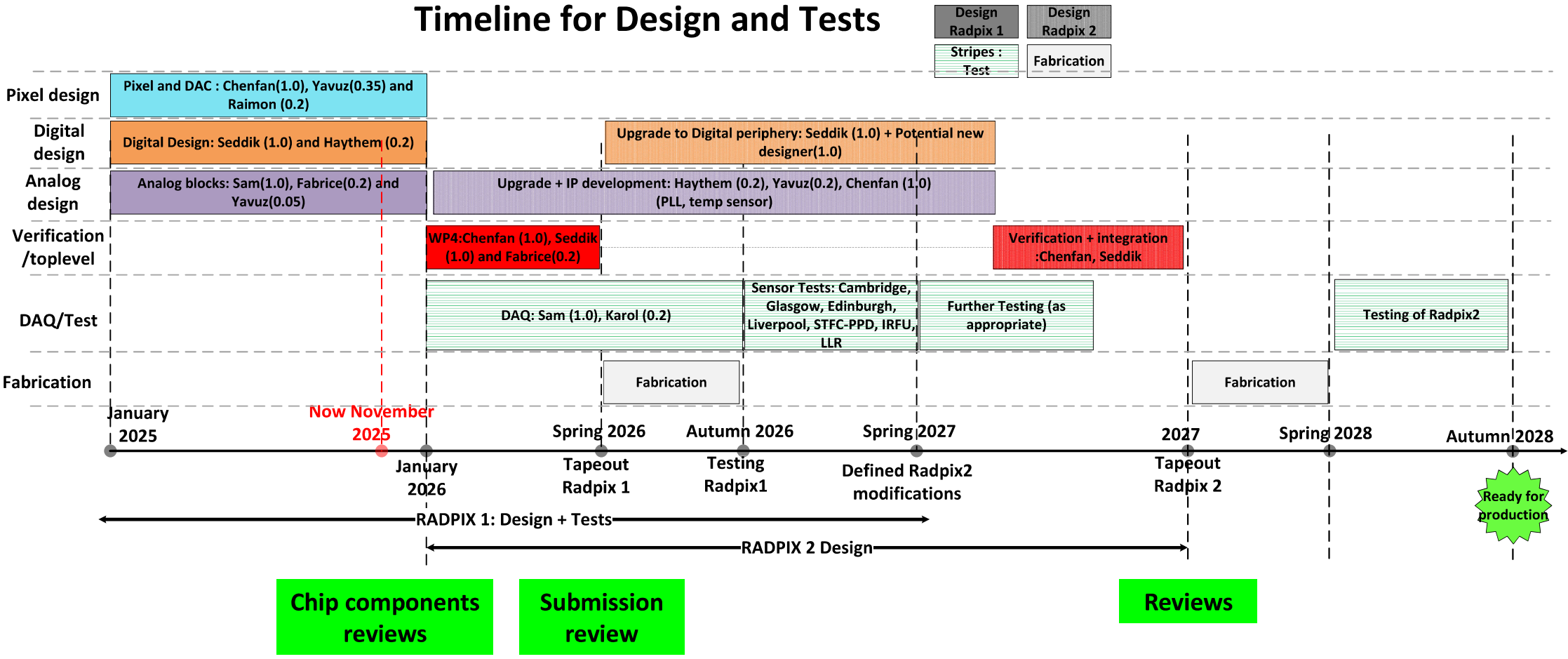


Panel of 16 circuits



Single circuit detail

Development Plan



Overview

- Development of ¼-size RadPix1 using LFoundry 150 nm is progressing well, target to submit in spring 2026.
- Optimisation of Pixel Matrix for power (150 mW/cm2) and speed (99% in-time efficiency) requirements with 4 different pixel flavours. **Meeting target.**
- Design of readout periphery for compatibility with LHCb protocols, and power budget. **Verilog blocks done, verification phase ongoing**
- Analogue blocks (LVDS transmitter & receiver, power-on-reset, voltage regulator for serial powering) **Ported to Lfoundry, some Completed others ongoing.**
- **LVDS Status: schematic, Corners simulations , layout & extraction On-going**
- **Power on reset done**
- Design verification. **Established communication and configuration, slow control + high speed data out done. TFC verification ongoing.**