Characterisation and System-Level Simulation of Fully Digital Pixel Architectures

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Introduction

Motivation: Bottlenecks in conventional pixel detectors

The Particam concept: A Fully Digital Sensor architecture

The PixESL framework: A System-level framework

Conclusions & Future work

Backup

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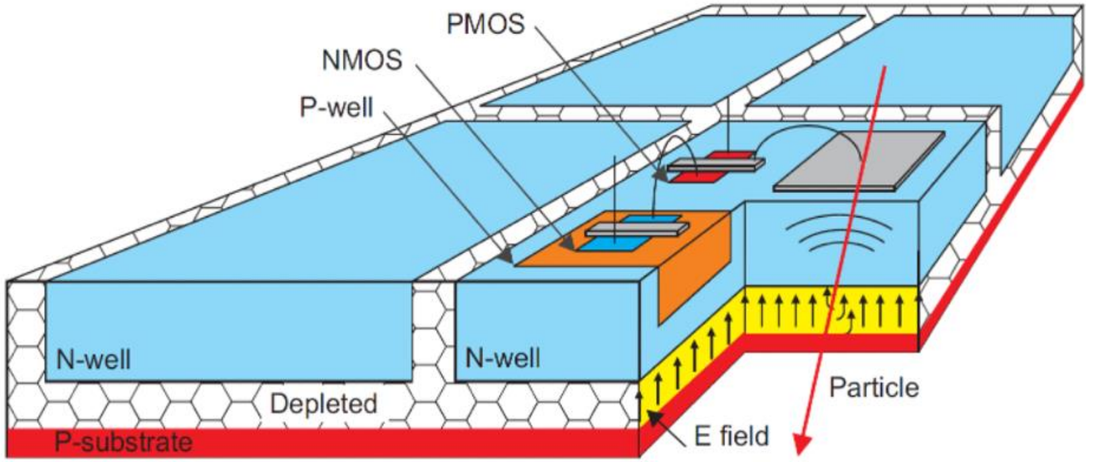
Motivation & Challenges

Analogue Scaling Limit:
Unlike digital logic, analogue transistors (CSAs, shapers) require specific voltage headroom and area to maintain Signal-to-Noise Ratio (SNR).

The Density Gap:
A conventional $2 \times 2\,cm$ sensor (with a 75 μm pitch) has $\sim 65k$ pixels;
Shrinking the pitch to $2.5\mu m$ (Particam goal) increases this to ~ 64 million pixel- a $1000 \times$ jump.



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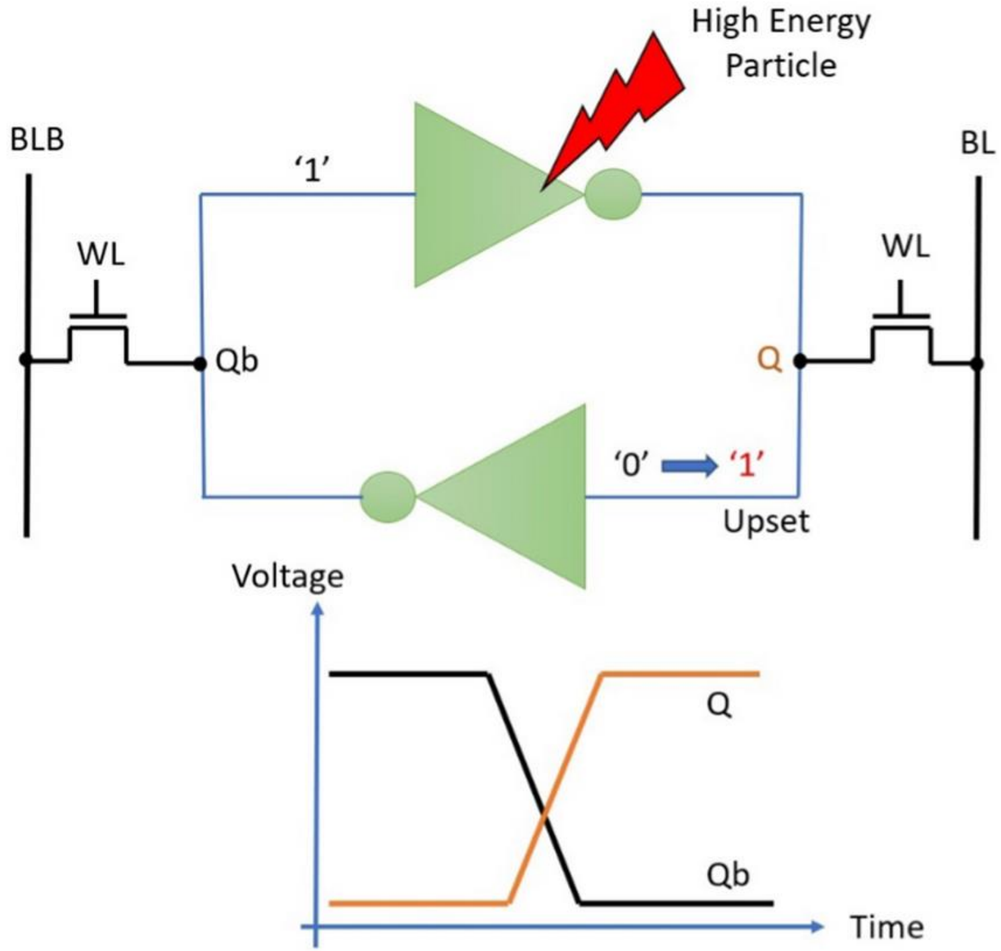
The Particam Concept-Fully Digital Sensor

Detection Mechanism:
Reproposing **Single Event Upset(SEU)** as the detection mechanism.

Detection Trigger:
A hit is registered when the deposited charge exceeds the Threshold Charge (Q_T)

Advantages:
1. **Area Efficiency**: Eliminate analogue amplifiers, leveraging high-density $65nm$ CMOS processes.
2. **Extreme Density**: Enables a pixel pitch of $2.5\mu m$, $1000 \times$ higher density than before.



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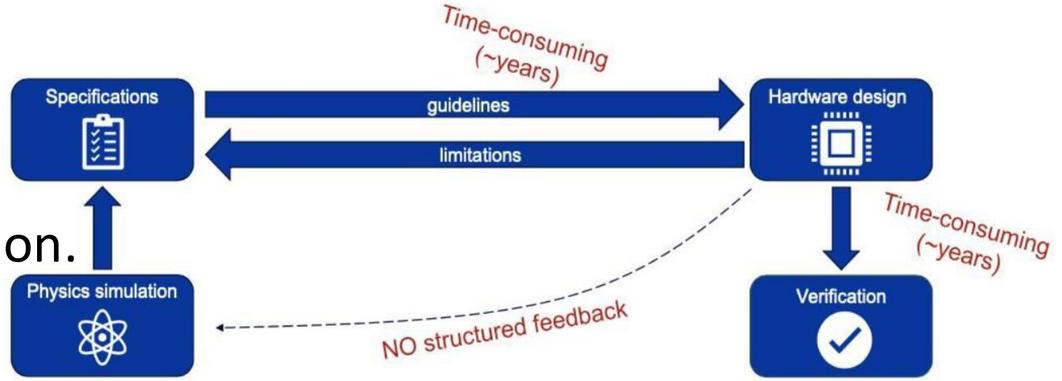
Verification Challenges & ESL Design

Limitation of RTL(Register Transfer Level):

1. **Cycle-Accurate &Slow**: Calculate every signal transition.
2. **Prohibitive Latency**: Days of CPU time for ms-scale data.
3. **Late Feedback**: Bottlenecks discovered after implementation.



The ESL(Electronic System Level) Solution: PixESL

1.**Virtual Prototyping**: C++/SystemC-based architecture modelling.

2. **Transaction-Level(TLM):** focus on data flow, not wire toggling.

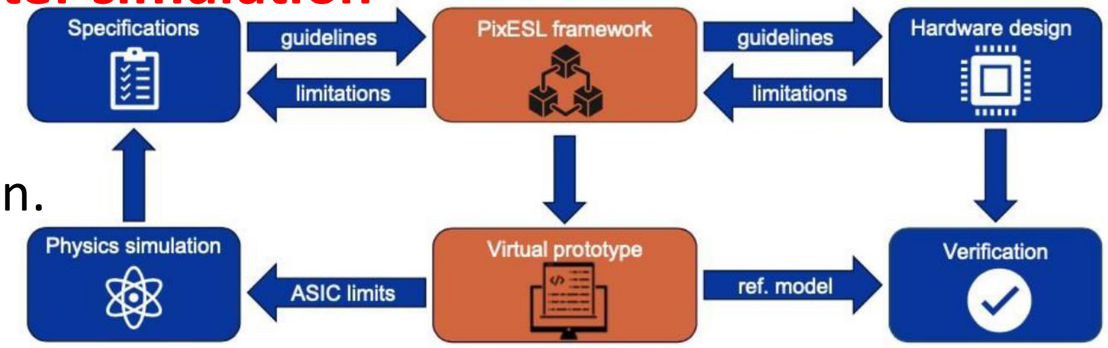
Conventional RTL

$50 \times$ Faster simulation

Key performance

1.**$50 \times$ speedup**: 70,000 transactions/second.

2.**Early Optimization**: Early validation before implementation.



Adapted from: Dhaliwal, TWEPP 2024

The ESL

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Technical Implementation: SystemC & TLM

SystemC: The framework

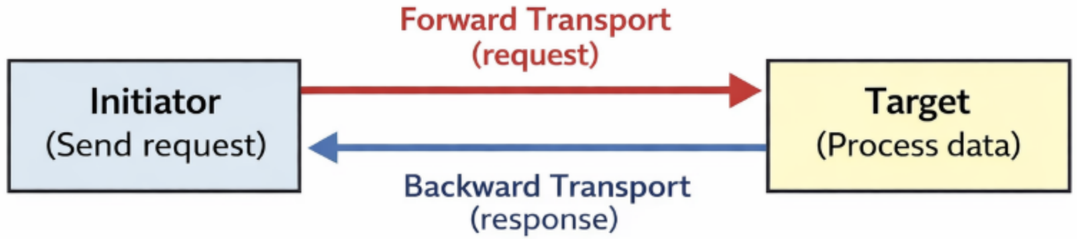
1. **Beyond C++**: Adds hardware concurrency, hierarchy and time.
2. **Unified Simulation**: Integrates physics(C++) with hardware readout logic.

Transaction-Level Modelling (TLM)

1. **Abstract communication:** Model data flow as “transactions” instead of signal toggling.
2. **Pass-by-reference:** Pointers transfer data packets directly.

The Generic Readout Node

1. **Initiator & Target**: Modular communication blocks.
2. **Flow Control**: Bidirectional path for data integrity.



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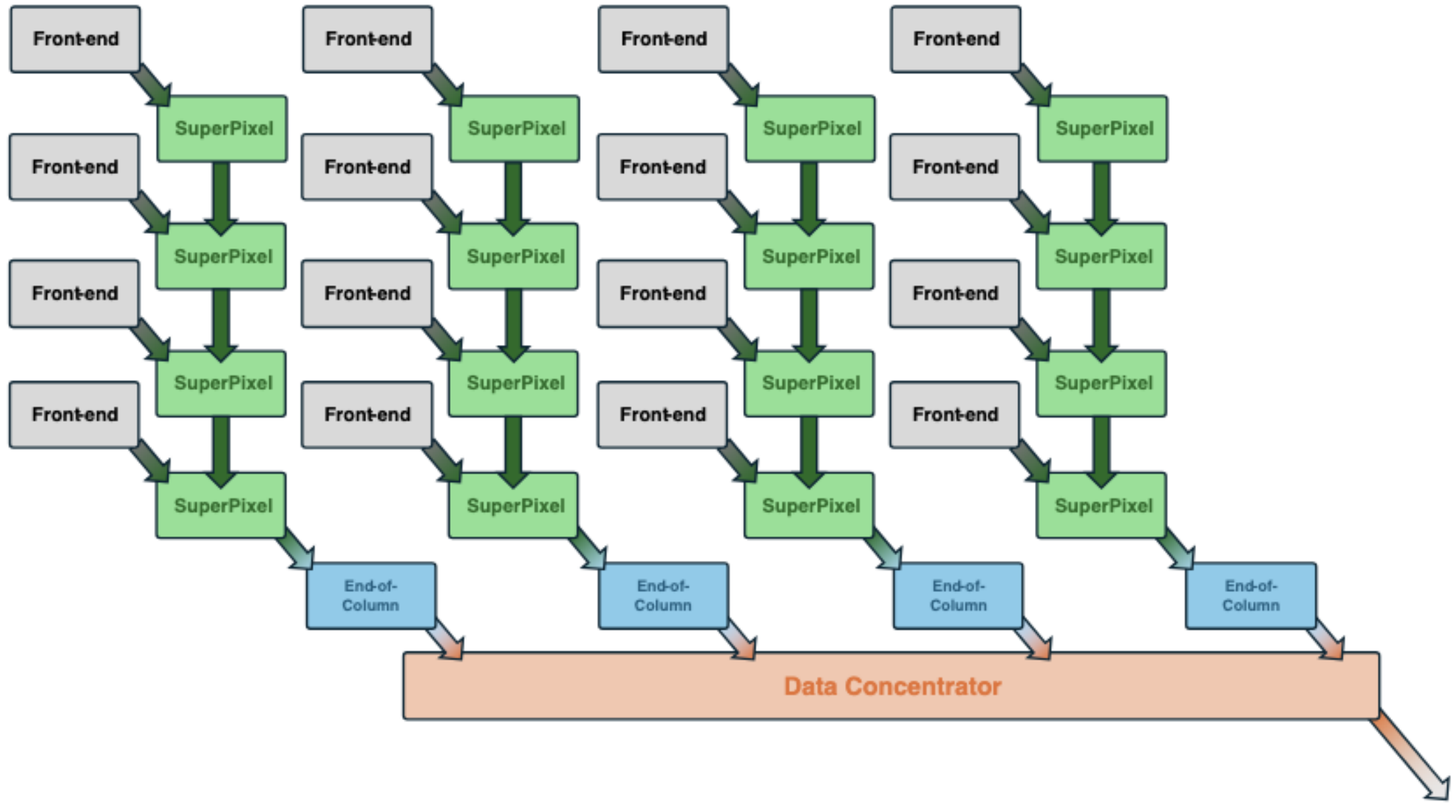
The PixESL Framework Architecture

Readout Modelling:
Spans seamlessly from the individual pixel frontend to global Data Concentration.

Configurable Hierarchy:
Highly modular design supporting flexible connectivity (e.g., group pixels into SuperPixel).

Scalability:
Allows rapid testing of different routing and aggregation strategies for large-scale matrices.



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Particam Readout Architecture Design

Rolling-Shutter Scheme

1.Mechanism: Rows are activated sequentially to extract hit information.

2.Advantage: Minimises in pixel logic, enabling the $2.5\mu m$ pitch.

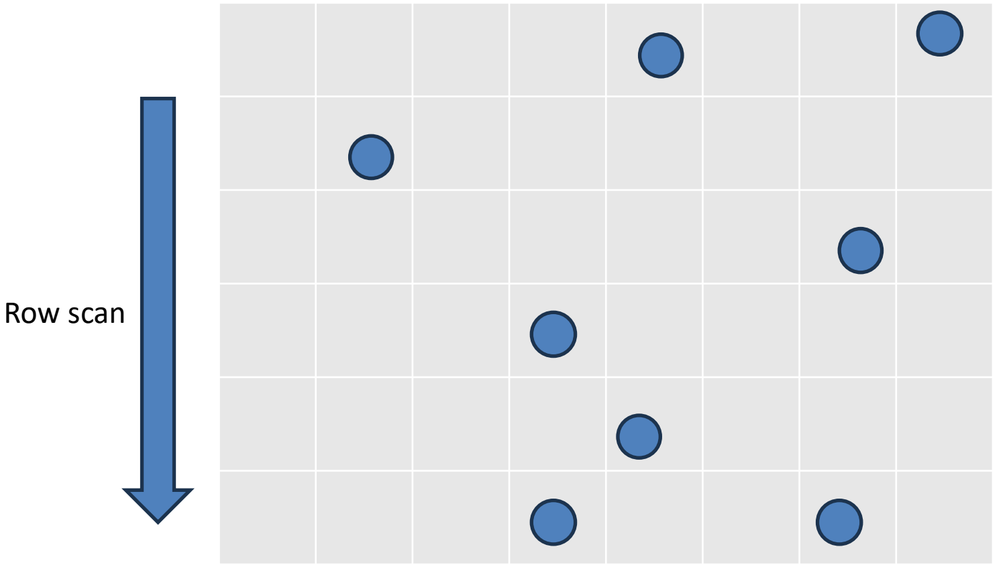
Two-Phase Operation

1.Acquisition Phase:

Particles are detected and latched in 1–bit pixel memory.

2.Readout Phase:

Column-wise scanning transfers data to End-Of-Column(EoC) buffer.



Two-phase operation

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My Work

Modelling the Particam within PixESL framework.

Further Directions

Build the Particam readout network within PixESL framework.

Optimise its architectural parameters.

Going FBK for 2 years.

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Thank you!

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Pixel Unit Modelling

AFE wrapper

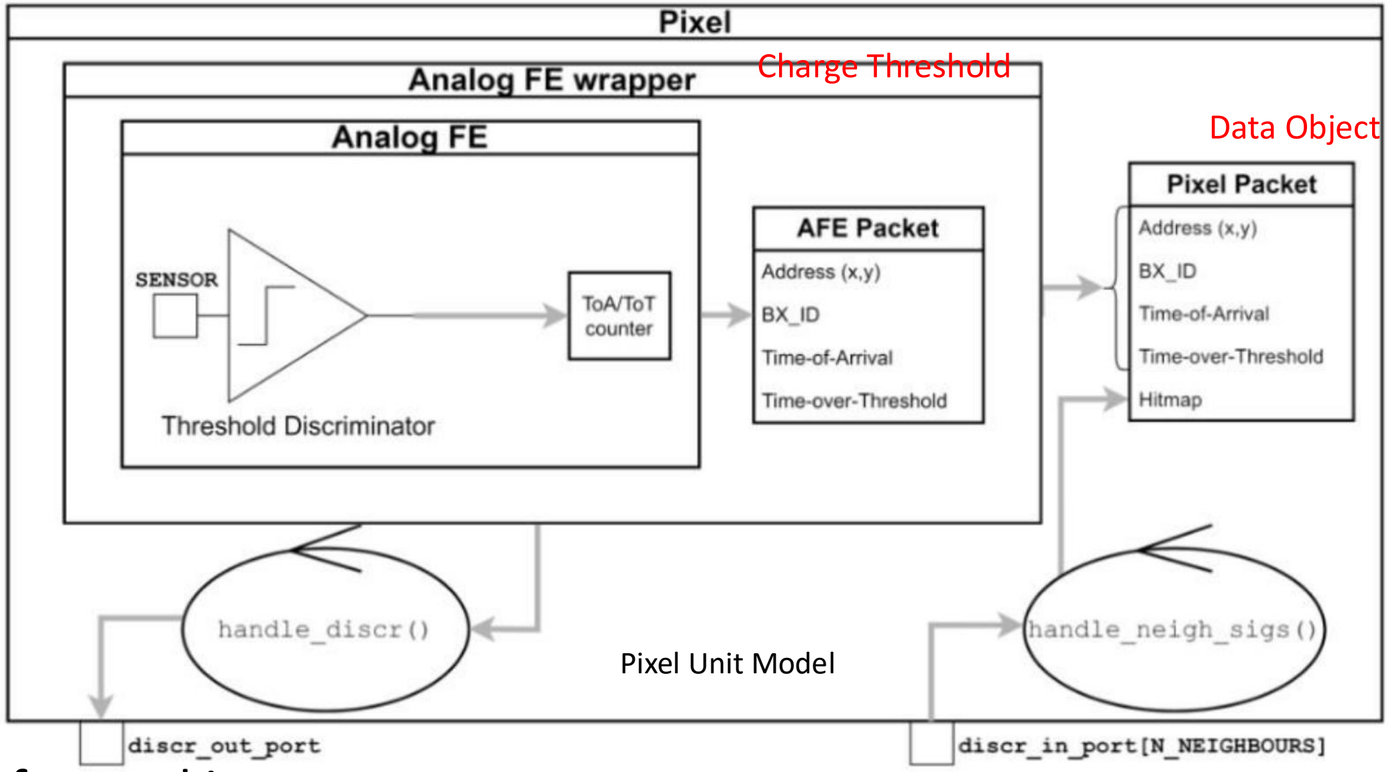
1. Models the physical charge collection of the N-well diode.
2. Triggers a hit when the deposited charge exceeds Q_T

Packet Generation:

Hit events are encapsulated into a Pixel Packet object for TLM transmission.

Packet Content:

Address (x,y): Spatial coordinates.
BX_ID(Bunch Crossing ID): Global timestamp for tracking
ToA & ToT: Time-of-Arrival & Time-over-Threshold
Hitmaps: Status flags for clustering.



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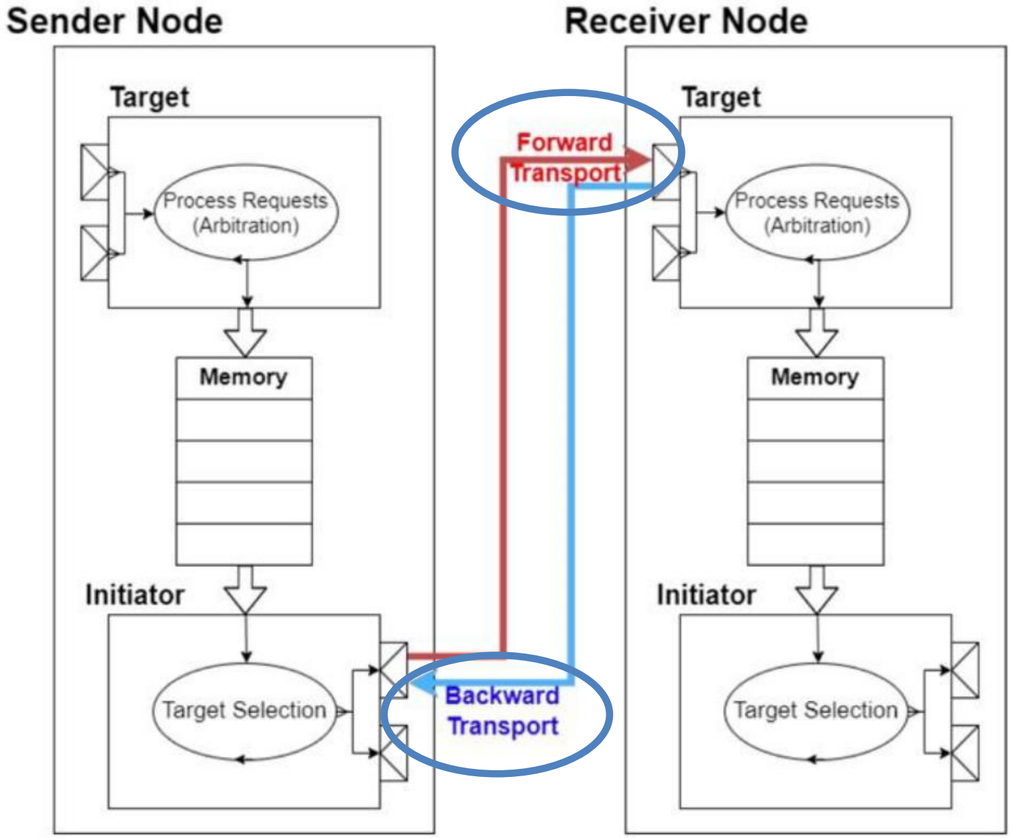
Generic Readout Node

The fundamental building block of the network is a generic node composed of an Initiator (sender) and a Target (receiver).

Arbitration:
The "Process Requests" block handles incoming data packets

Buffering:
This buffer temporarily stores pixel hits during high-occupancy bursts, preventing data loss when the output link is busy.



The generic TLM Readout Node

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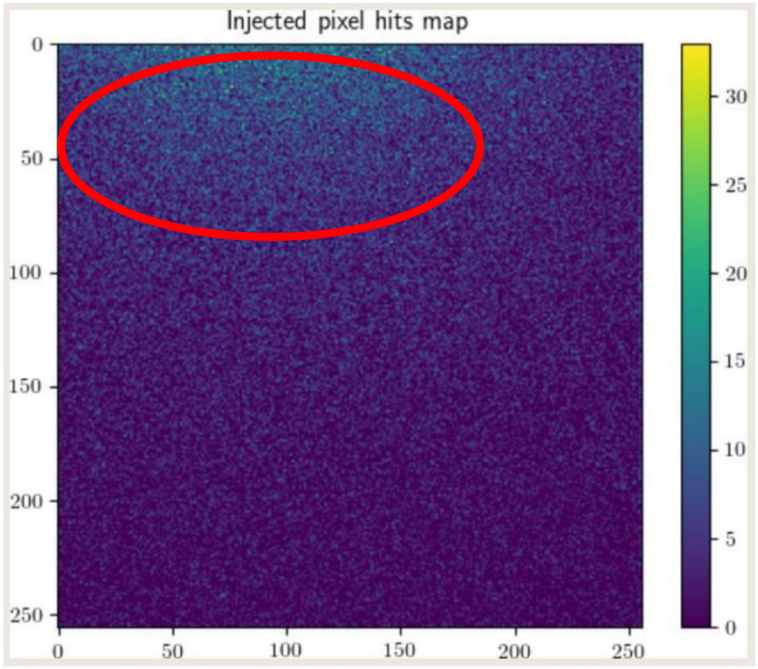
Previous Case Study: VeloPix & Validation

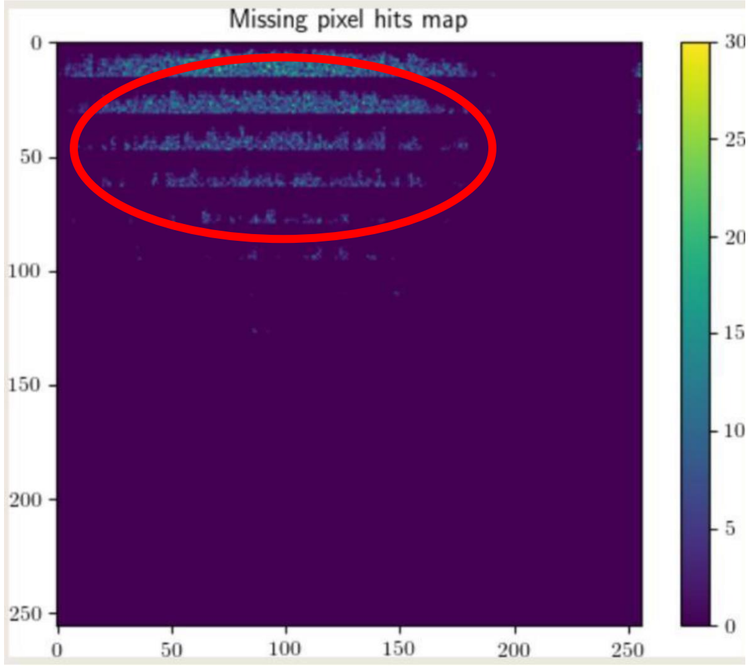
Objective:
Validate the PixESL framework by evaluating the VeloPix architecture under HL-LHC conditions

The input (Left)
Simulated highly non-uniform particle hits

The Diagnosis:
1.PixESL successfully identified hidden architecture bottlenecks.
2. FIFO saturation: High hit rates caused buffer overflow.
3. Missing hit: Clearly visualized exactly where and why data drops occur.



Injected Pixel hits map



Missing pixel hits map

Conclusion
PixESL proves effective in pinpointing data-flow vulnerabilities before physical implementation.

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