Design, Simulation, and Characterisation of Fast Timing Silicon Sensors for HEP applications

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2026 HEP meeting

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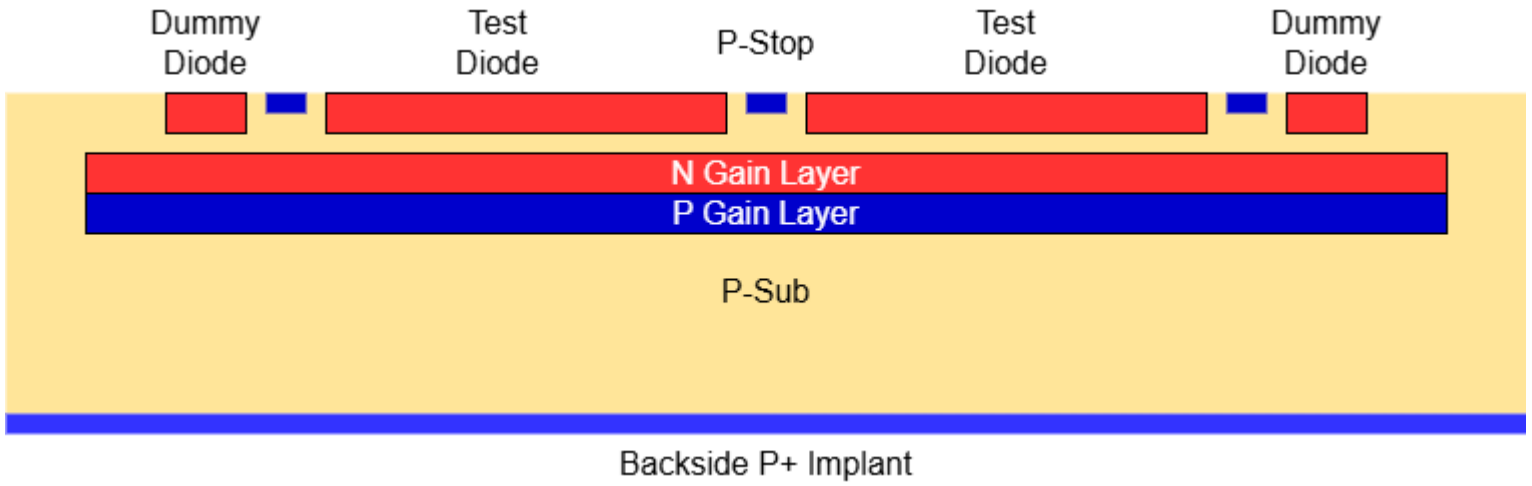
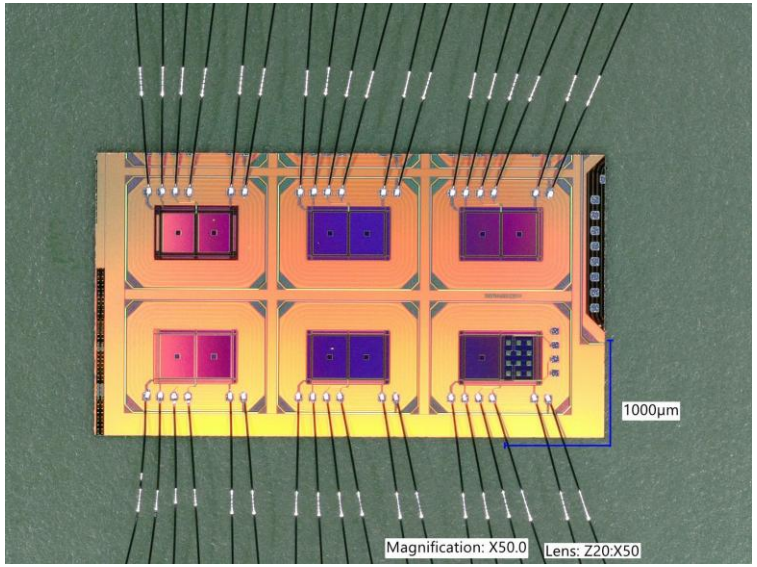
Introduction

- Cactus-GL, aims to achieve sub 50 ps time resolution with embedded readout electronics.
- Initially a proof of concept, to observe if gain can be obtained



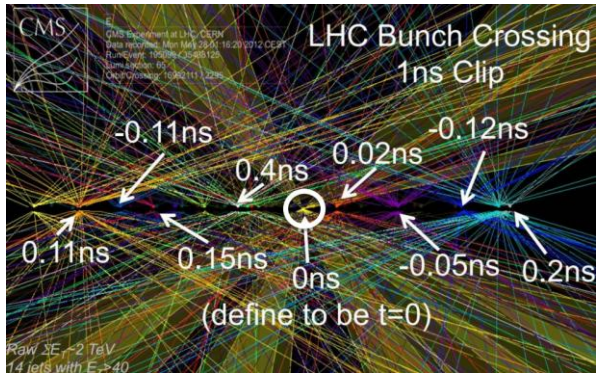


*Testbeam results of the MiniCactus V2 timing demonstrator

Requirements of Fast Timing

Anticipated ~200 pile-up events per bunch crossing at the HL-LHC, making vertex reconstruction complex

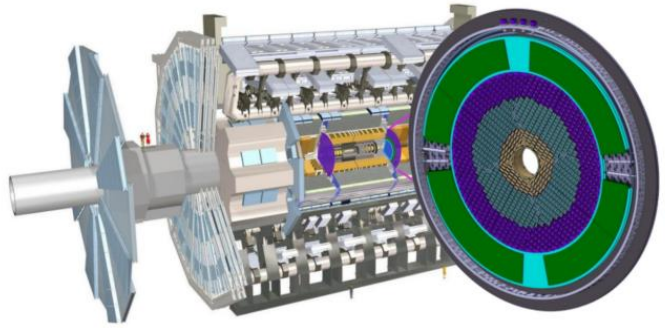
HL-LHC, and FCC-ee aim to achieve 4D particle reconstruction. Active R&D effort to developing sensors which can achieve this



[1] Simulated collision at CMS in the HL-LHC

The ATLAS High Granularity Timing Detector (HGTD) aims to provide 4D reconstruction, to do this requires less than 30 ps timing resolution

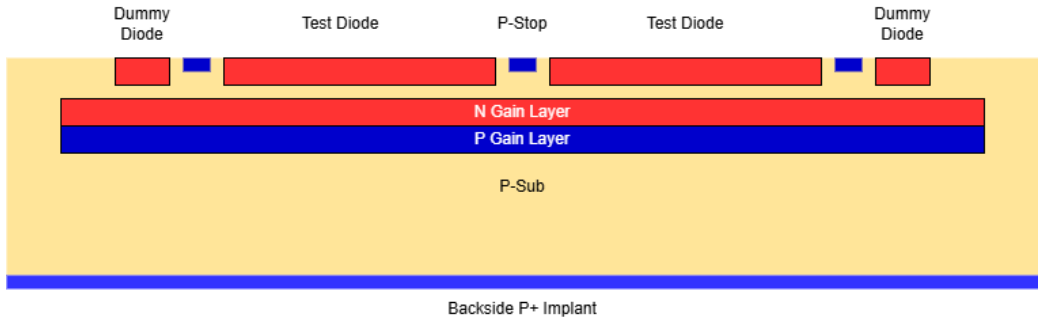
Must withstand fluences up to 2.5×10^{15} n_{eq}/cm^2 over its operational lifetime.

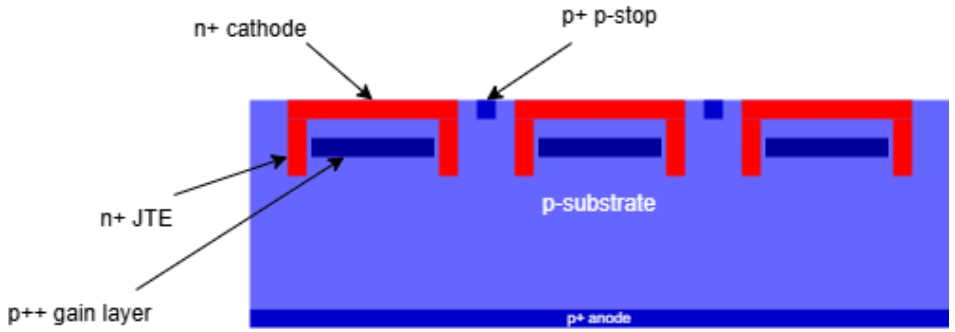


[2] Diagram of the HGTD

Motivation for Gain in CMOS Process

- Standard LGADs do provide fast timing, at a trade off being hybrid sensors
- Complex bump bonding to ASICs
- CMOS process has many commercial foundries, production can be carried out on a large scale
- CMOS enables development of monolithic sensors, with readout electronics on chip



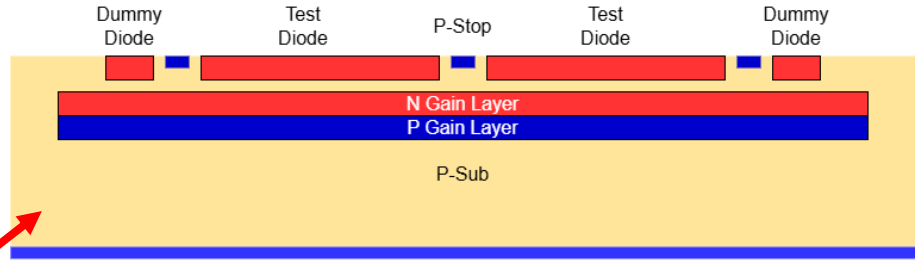


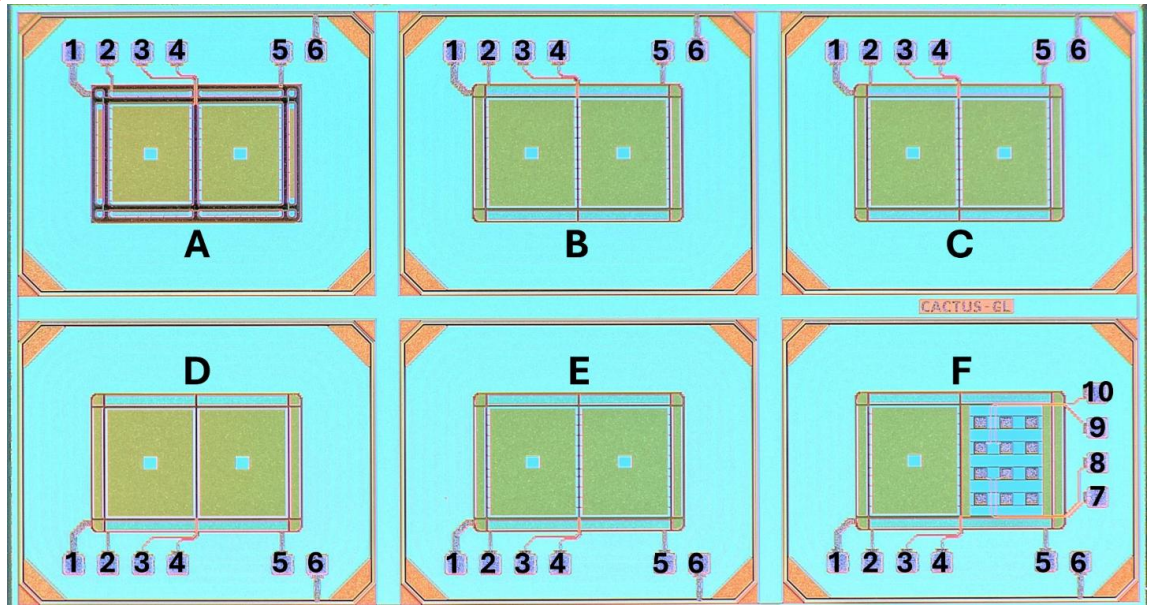
	Standard LGAD	LGADs in CMOS
Fast Timing	✓	✓
Monolithic	×	✓
Large production capability	×	✓
Low manufacturing cost	×	✓

CactusGL

- 6 different structures, each with two test diodes
- 4 wafers manufactured on two different high resistivity wafers, with high and low gain layer concentrations

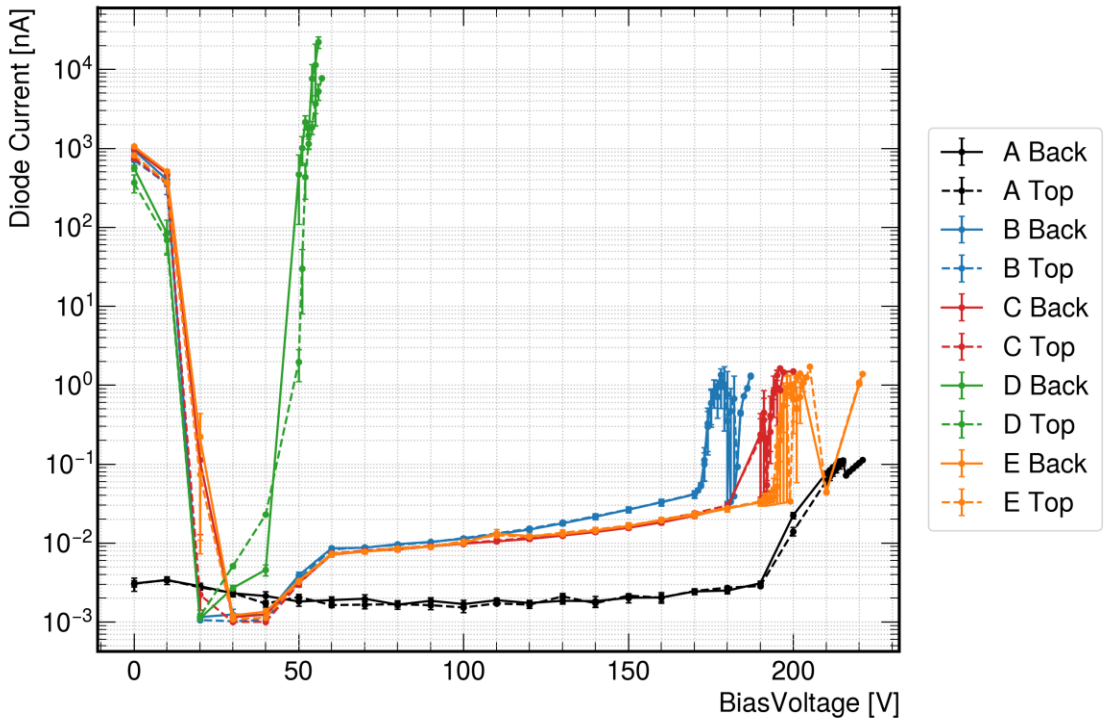
Structure	Features
A	Reference structure, no gain layer
B	Base gain structure
C	Polysilicon interpixel isolation
D	Higher concentration n-diode
E	B, with a different guard ring structure
F	AC LGAD





I-V's

HR Wafer, high P dose



- Highest breakdown observed in structure A (no gain layer)
- Similar breakdown in all other structures, except D
- No dependency on location of biasing

Structure	Features
A	Reference structure, no gain layer
B	Base gain structure
C	Polysilicon interpixel isolation
D	Higher concentration n-diode
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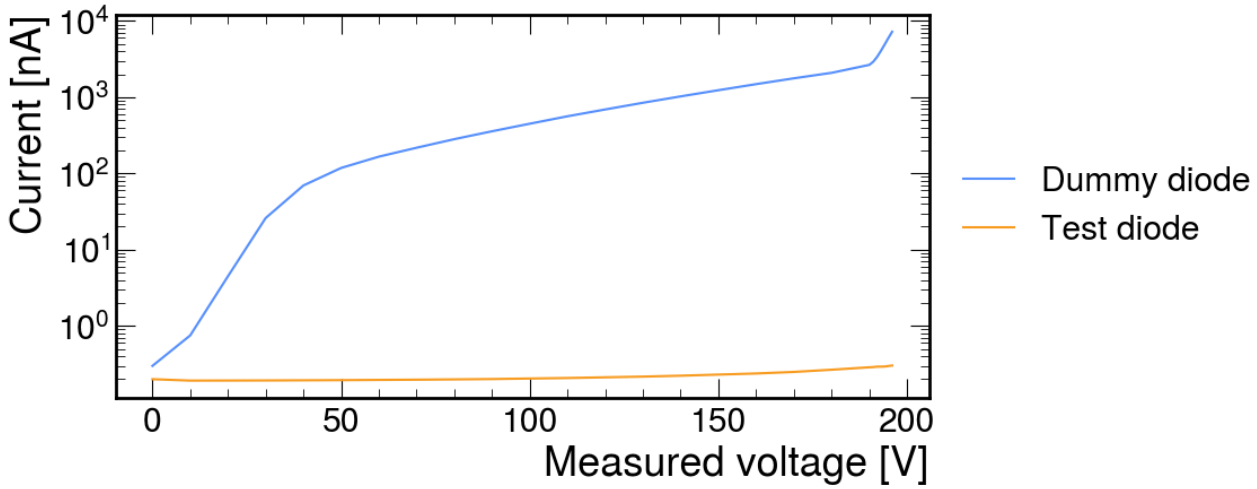
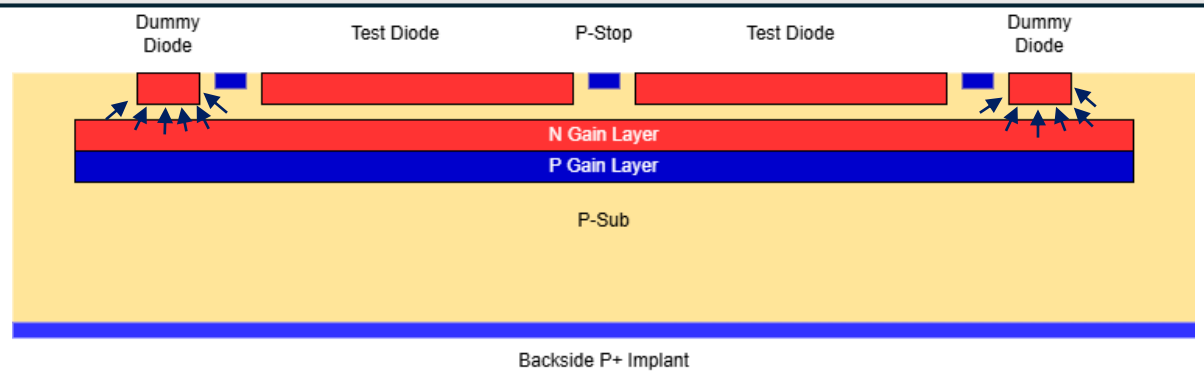
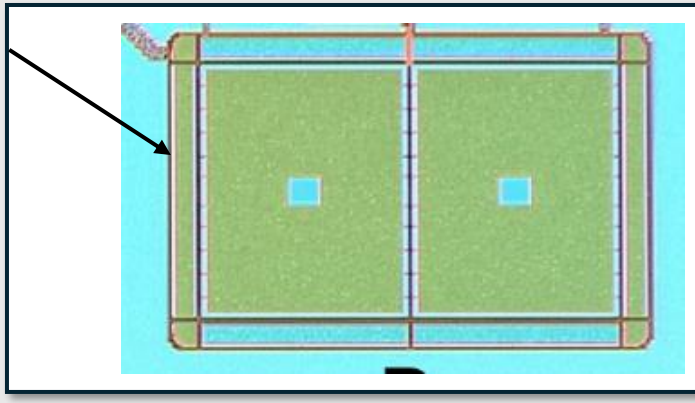
Breakdown Location - Measurements



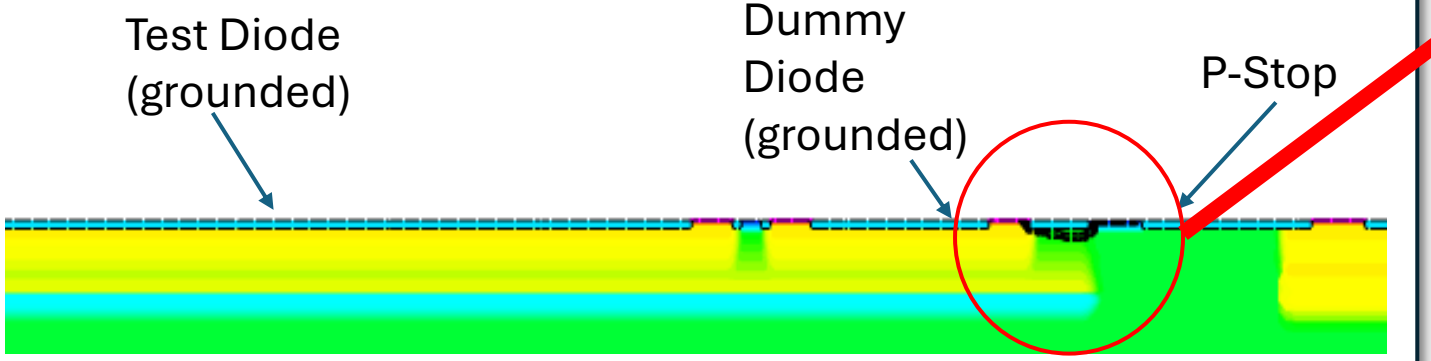
- Vast majority of current being drained through dummy diodes rather than the test diodes
- Suggests breakdown in ring scheme, gain termination or dummy diodes



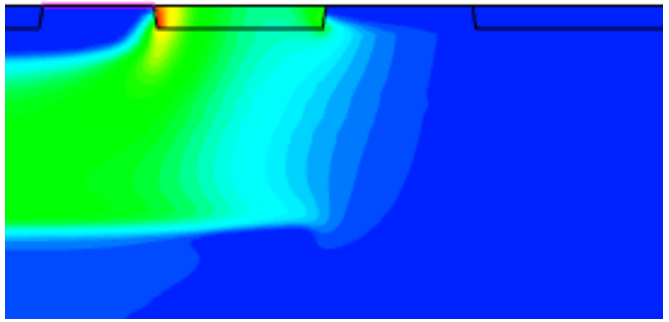


Breakdown Location - Simulation

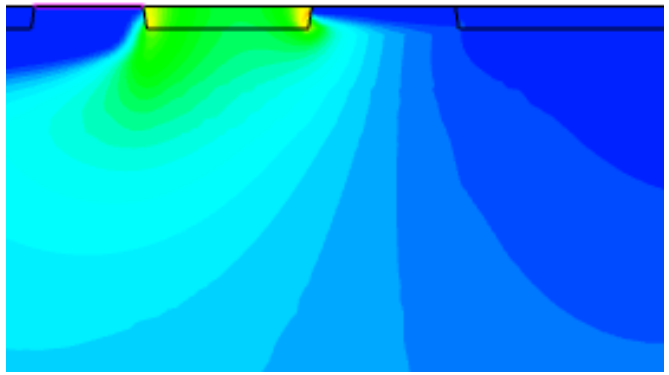
- Investigated the edge of the dummy diode within TCAD
- Breakdown observed between P-Stop and Dummy diode
- Location the same regardless of if gain layer is present or not
- Seen earlier in structure with gain – larger potential drop off between P-Stop and Dummy diode



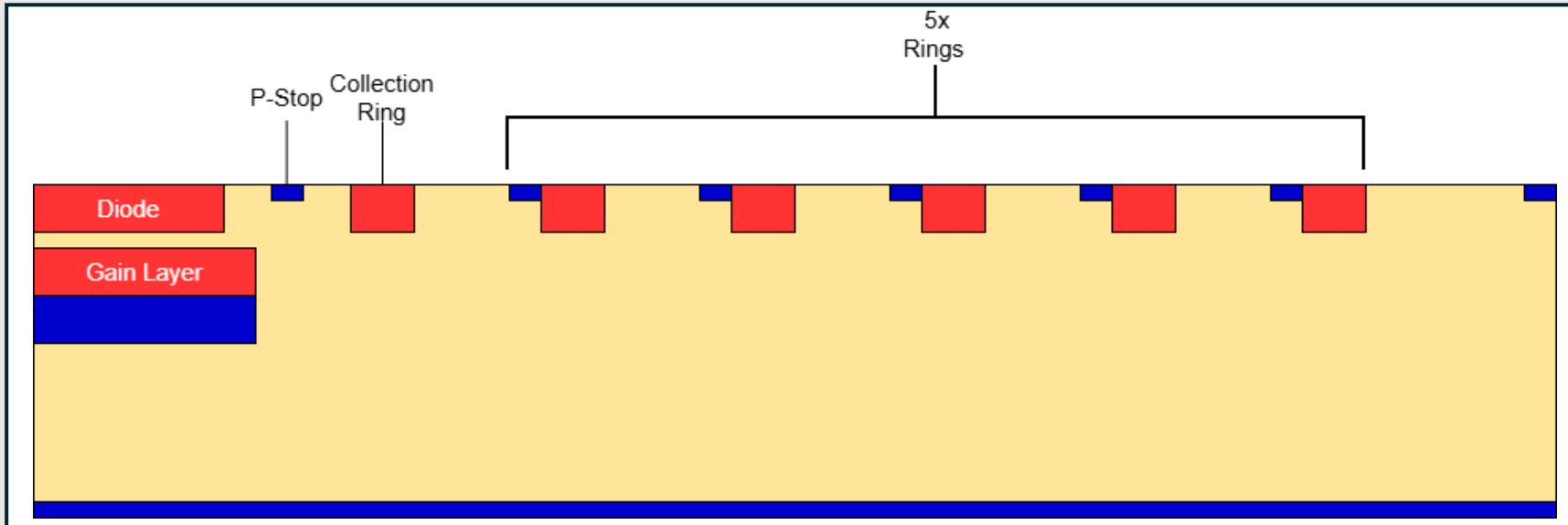
E-Field with Gain

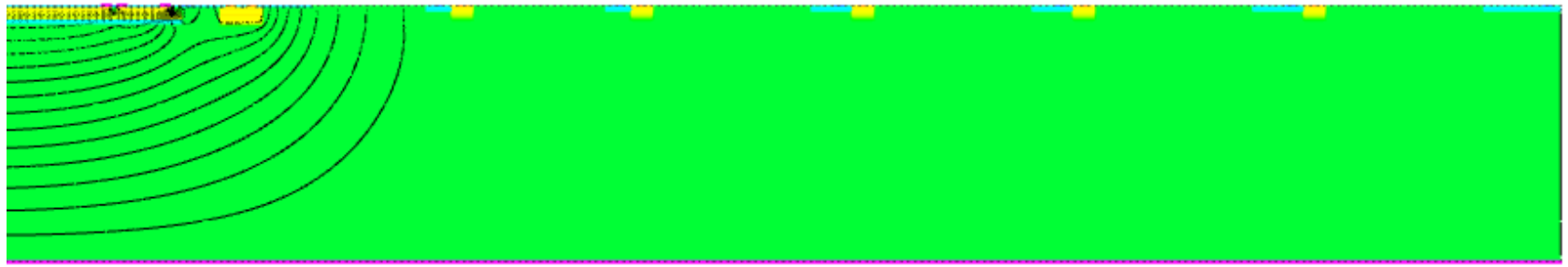


E-Field Without Gain



Ring Scheme Investigation



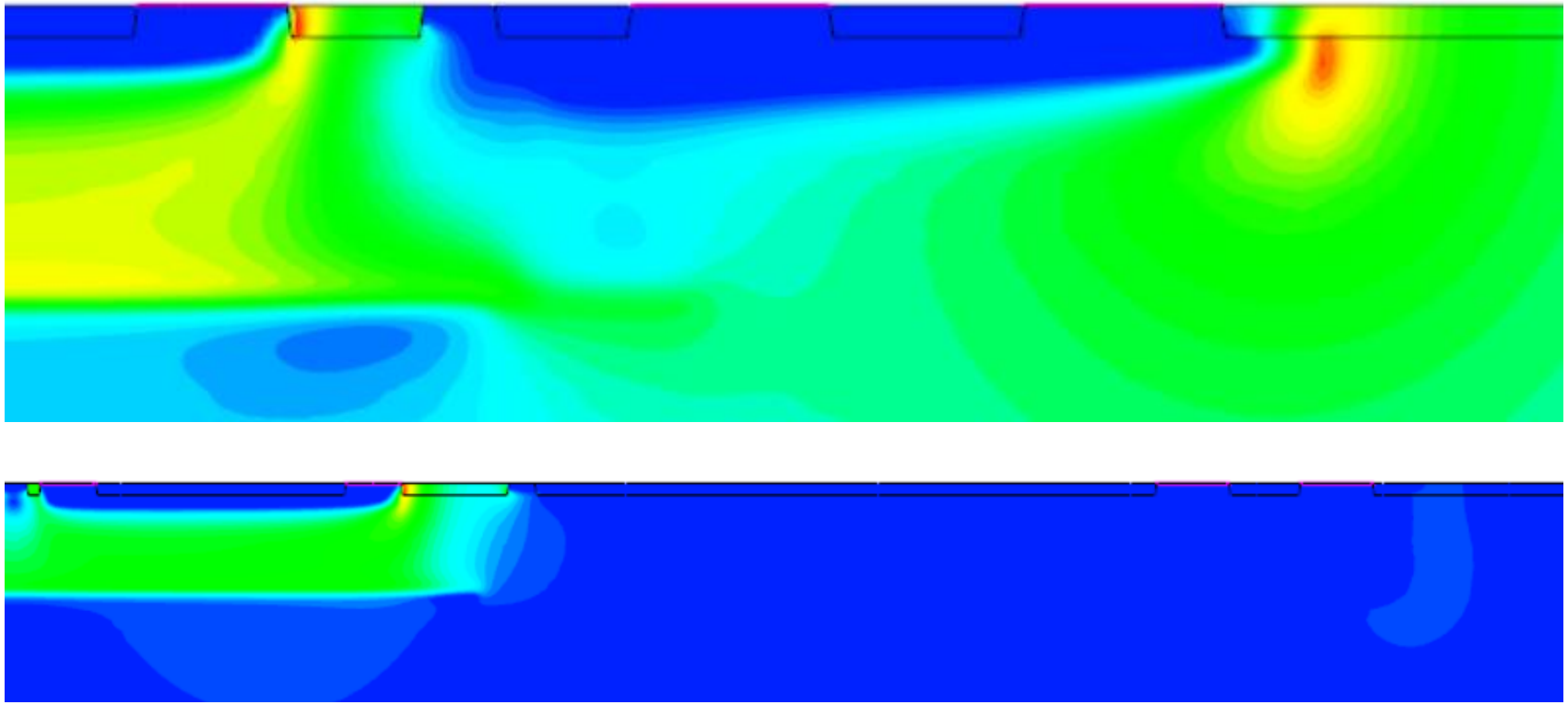


- Ring scheme for the Cactus-GL has been taken from LF-Monopix2
- Has not been optimised for use in gain layer
- Not effectively sharing potential and electric field

Ring Scheme Investigation

Dummy Diode

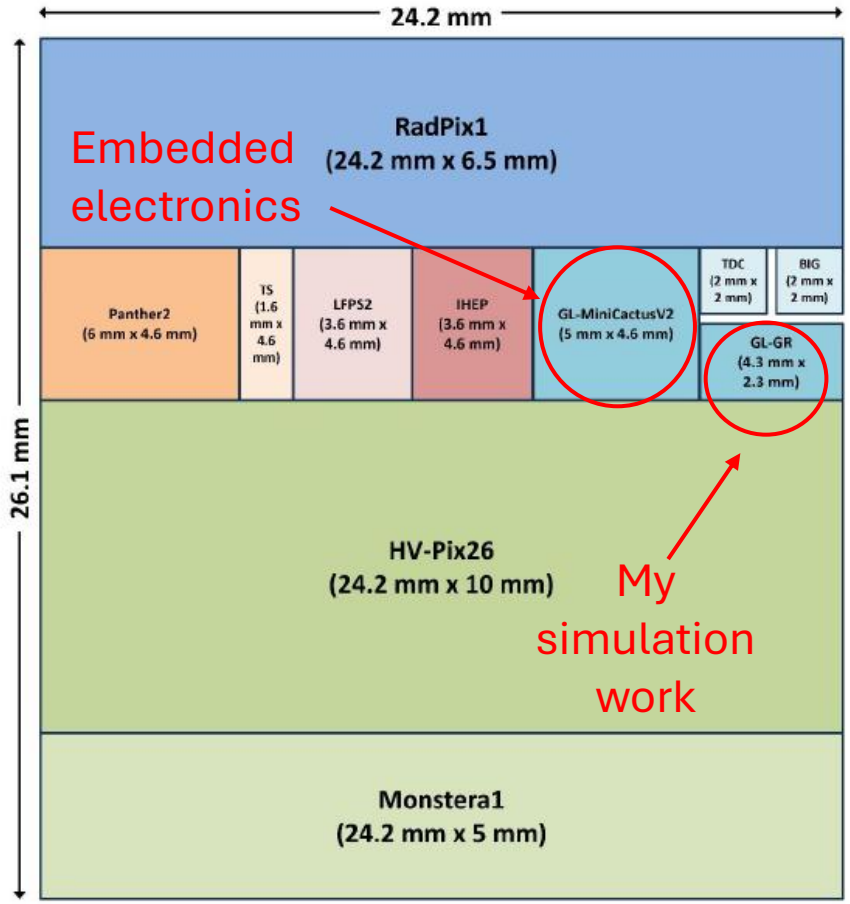
N-Ring



Electric field better shared by reducing distance to the first ring

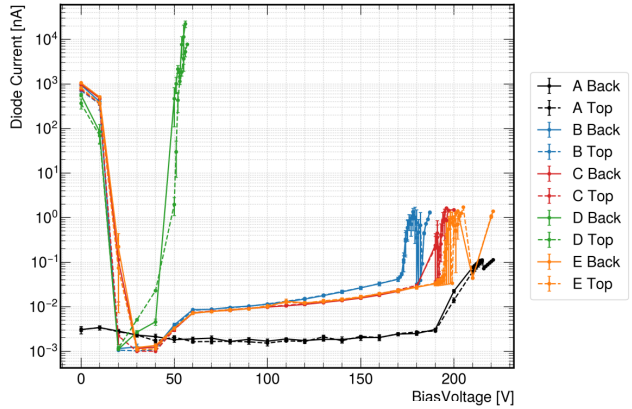
New Submission

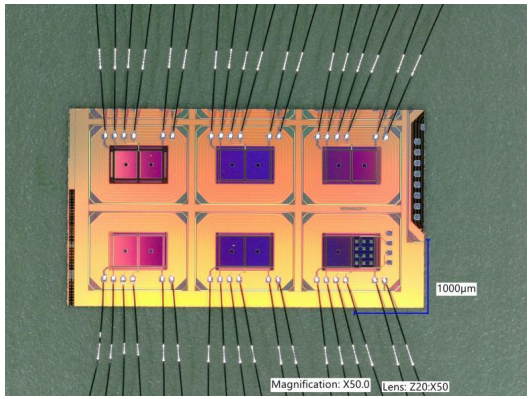
- New submission of new chips planned, as part of a DRD3 shared submission in 2026 in LFoundry 150 nm
- Plans to submit GL-MiniCactusV2, a new iteration of the MiniCactus chip, with the addition of a gain layer
- Also, the GL-GR chip, a chip with multiple test structures, optimising performance

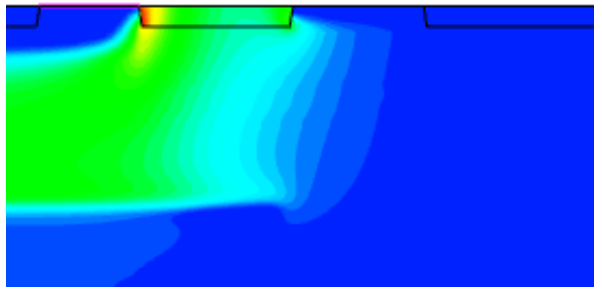


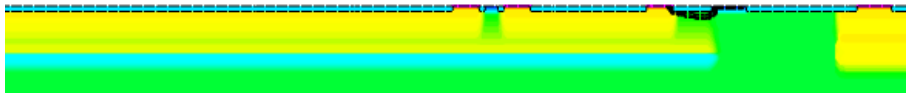
Outlook

- Achieved gain in CMOS
- Understood limitations of the chip
- Measurements are ongoing
- Irradiation study to come
- Timing study to come
- New submission of an improved chip planned for June 2026
- Now moved to FBK, Italy, to work on quantum sensors



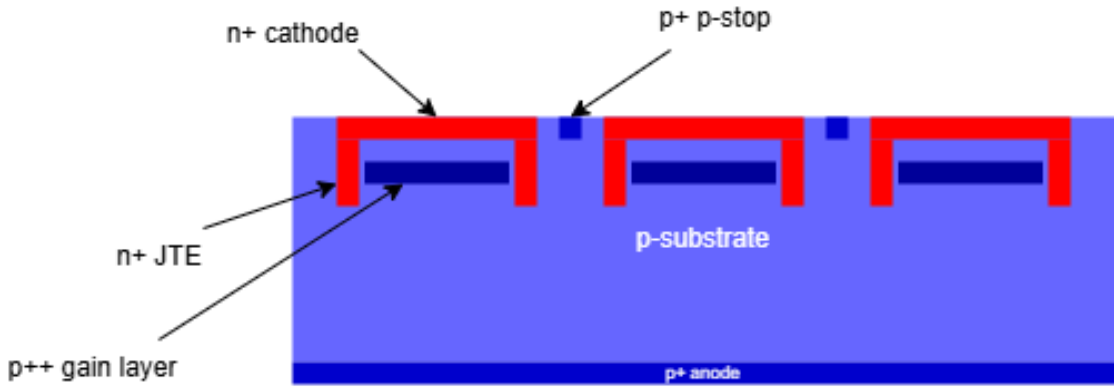


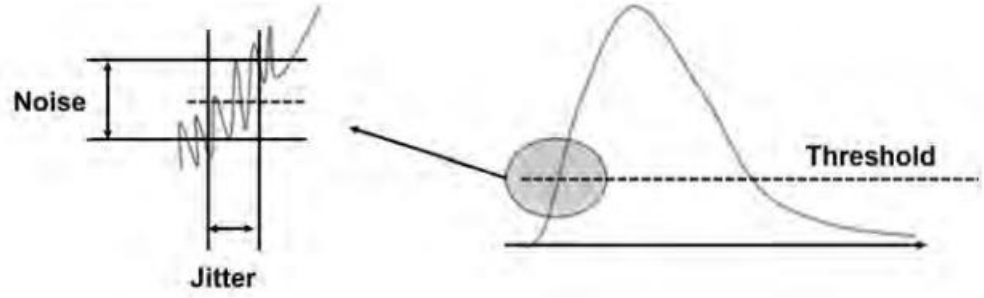




Backup - Low Gain Avalanche Detectors (LGADs)

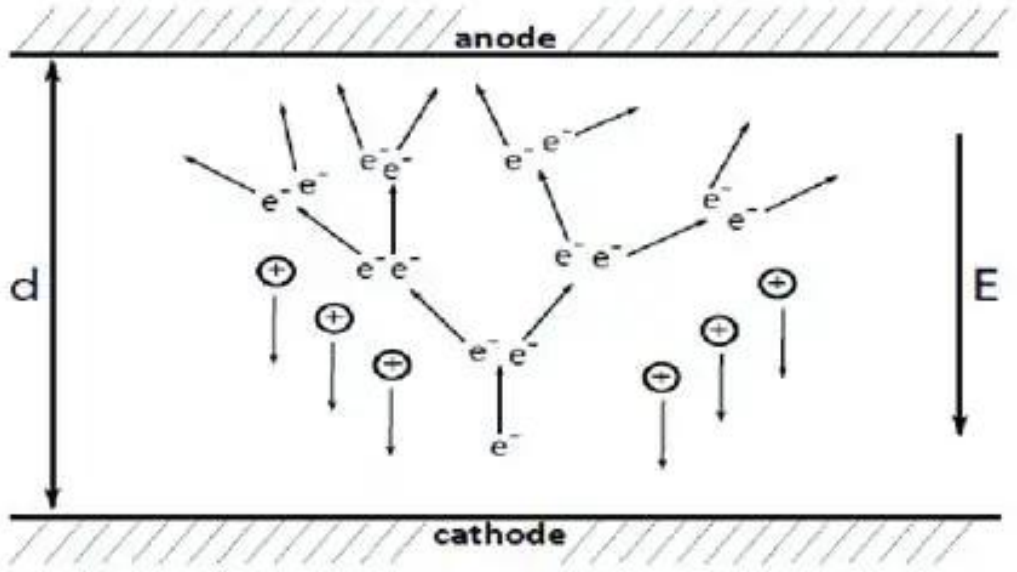
- Modified n-on-p silicon sensor with internal gain, surrounded by a Junction Terminal Extension (JTE)
- High localised electric field generated within the gain layer, resulting in electron avalanche and ultimately an amplified signal
- Gain layer enables charge multiplication ~×10
- Time resolution: ~30–50 ps
- Hybrid technology: sensor + external ASIC
- Trade-offs: better timing vs. more material & scattering





Backup - Electron Avalanche

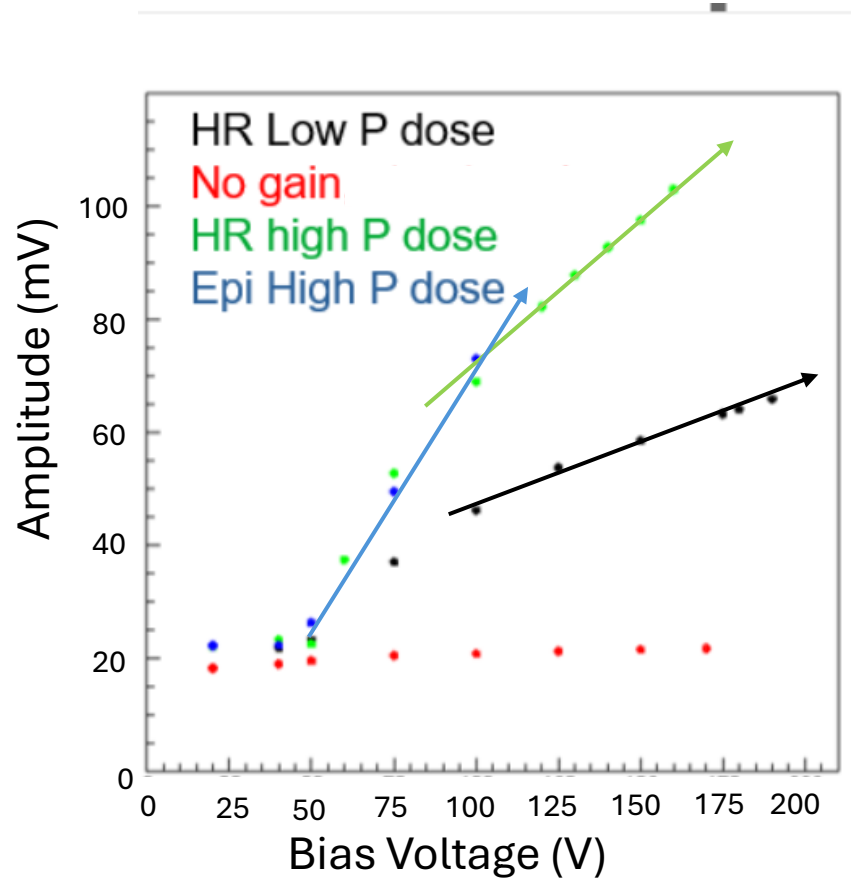
- High electric field within the highly doped gain layer
- Accelerates the electrons – ultimately resulting in impact ionisation creating further electron hole pairs
- This in turn creates an overall signal gain between 10x-40x



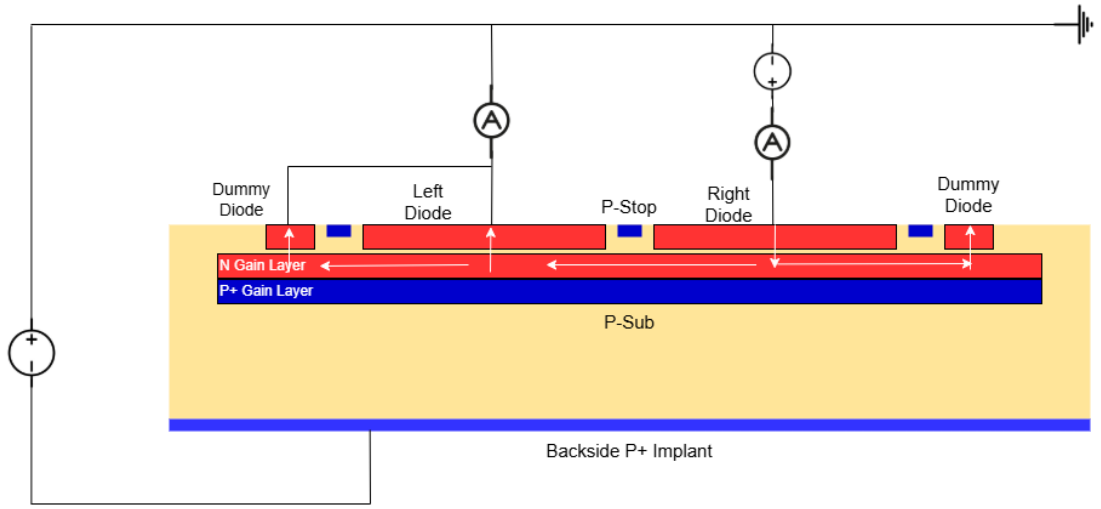
[3] Diagram of electron avalanche

Backup - Gain Measurements

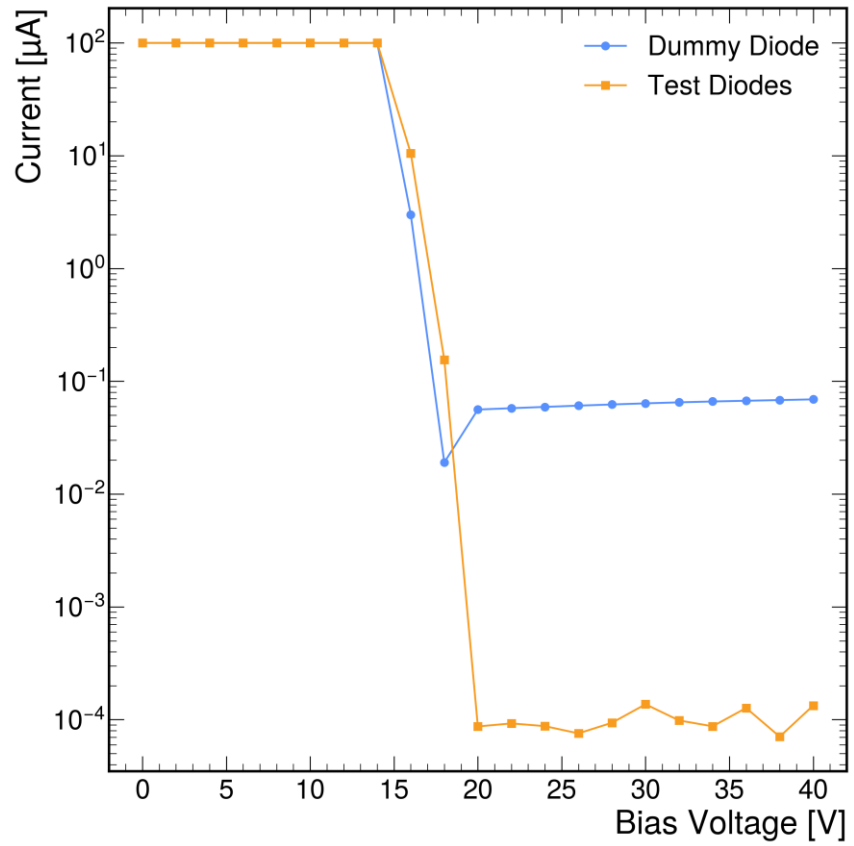
- Measurements taken at CEA with a 940nm IR laser
- Highest gain in high concentration wafers
- Voltage dependence on gain
- PCB with included FE under development
- Samples have been sent to take part in a DRD3 common proton irradiation campaign at Fermilab



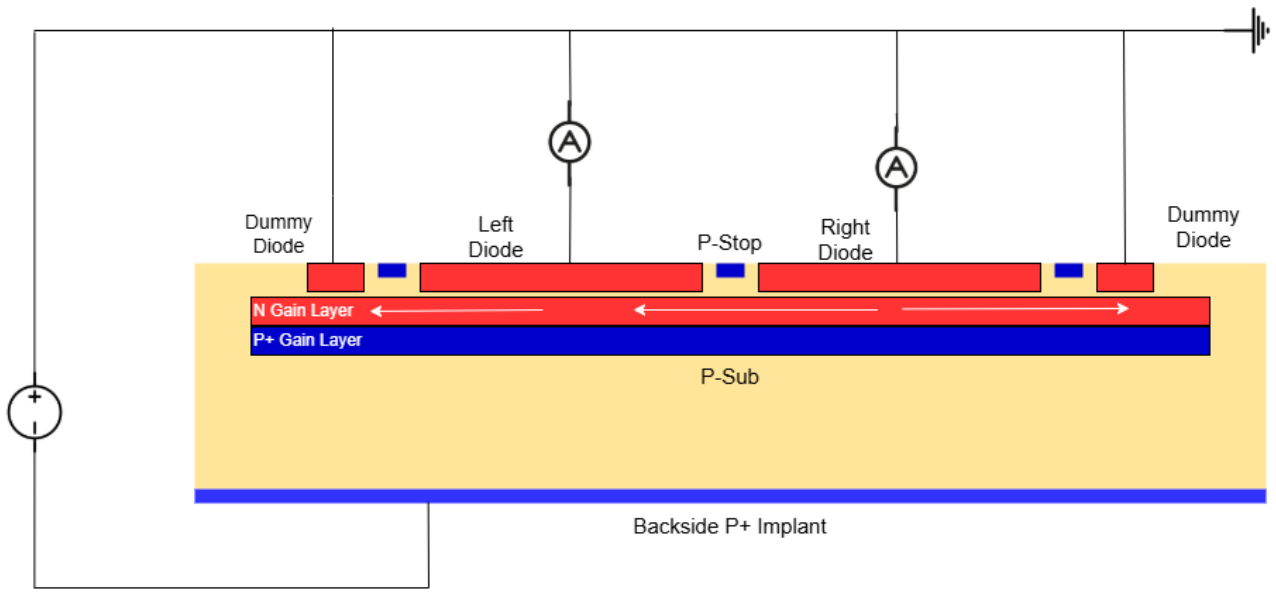
Backup - Channel Currents

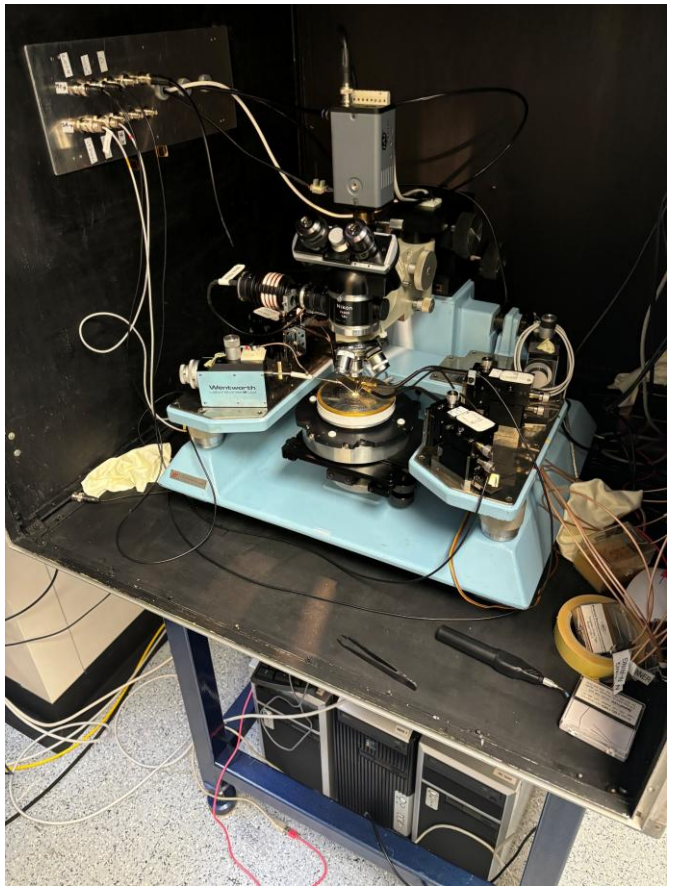


- Channel exists through N-Gain layer between both the diodes and dummy diodes below 20V
- Once the N gain layer is depleted, channel is removed

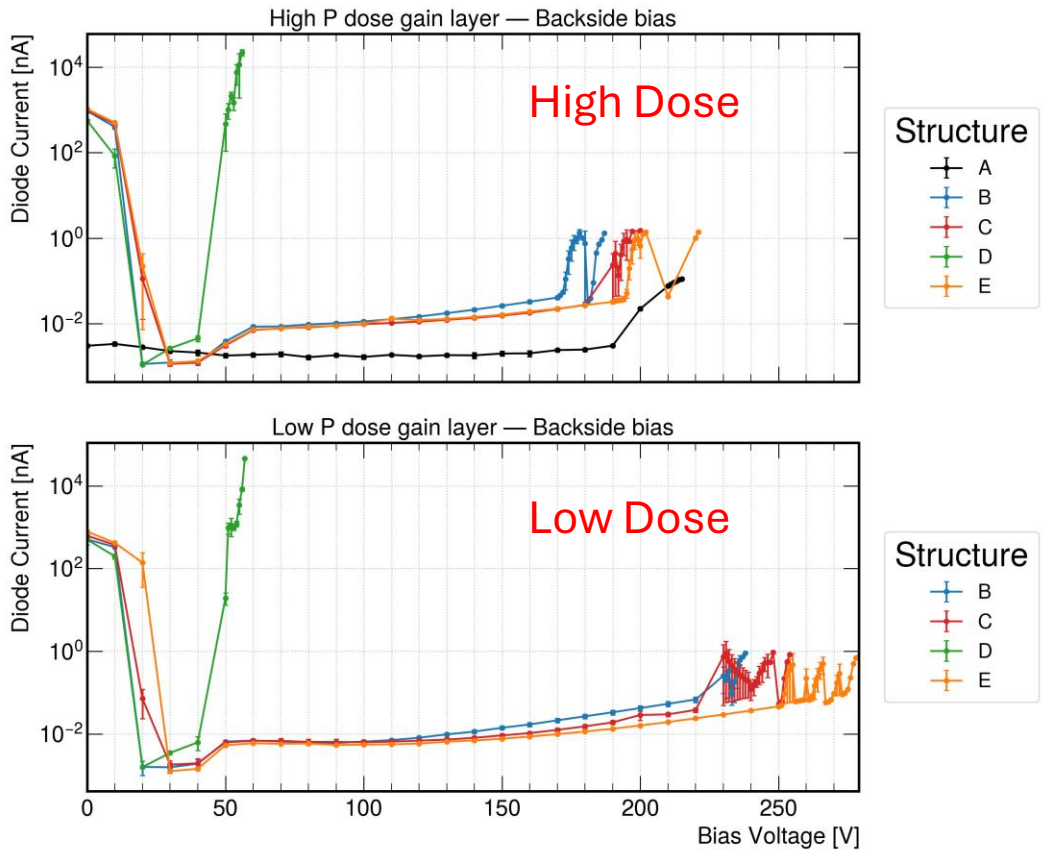


Backup – IV Setup

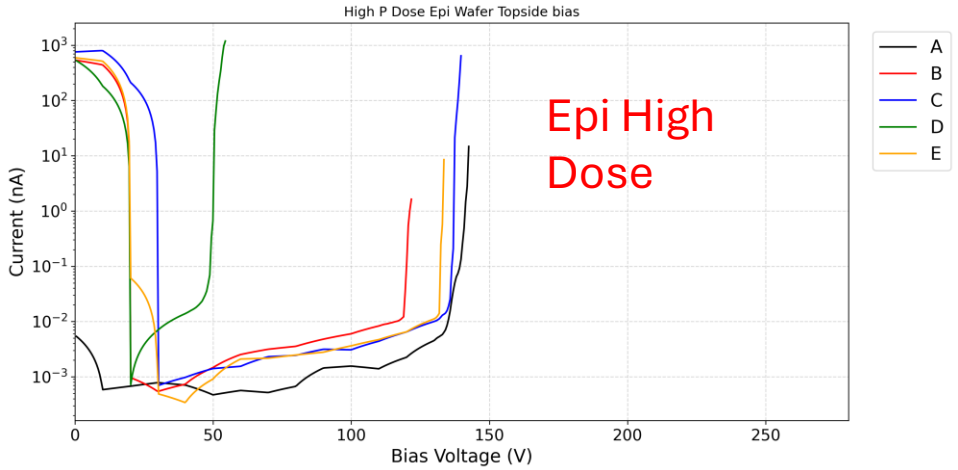




Backup I-V's



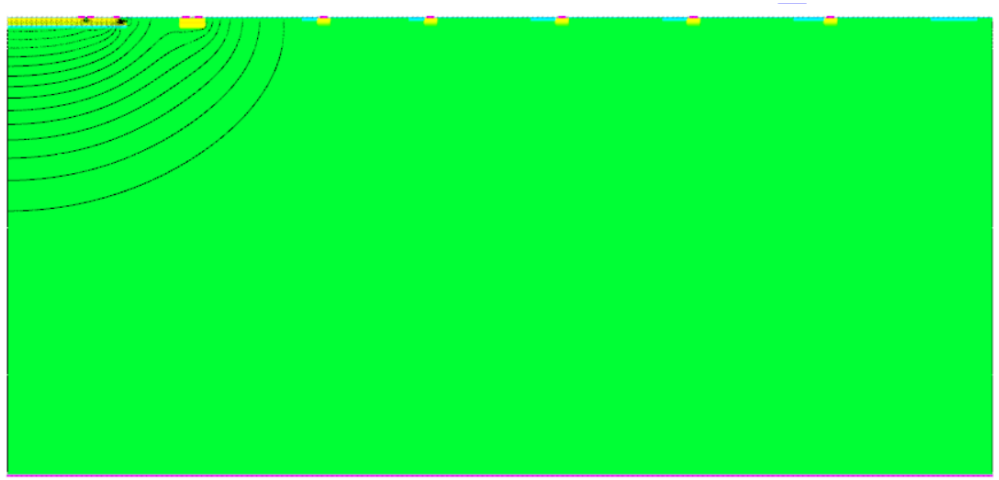
- High P dose wafer has systematically lower breakdown
- Suggests breakdown is gain layer dependent – higher electric field in high gain structures



Backup – Chip Thickness

- Ring scheme functionality has no dependency on sensor thickness

150 µm



50 µm