LHCb Upgrade II

on behalf of Mighty Tracker group

Karol Hennessy

2026-05-22

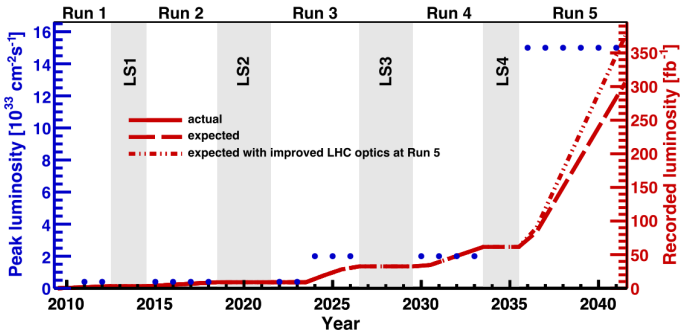
UNIVERSITY OF LIVERPOOL

LHCb

LHCb Upgrade II

- Physics programme limited by detector, NOT by LHC

$\Rightarrow$ upgrade to get the maximum physics LHC can deliver

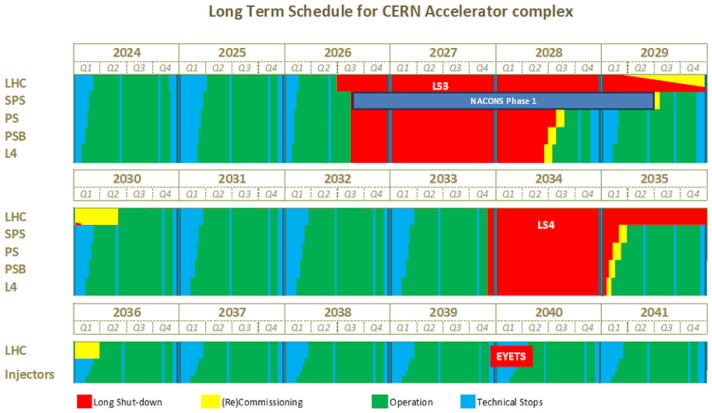


Upgrade I

- $L_{peak} = 2 \times 10^{33} cm^{-2} s^{-1}$

Upgrade II

- $L_{peak} = 1.5 \times 10^{34} cm^{-2} s^{-1}$
- $L_{int} = 300 fb^{-1}$ during Runs 5 & 6. Installation in LS4



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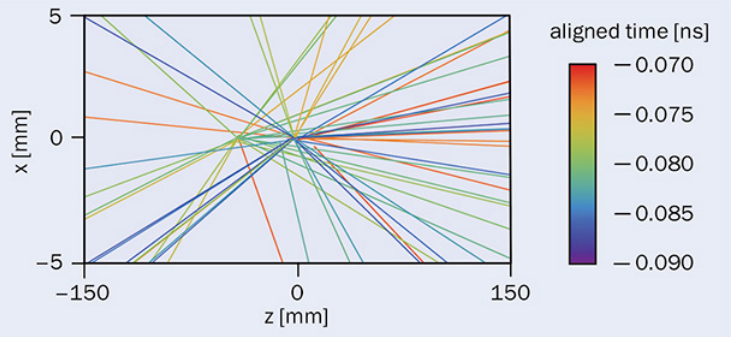
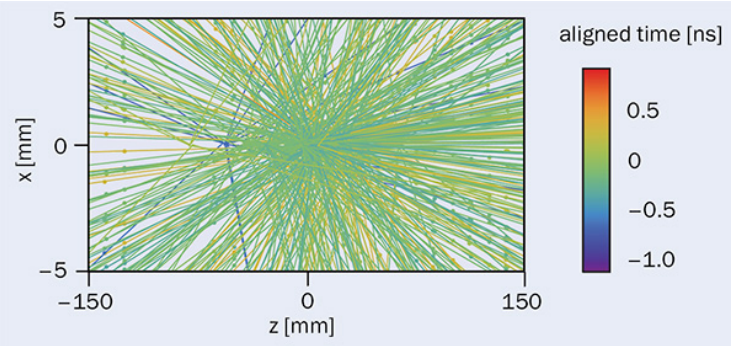
Tracks today:



Tracks at Upgrade 2 luminosities:



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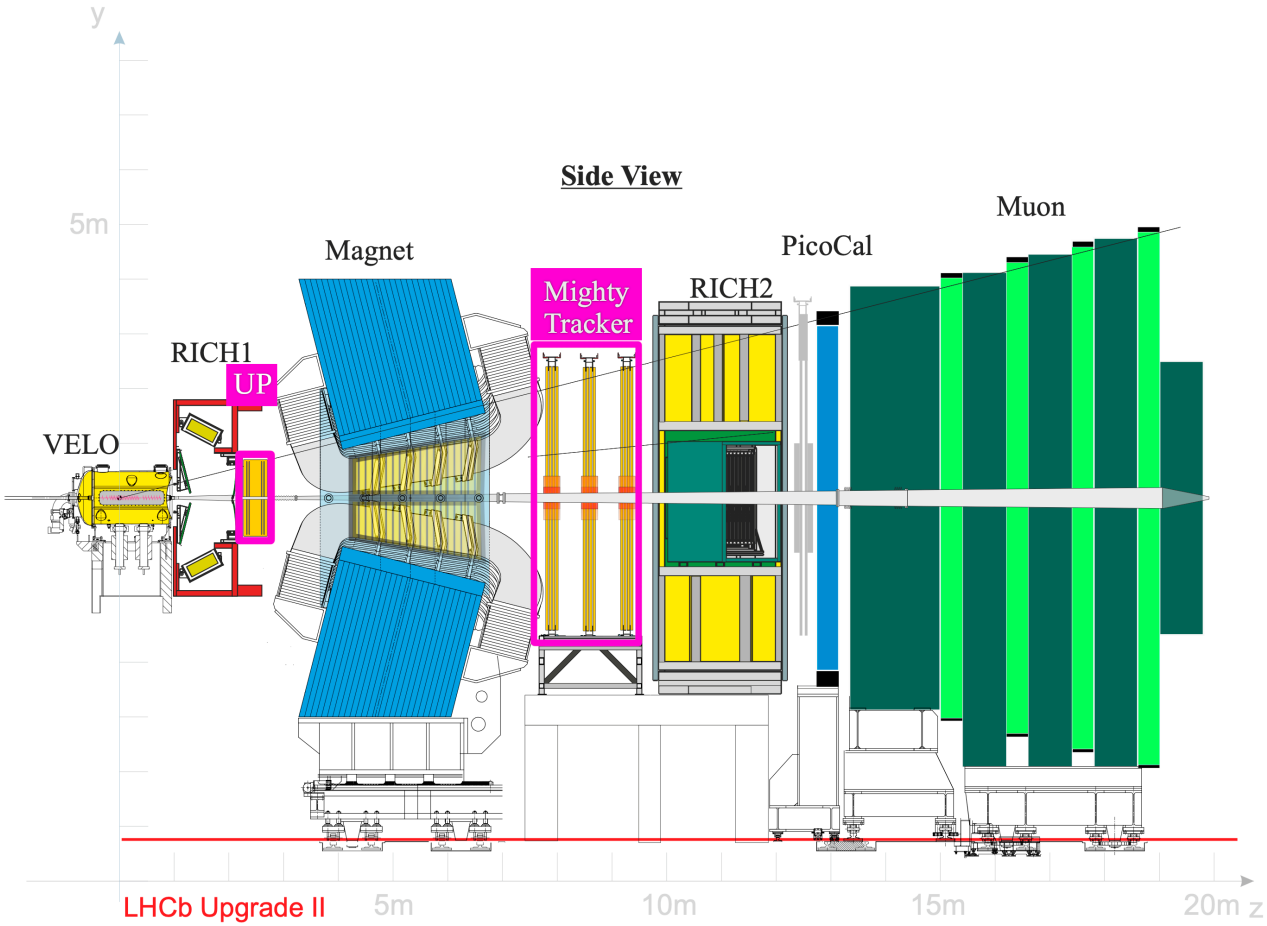
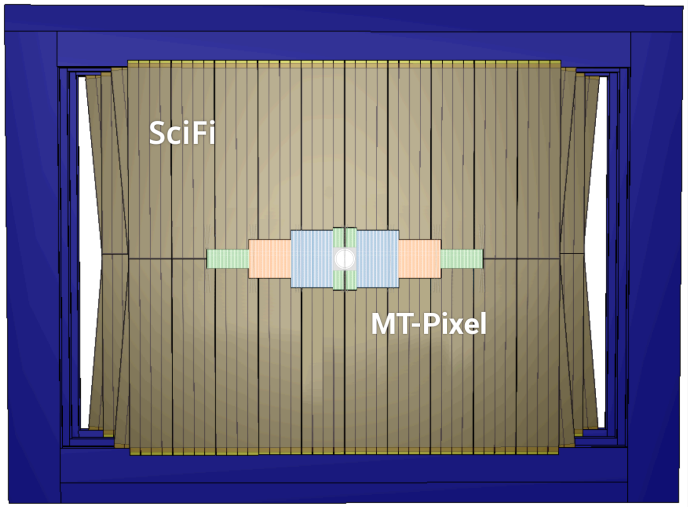
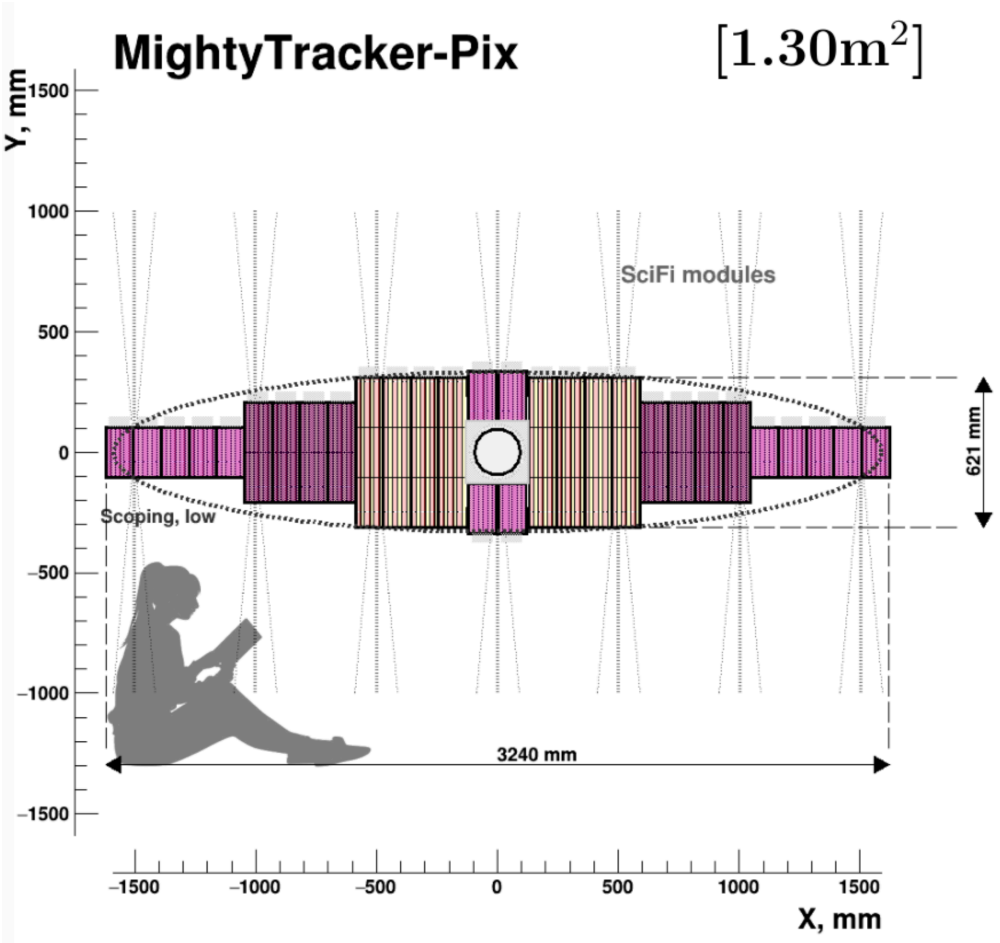




Mighty Tracker - Scifi + **Pixels**

Mighty Tracker



Requirements

Parameter	MP specification
Pixel size (x)	≤ 100 µm
Substrate thickness	100 – 200 µm
Max. Particle Rate	37.6 MHz/cm²
Max. Hit Rate	18.8 MHz/cm²
In-time efficiency	> 99% within 25 ns
NIEL	2.4×10^{14} n_eq/cm²
TID	24 MRad
Power consumption	≤ 150 mW/cm² + 30% overhead for serial powering

- Hit efficiency > 96%
- Low power, high radiation tolerance

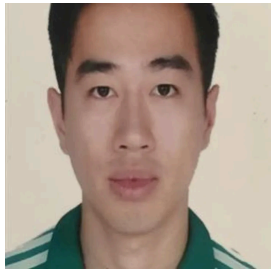
Mighty People

Eva Vilella Figueras: Mighty-Pixel UK lead, Mighty-Tracker deputy PL

Me: DAQ WP co-coord., backend development

Bilal Ganie: Assembly techniques & procedures

Maria Cecilia Queiroga Bazetto: Mechanical assembly, starts PhD. Oct.



Chenfan Zhang: Radpix chip design (pixels)

Sven Wonsak: Jig design & testing procedures

Ashley Greenall: Hybrid and flex design

George Stavrakis: FEA simulation

Sam Powell: Radpix chip design (Serial Power) & DAQ

Kieran Bridges: Mechanical design

Mighty Tracker Collaboration

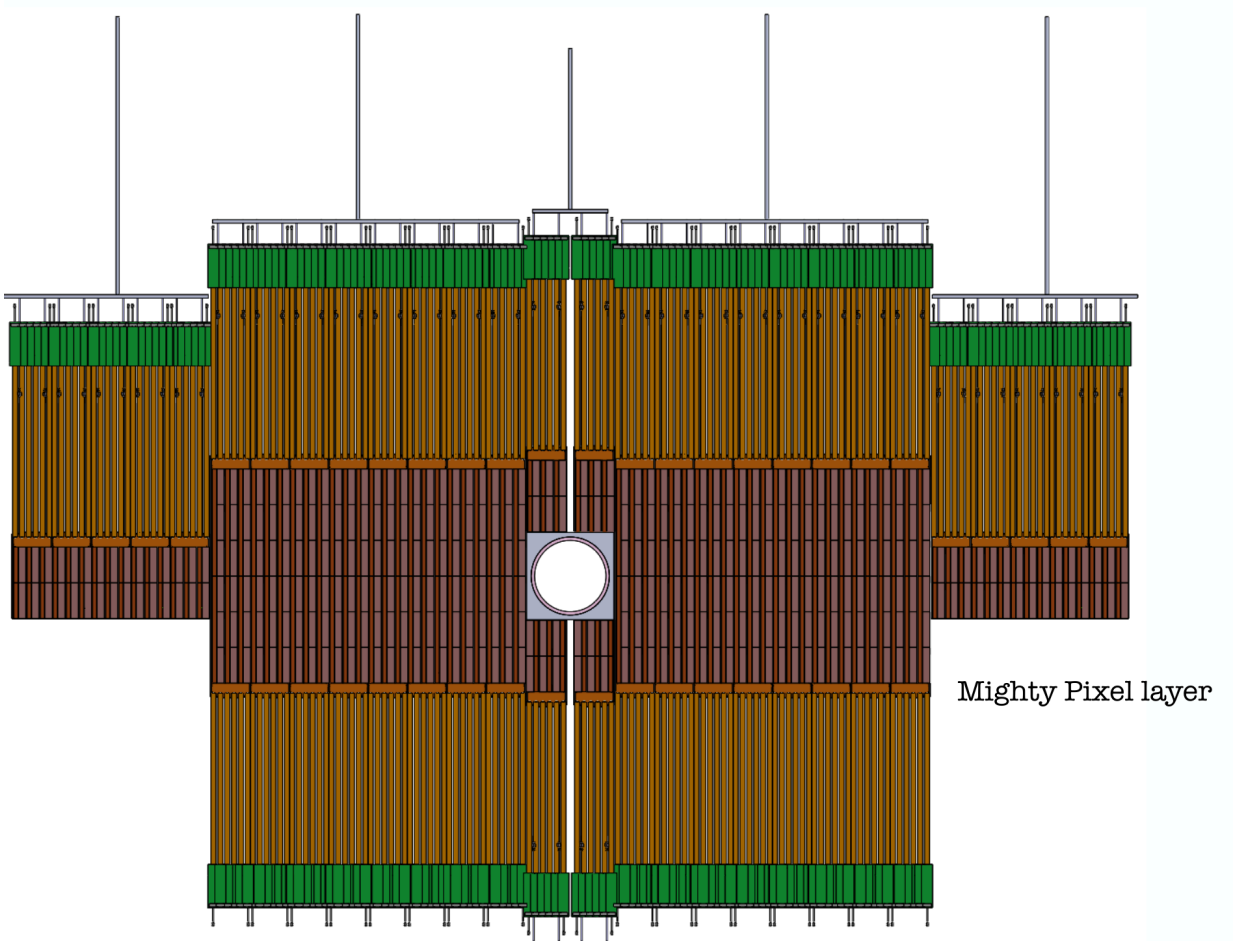
Mighty Tracker Collaboration

🍺 A beer for whoever spots the most AI slop mistakes in this image! 🍺

Milestones

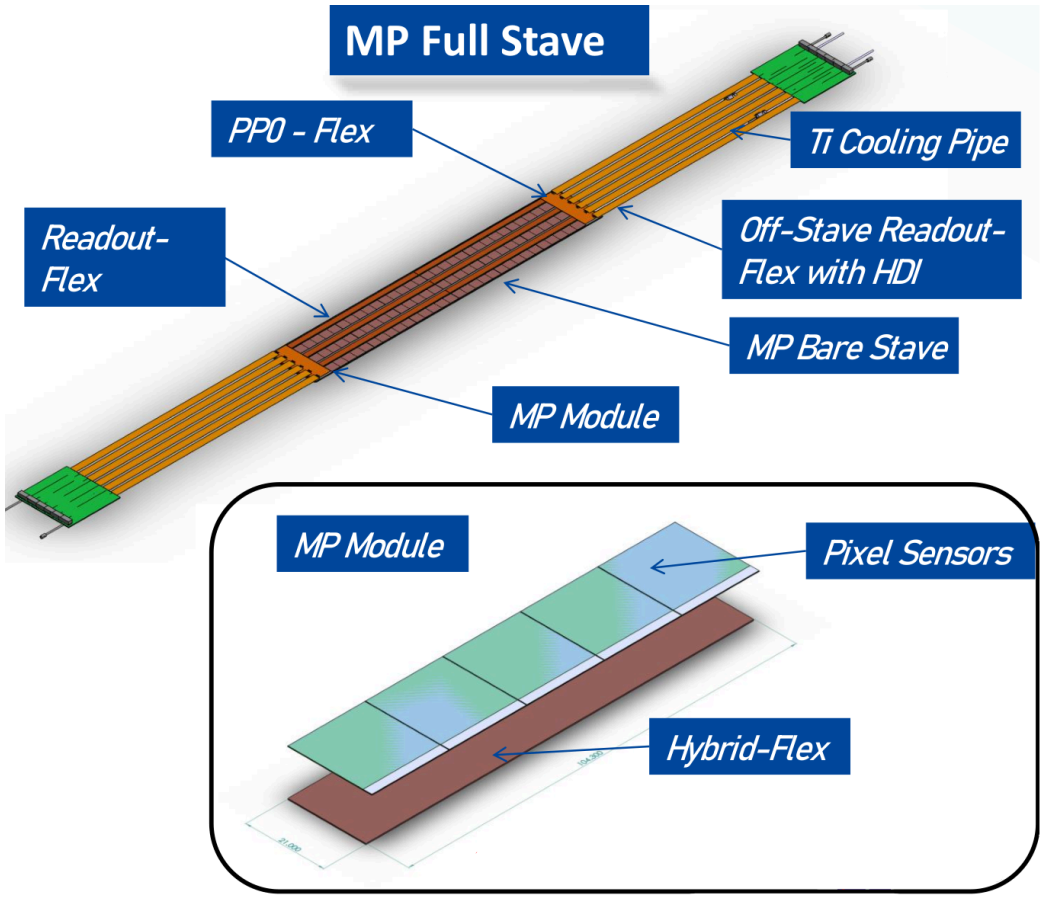
			Progress
SciFi	Completion of a cryobox demonstrated program	Q4 2025	advanced
	Demonstration of radiation hardness of SciFi technology	Q1 2026	advanced
Pixel	Demonstration of radiation hardness of MAPS technology	Q2 2025	done
	First test results of Mighty-Pixel chip	Q2 2026	See later
	Concept of a readout flex	Q3 2025	done
	Baseline design of the module Now Full Stave	Q3 2025	done
	Proof of concept of a module	Q1 2026	advanced
Mighty	Concept design of electronics architecture	Q2 2025	done
	Concept design of mechanical integration of the Mighty-Tracker (SciFi+Pixel)	Q4 2025	ongoing
	Proof of concept of a Pixel insulated enclosure box	Q2 2026	ongoing

Layer design



- 6 layers of staves
- 6 columns per stave
- columns have 2-3 modules
  - alternate back and front sensors
- 5 sensors per module
- patch panels at end of long readout flex

Stave design

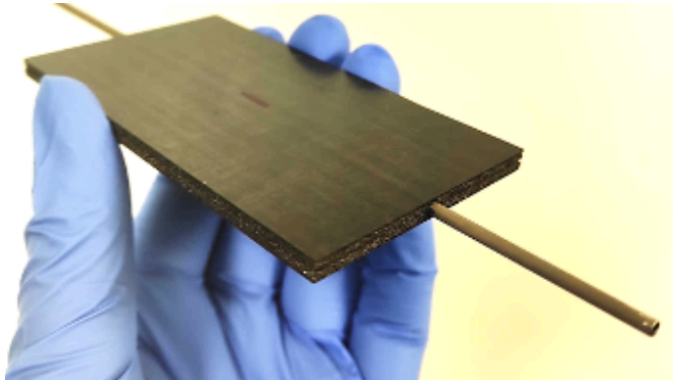


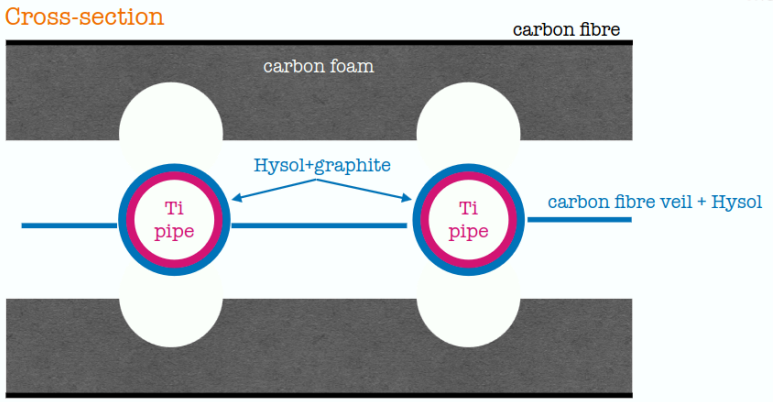
Liverpool focus for prototyping and production

- Flexes for hybrid and data
  - electronics testing
  - Serial powering
  - HV design
  - Readout
- Chip design and testing
- Module mounting and tooling
- Carbon fibre support
- Assembly procedures

Bare Staves

P. Sinclair, T. Jones





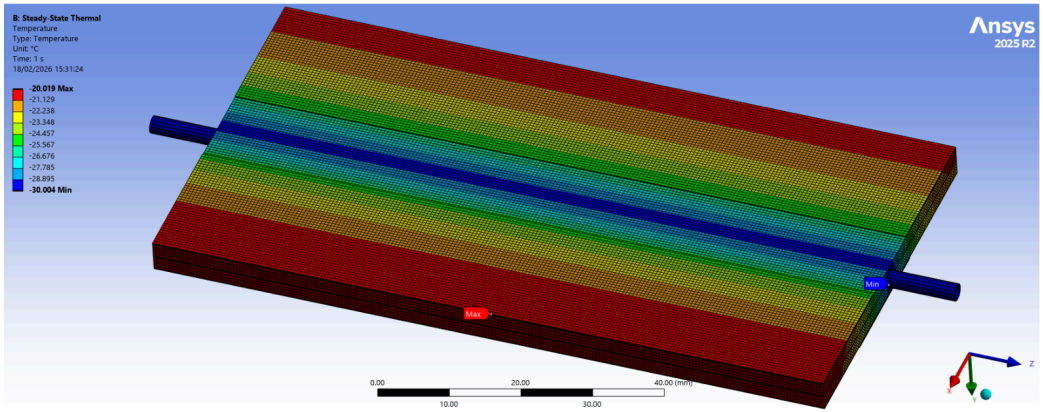
- Need large uniform rigid objects
- Carbon fibre structures made in AML

- Then sent to Manchester to assemble bare staves with CF and cooling pipes
- Thermal/Mechanical mockups being made at U.Freiburg too

FEA modelling of modules

G. Stavrakis

- Method to perform FEA much faster
- Thermal models prepared using Creo and transferred/redefined in Ansys
- Compare to Solidworks
- Working closely cooling experts in Manchester

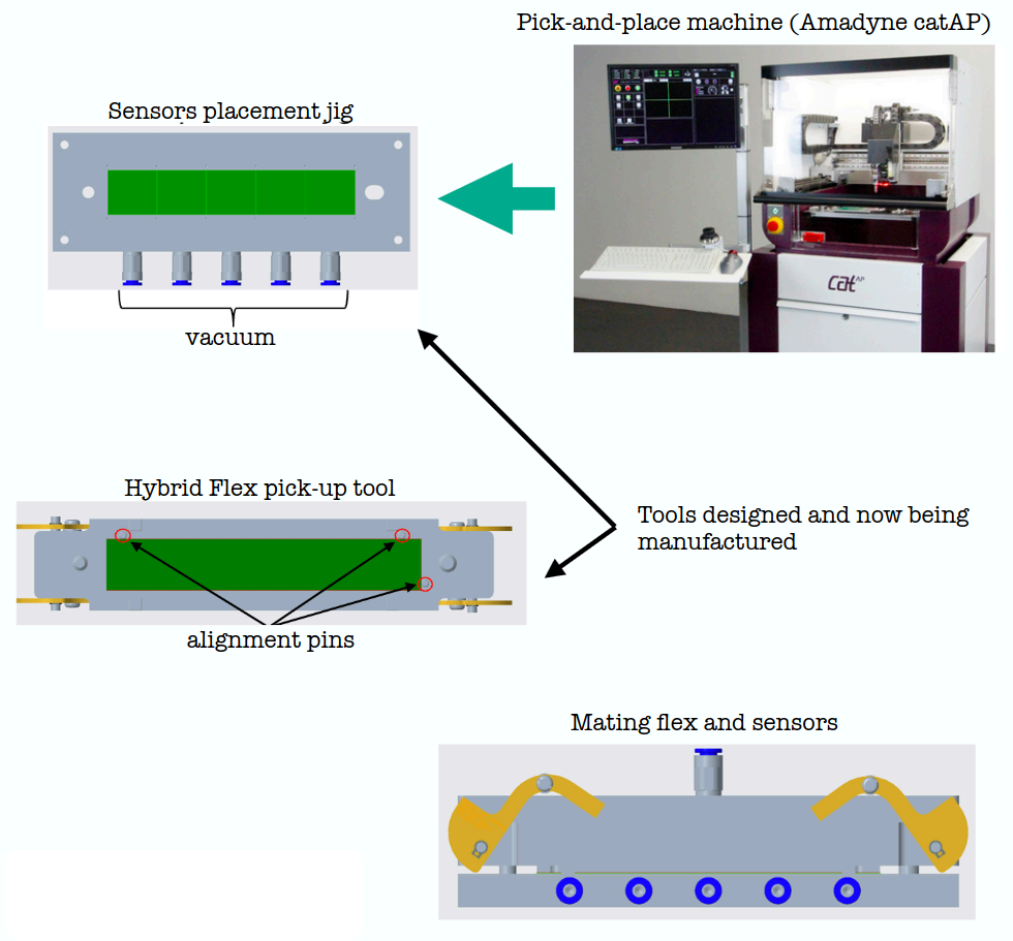


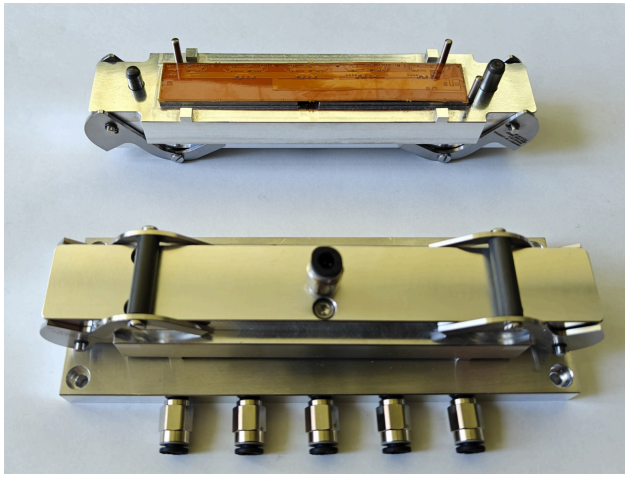
Results for Baby Stave

	Kapton Heaters ΔT	Silicon Heaters ΔT
Ansys	$13.96^{\circ}C$	$9.98^{\circ}C$
Solidworks	$13.8^{\circ}C$	$10.5^{\circ}C$

Jigs and tooling

A. Greenall, S. Wonsak

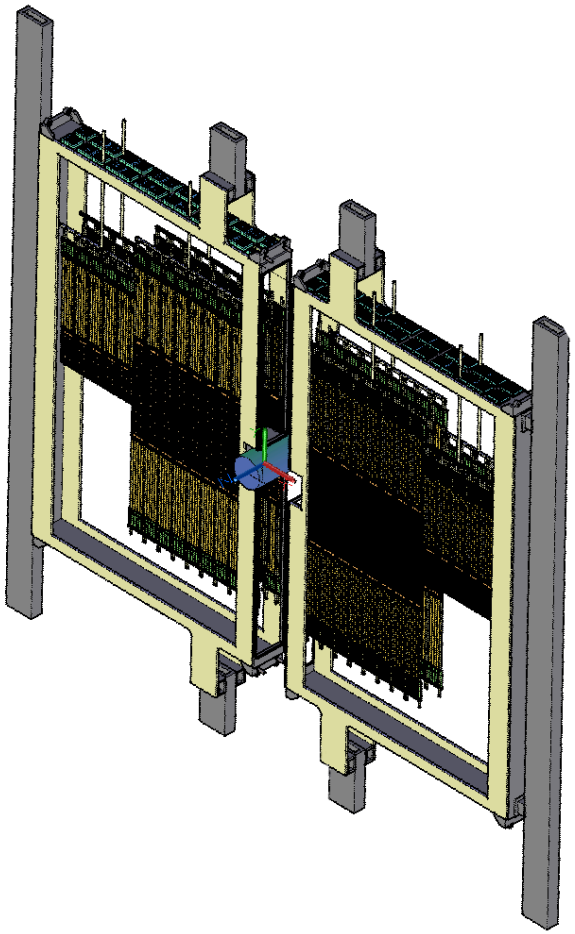




- Livepool Design (Sven)
- Fabricated in Heidelberg, came back with some chip dummies from Bonn

Enclosure

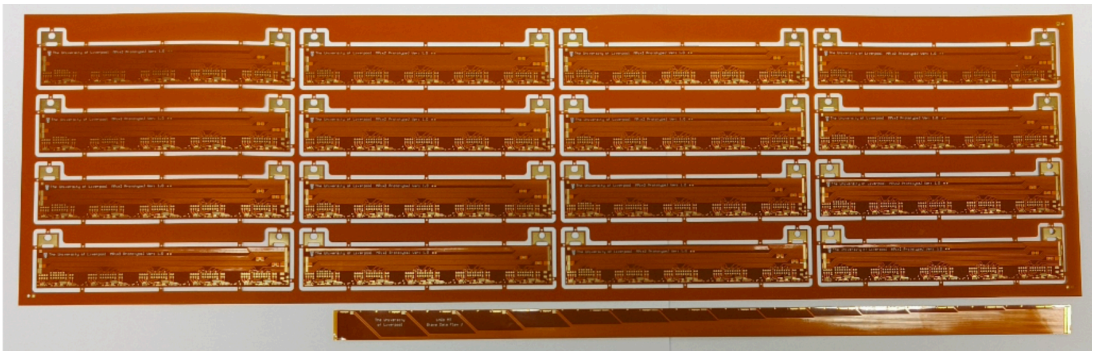
- Imperial contribution to Mighty Tracker ending
  - Sharing current designs
- New groups required for enclosure box
  - New interest from:
    - Edinburgh
    - Krakow
    - CBPF (Brazil)
    - Liverpool (Kieran)
  - In discussions with RAL and Manchester on how best to contribute

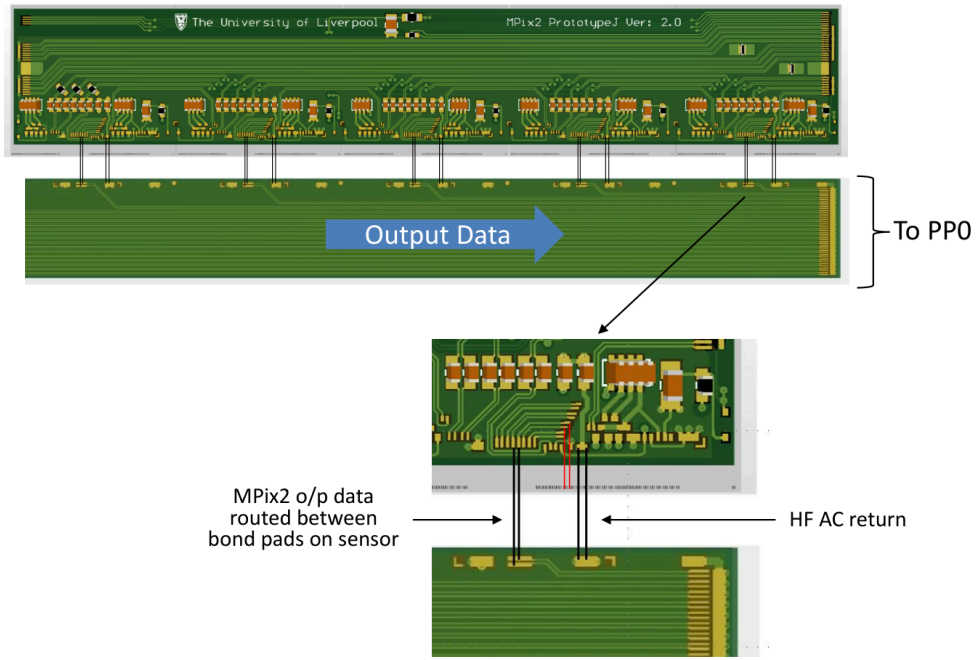


Hybrid and data flex prototypes

A. Greenall

- First flex prototypes arrived end of 2025
  - double-sided, Cu clad polyimide laminate with polyimide cover layers
- Testing with chips and glass dummies
- Good signal quality in first scope tests





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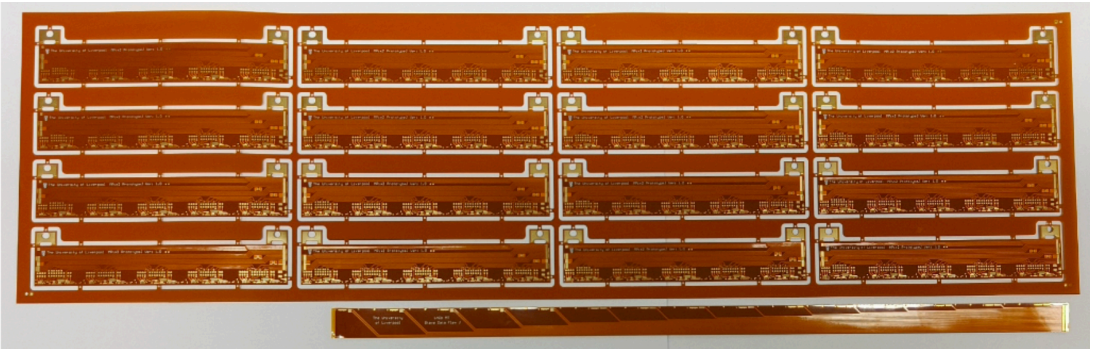
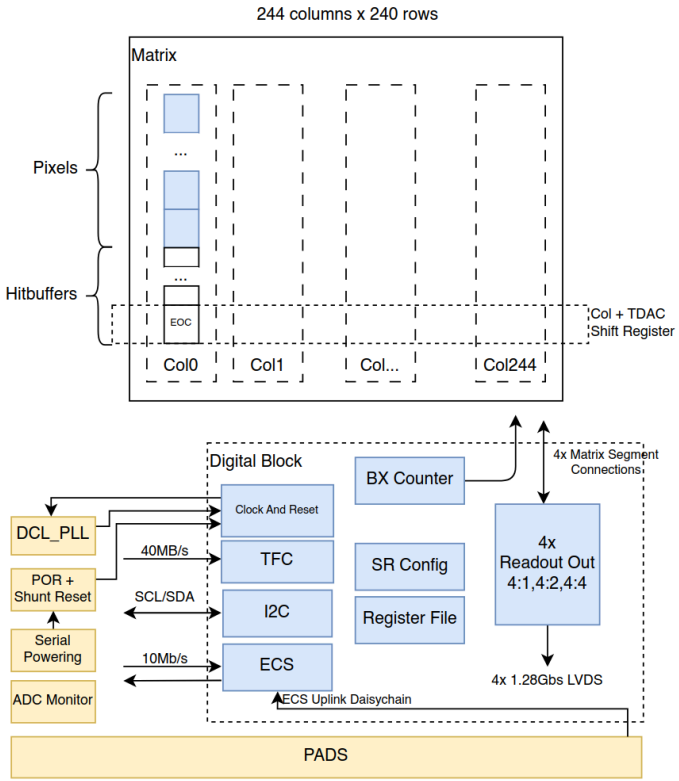
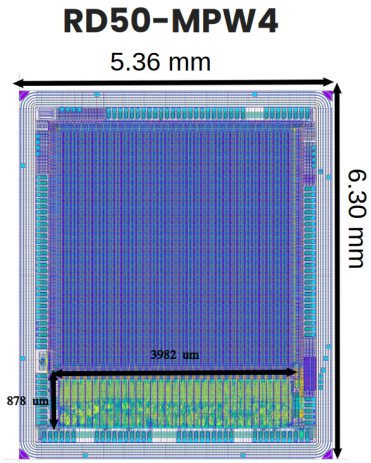


MightyPix 2

- submitted to AMS for fabrication at end 2025
- fabrication delayed (for several reasons)
- expected Dec. 2026
- Therefore, not available for TDR
  - Results from related LF-MightyPix (v. successful testbeam in April) and P2Pix
  - Serial powering tests planned with ATLASPix3 and M-Pixel hybrids adapted (New WG)



RadPix : evolving RD50-MPW4



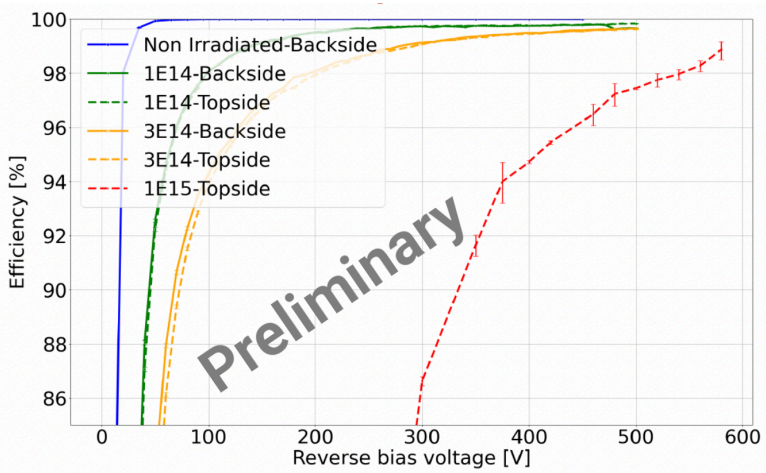
- 62 µm x 62 µm pixels
- 64 x 64 pixels matrix
- In-pixel low-noise
- Backside HV biasing
- VBreakdown > 600 V
- small leakage current

Unirradiated

- Efficiency measurements show full efficiencies > 99% up to thresholds of 200mV (HV = 190 V)

Irradiated

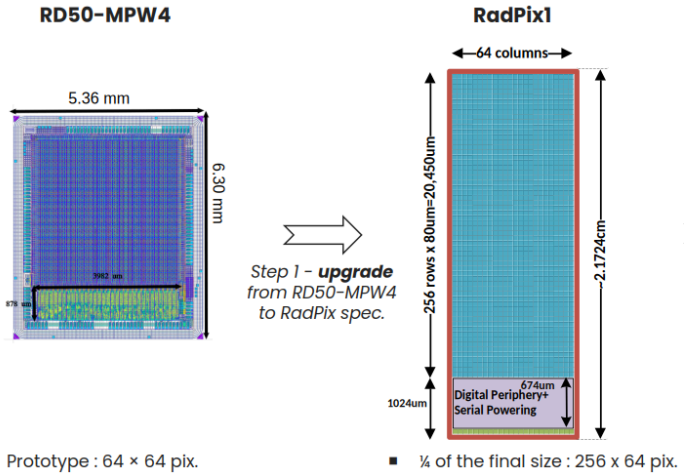
- Test-beam for irradiated sensors and increase of Vbias
- 99% efficiency up to $1 \times 10^{15} n_{eq} \cdot cm^{-2}$ @ HV = 580 V, T = −20°C



Main objectives for RadPix1

A more LHCb compatible chip

- **Power density**: Power (150 mW/cm2), while keeping 99% in-time efficiency within 25ns.
- 95% sensitive area: Careful floor planning
- **Upgrade digital periphery**:
  - LHCb communication protocols.
  - sensible approach reduce power consumption



- **Porting and developing necessary IPs**: Serial powering, LVDS drivers and receivers, Power-on-Reset.
- Candidate for UP detector as well as Mighty Pixel
- **Institutes:** Liverpool, RAL, Cambridge, Glasgow, Paris-Saclay, Barcelona

RadPix : sensor design

WP1 - Pixel Matrix

- Optimisation of the Pixel array size and power consumption.

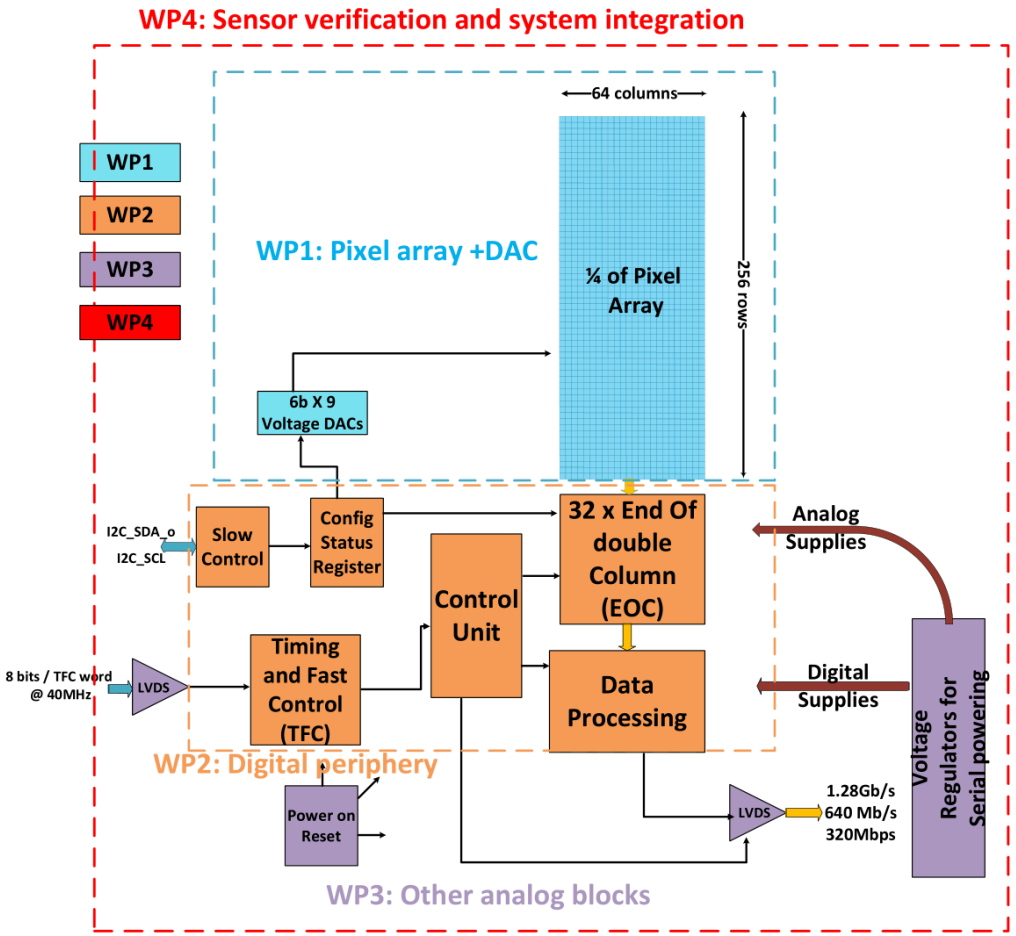
WP2 - Readout Periphery

- RTL description of the digital readout periphery + Place&Route

WP3 - Analog blocks

- Design of Shunt LDOs for serial powering
- LVDS drivers and receivers
- Power On Reset

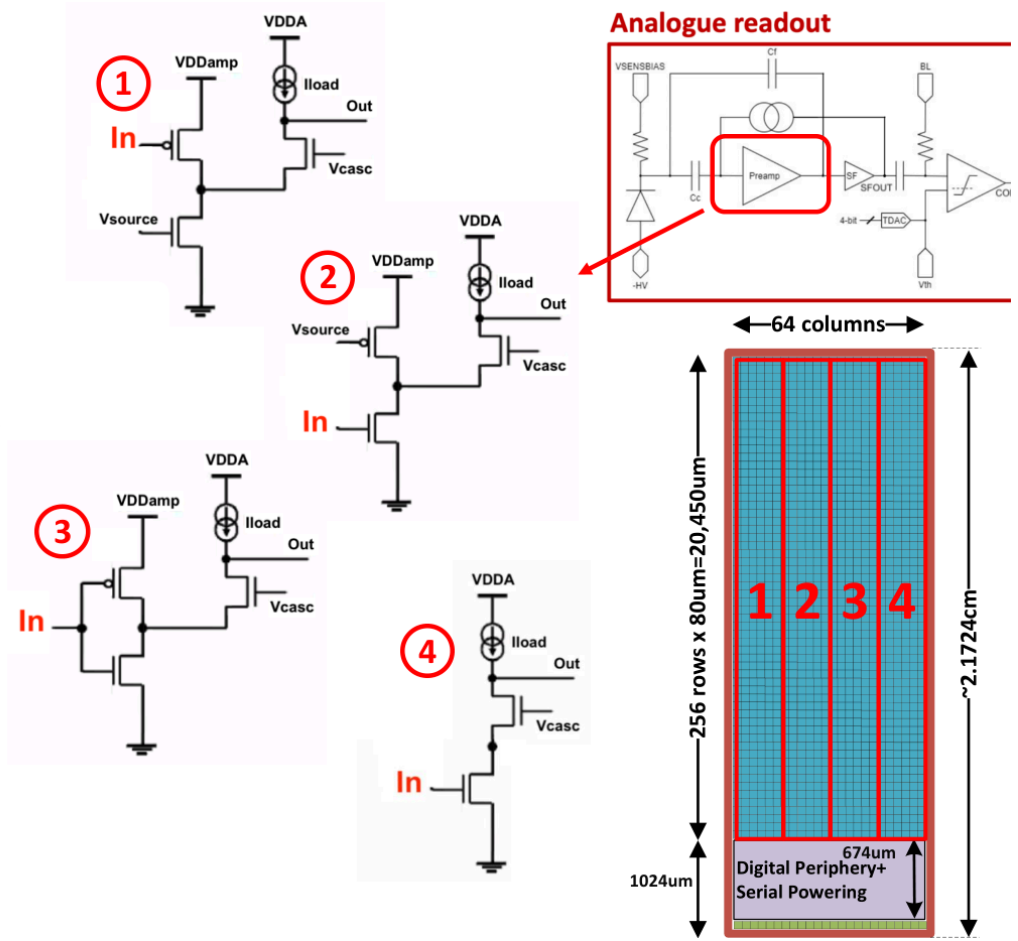
WP4 - System verification and integration



RadPix: Pixel Matrix

C. Zhang

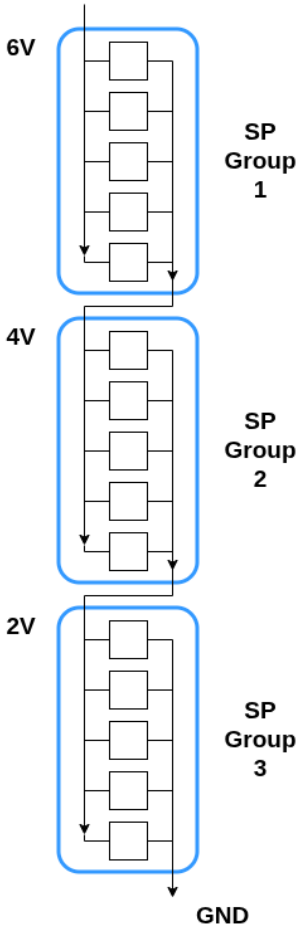
- **Pixel** = $80\mu m \times 80\mu m$
- **Analog**: Charge Sensitive Amplifier (CSA) - 4 flavours
  1. PMOS (based on RD50-MPW4)
  2. NMOS (based on Monopix)
  3. CMOS (based on Monopix)
  4. Trans-impedance amplifier
- All optimised for **99% in-time efficiency and $150mW \cdot cm^{-2}$ power**
- Simulation shows *rise-time*: 11-14ns, *time-walk*: $1.5ke^- - 15ke^-$
- **Digital** (not shown): adds timing and address info



RadPix: Serial Powering

S. Powell

- For reasons of space, power, and material budget, serial powering was chosen as preferred option for Mighty Tracker
- Shunt Low Drop Out (**SLDO**) Voltage regulator design
  - Shunt regulator - regulates current to the chip
  - LDO regulator - generates the voltage
- **Implications**
  - Each chip sits on a different ground
  - Data must be A/C coupled
  - Can cope with up to 3 failures per group
  - Critical component must be tested early and extensively
  - For RadPix1, the serial powering will be a separate ASIC wire-bonded to the main pixel chip



DAQ

K. Hennessy, S. Powell

- Planning
  - Two stage approach
  - MARS (small system) common readout for everything up to a module -> needed soon
  - MiniDAQ (larger optical readout system) designed for larger structures ; required for full readout with serial powering
- MARS hackathon (Nov 2025)
  - aims: to get more people involved
  - get the system ready for testing sites
- First MARS systems going out in the next couple of weeks

Concluding remarks

- We're starting to make hybrids and modules
- We're building on a great foundation with the experts from the ATLAS build
- We're making RadPix v1
  - Great progress in the last year
  - Almost ready to submit
  - just had submission readiness review on Monday

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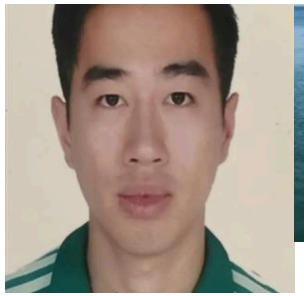
- We're making RadPix v1
  - Great progress in the last year
  - Almost ready to submit
  - just had submission readiness review on Monday
  - Sadly we're losing one of our star designers - **Chenfan**
    - A huge contribution is encapsulated in an 80×80µm pixel 🤦
    - We wish him the best for his future career in China 🎉



All the power of internet data leaks and these are best images I could find 🤦

No Questions

- I am appalled at how the University is treating our staff
  - **Angie and Hannah** are an essential part of our group
  - The manage our inescapable chaos and our “last minutedness” with professionalism and we put our trust in them

- I’m proud of our group. I am not proud to represent a university that treats people like commodities.
- What can we do to protect the people who have served us and our science?

Backup

Institutes

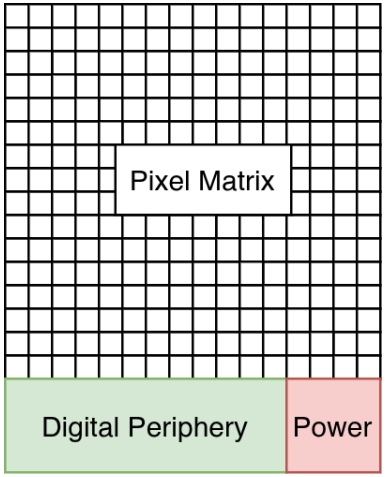
- Brazil: CBPF
- Chile: UNAB
- China: ?
- Costa Rica: CONARE
- Germany: Aachen, Bochum, Bonn, Dortmund, Fribourg, Heidelberg, KIT
- Lituanie: Vilnius
- Poland: AGH, CUT, HNI, IPJU
- Spain: Barcelona, Valencia
- Switzerland: Lausanne, Zürick
- UK: Cambridge, Edinburg, Glasgow, (Imperial), Liverpool, Manchester, RAL

Mighty-SciFi
Mighty-Pixel
Mighty-Tracker

Let's make a chip!

It needs to be :

- Radiation Hard
- Low Mass
- High Data Rate
- Low power consumption
- Low Cost



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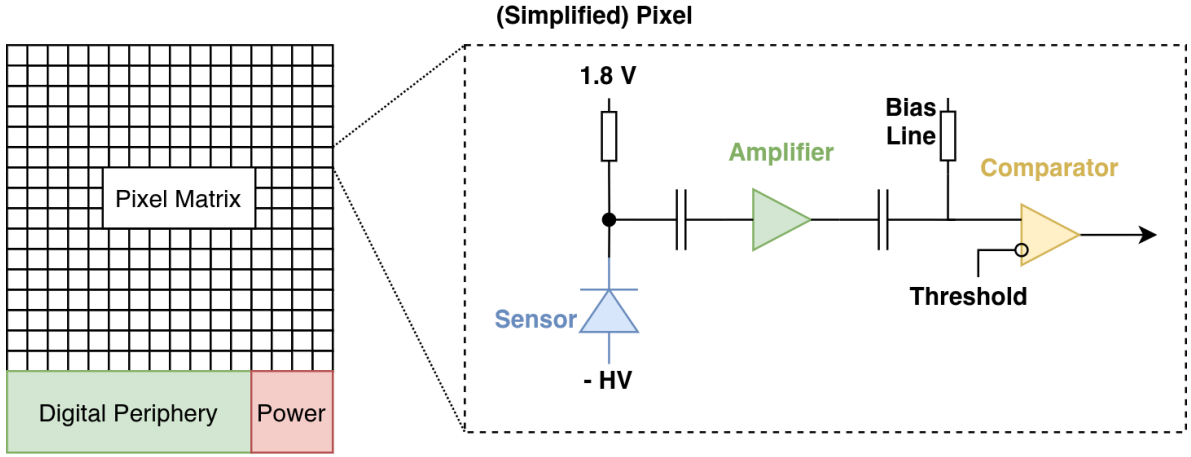

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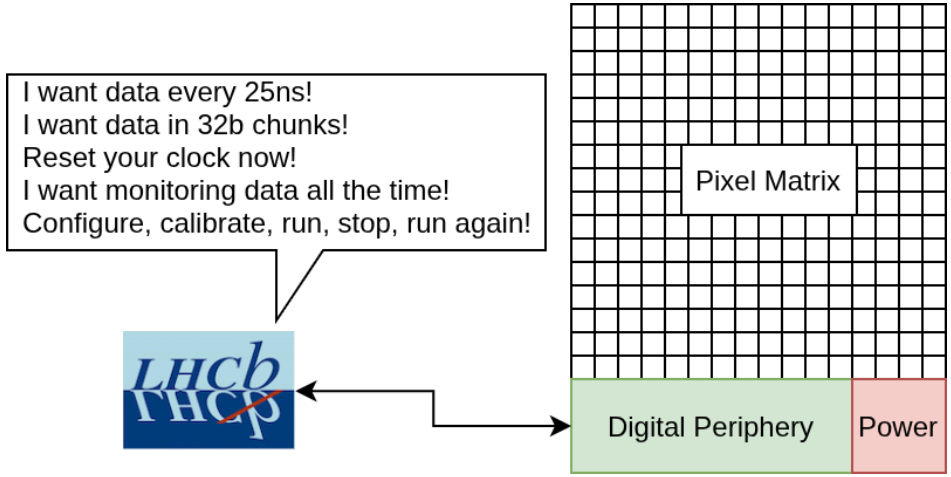
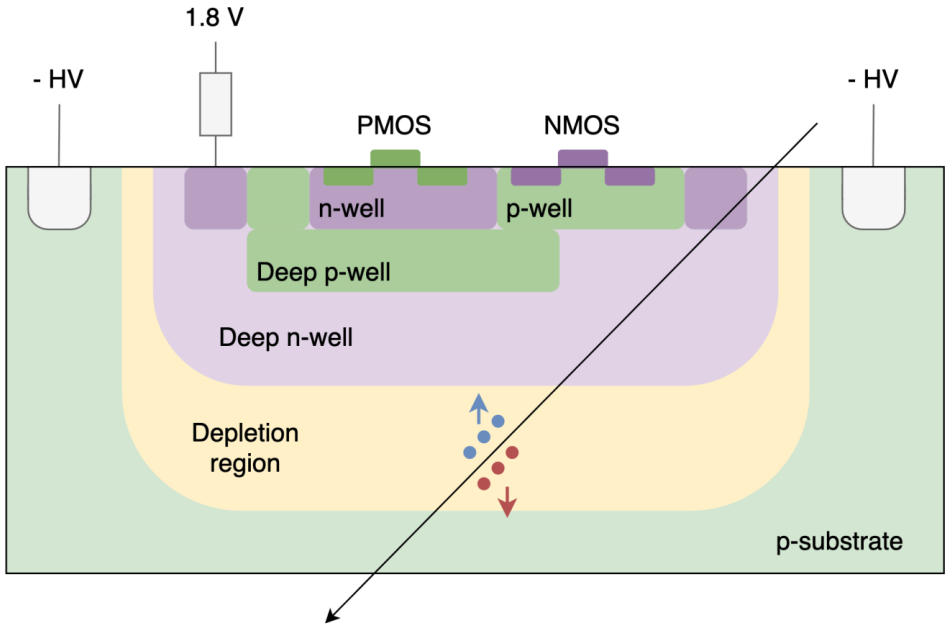


HV-CMOS

- Good candidate solution
- Sensor and readout chip in one



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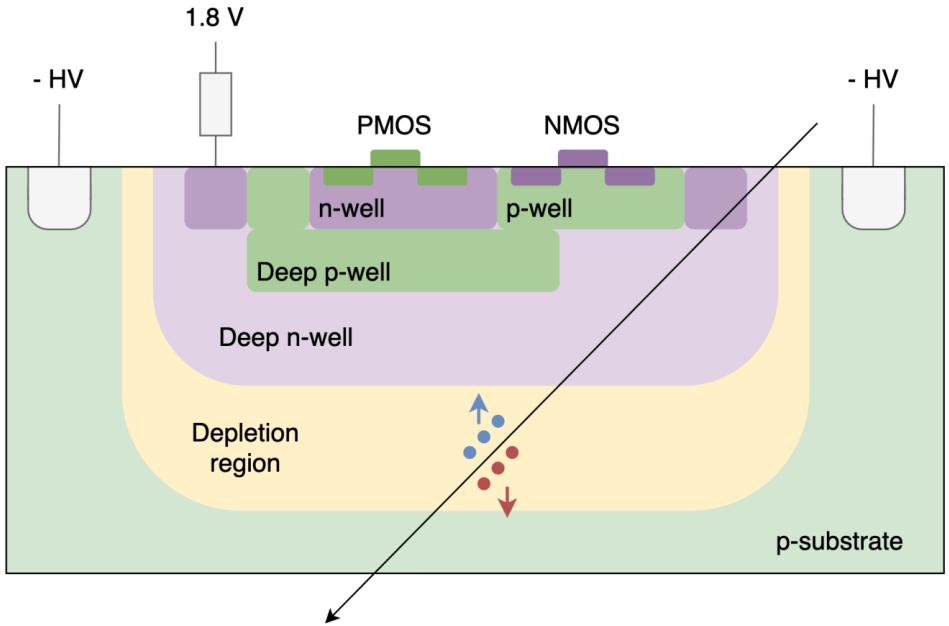
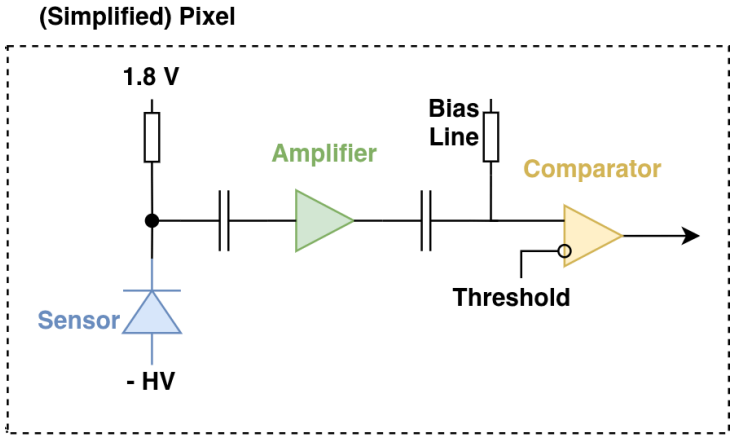
  ⇒ **low mass, low cost**, easier assembly





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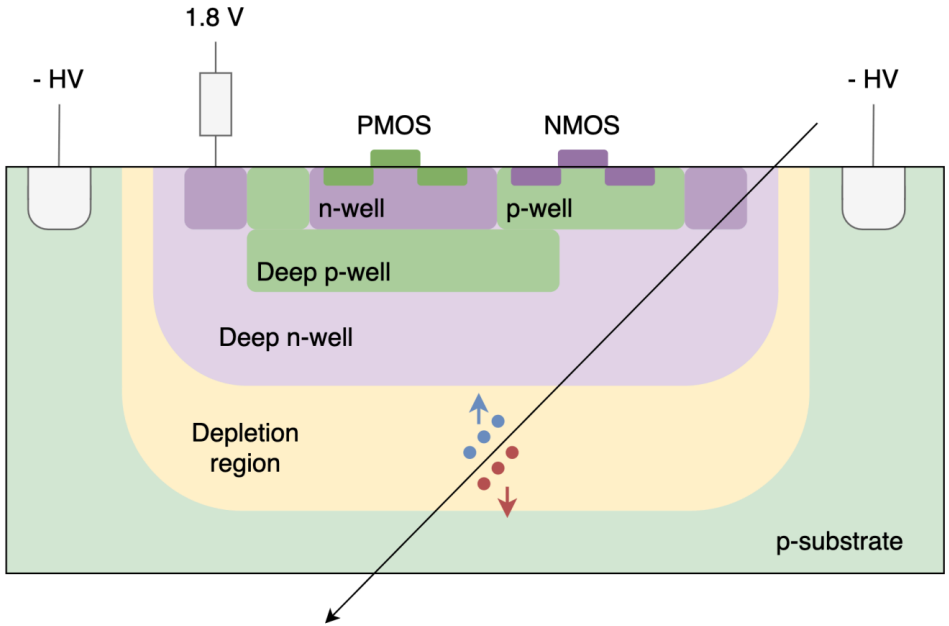
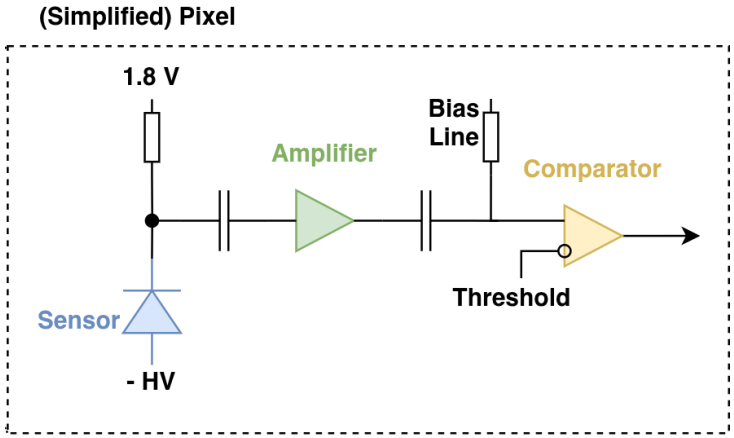


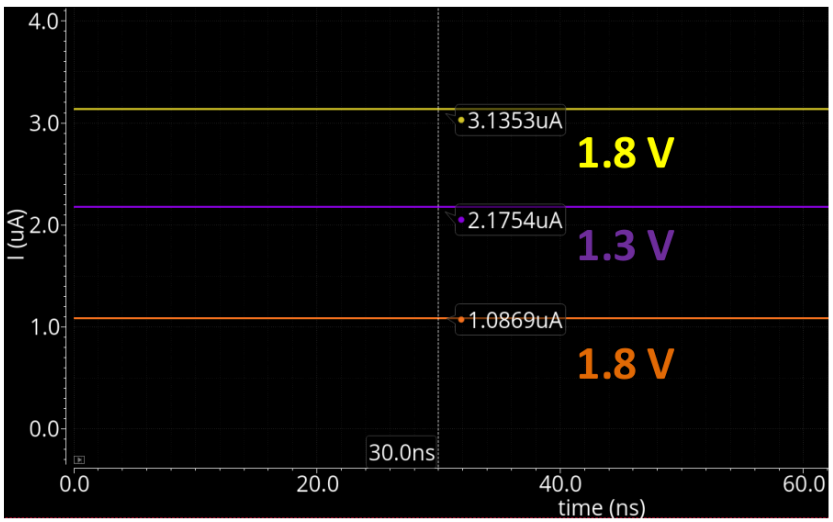
RD50 collaboration studies

"Radiation hard semiconductor devices for very high luminosity colliders"

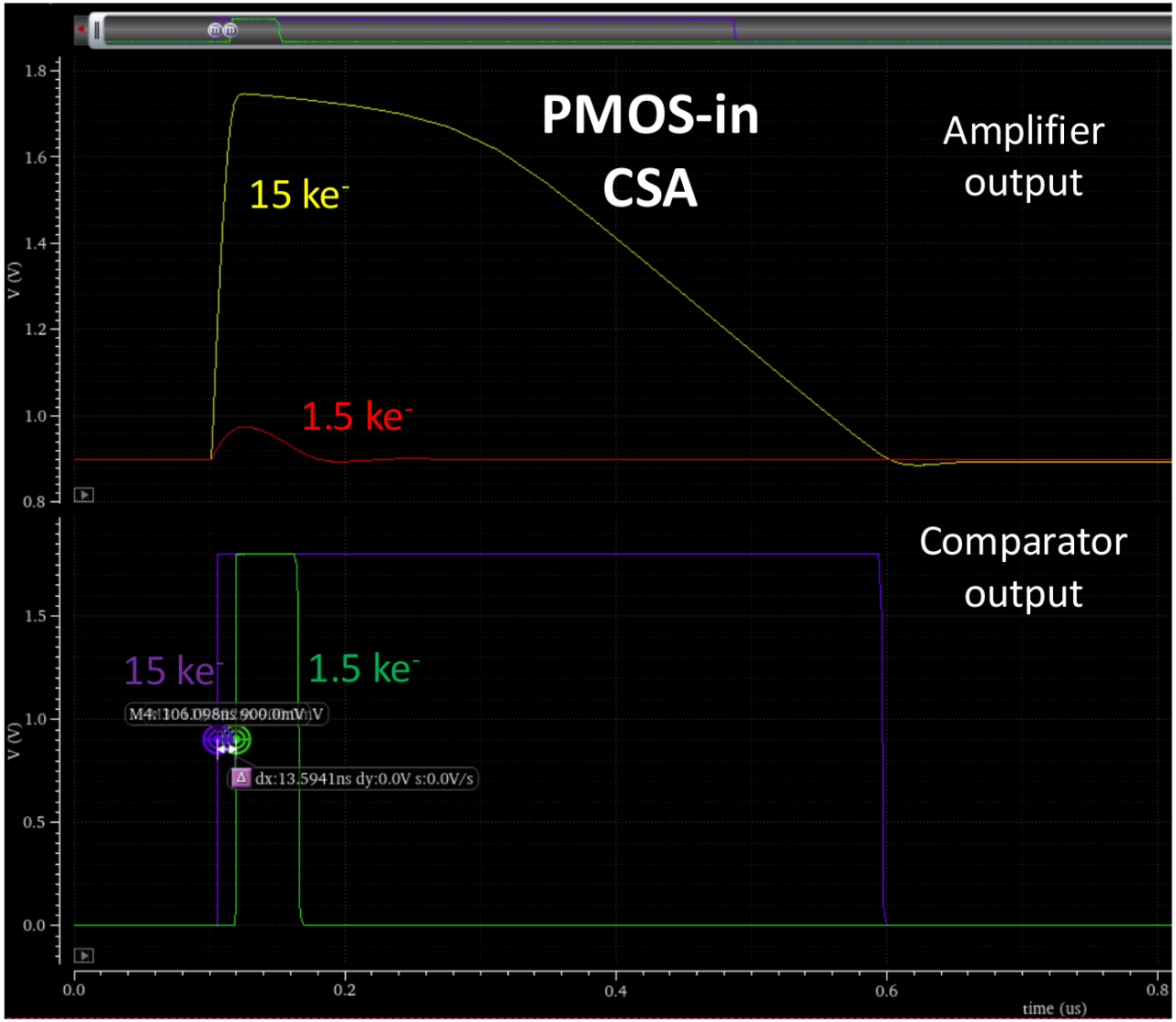


WP1 - Pixel matrix

- All pixel flavours:
  - ~ 10 µW/pixel -> ~ 150 mW/cm^2



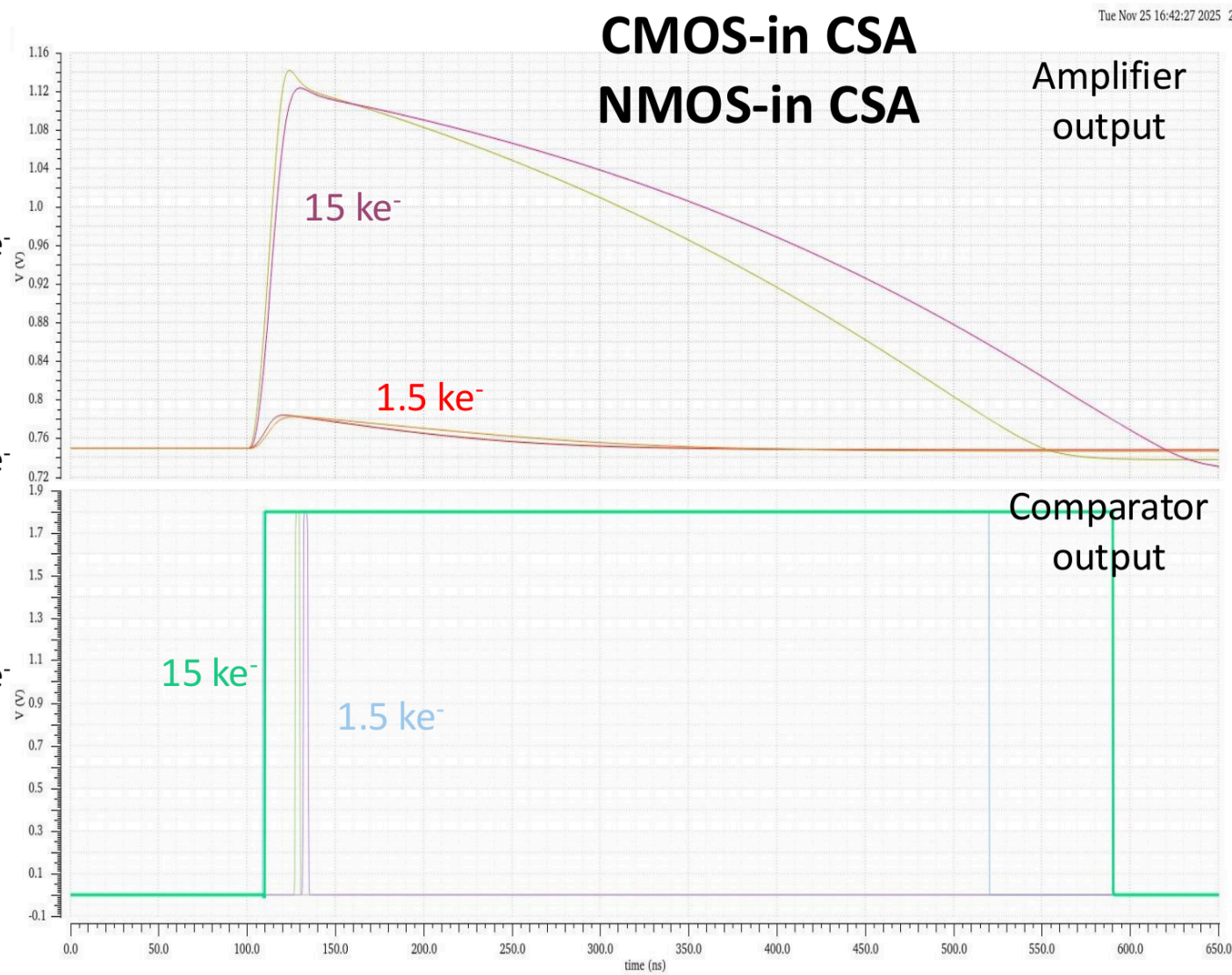
1. Pixel with **PMOS-in CSA**:
   - Rise time: 11 ns
   - Time walk between 1.5 ke$^-$ and 15 ke$^-$ input signals: 13.6 ns (Vth -> 5 x ENC)



WP1 - Pixel matrix

2. Pixel with **NMOS-in CSA**:
   - Rise time: 13 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals: 21.8 ns (Vth -> 1.5 ke⁻)
3. Pixel with **CMOS-in CSA**:
   - Rise time: 11 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals 18.5 ns (Vth -> 1.5 ke⁻)
4. Pixel with **Trans-impedance amplifier**:
   - Rise time: 12 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals: 8 ns (Vth -> 5 x ENC)

- **Status:**
  - pixel schematic & simulations **Done**
  - pixel layout & extraction **Finishing**



DAQ development and evaluation plan

- Use **MARS** as the DAQ system to maximise compatibility between institutes

- **Lab measurements**
  - I-V curves, with controlled temperature
  - Standalone chip block performance against chip specifications
    - Pixel matrix with test pulses and with radioactive sources (analogue output, S-curves, in-pixel trimming DAC optimisation)
    - Chip periphery functionality (TFC, LVDS at required speed)
    - Voltage regulators (as a function of temperature, VDD and process variations)
  - Full chip (pixel matrix + digital periphery powered with voltage regulators)
    - Time resolution (with scintillator setup)
    - Power consumption
    - Hit rate
  - Serial powering with > 1 RadPix chip

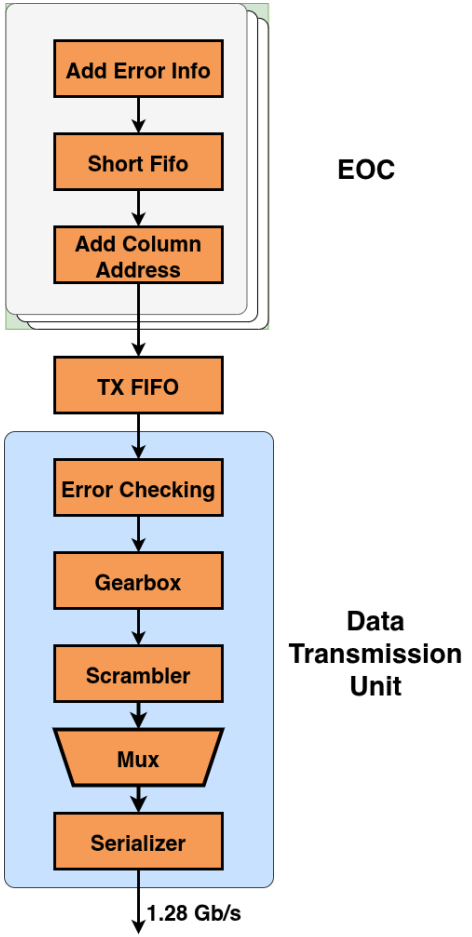
Chip thickness [µm]	100, 200
NIEL [n_{eq}/cm^2] at Ljubljana	Several steps until 4E15
TID [Mrad] at Oxford or RAL	Several steps until 250 MRad

- **Irradiation studies and test beam evaluation**
  - NIEL, TID, SEEs and test beams (efficiency, time resolution as a function of HV, comparator threshold…)

- **Multi-chip operation (*e.g.* RadPix on on-module hybrids/flexes)**

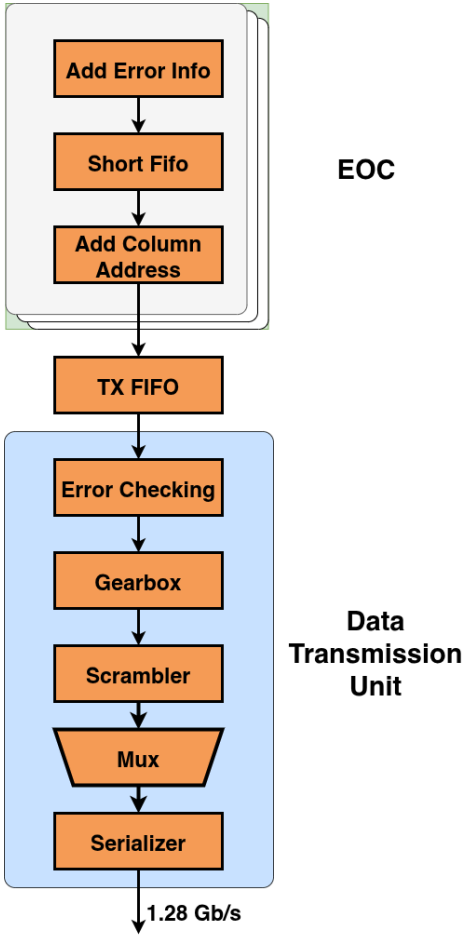
2. Digital Periphery

- **End-of-Column (EOC) logic**
  - add error info
  - buffer
  - add column address info
  - driven by a state machine
- **Data transmission unit**
  - prepare data for transmission in 32b chunks
  - scramble data for DC balancing
  - add header
  - serialise and send out: up to 1.28 Gb/s
- Verification: unit and system tests



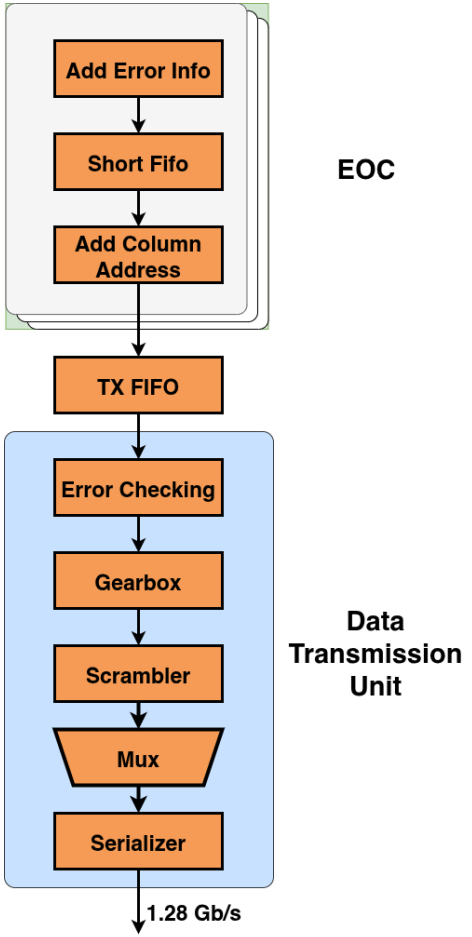
2. Digital Periphery

- **High data rate?** - RadPix1 data transmission is designed for fidelity first. Once we know we have good data from the matrix, we will optimise the data formats.



2. Digital Periphery

- **High data rate?** - RadPix1 data transmission is designed for fidelity first. Once we know we have good data from the matrix, we will optimise the data formats.
- **LHCb compatible?**
  - Slow Controls will be I2C for first version (too slow for final system)
  - TFC (Timing and Fast Control) are shared with other systems (well tested)



How does our chip fare?

It needs to be :

- Radiation Hard
  - RD50-MPW4 matrix
  - new digital components to be tested
- Low Mass - by design
- High Data Rate - RadPix2
- Low power consumption - in design but needs measurement
- Low Cost - by design