# Mighty-Tracker R&D Status at Liverpool: chips, flexes, modules and DAQ

S. Powell

University of Liverpool

# Overview

# RadPix1 design objectives

**Main objectives of RadPix1**

**1- Meet power density:**

- **Power optimization of the pixel (150 mW/cm²)**, while keeping 99% in-time efficiency within 25ns.

**2- Meet 95% of sensitive area on the full sensor scale:**

- Careful floor planning of the pixel array and the periphery circuits (Digital Readout + Serial Powering)

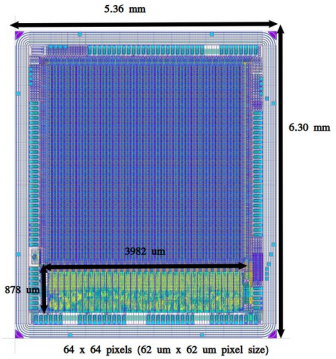
**3- Upgrade the digital periphery:**

- **Align to LHCb communication protocols**.
- Follow a sensible approach to reduce power consumption.
- Follow a sensible radiation tolerance design strategy.

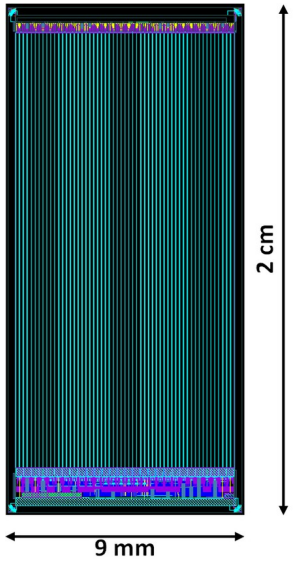
**4- Porting and developing necessary IPs:**

- Serial powering, LVDS drivers and receivers, Power-on-Reset.

RD50-MPW4

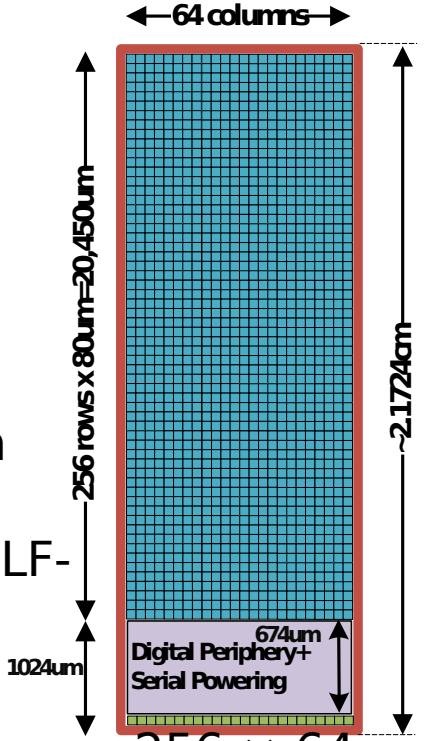



LF-Monopix




Based on RD50-MPW4 & LF-Monopix

RadPix1




256 × 64 pixels

(80 µm × 80 µm)

# Top level block diagram

**The RadPix sensor design is divided into a four work packages:**

**WP1) Pixel Matrix:**

- Optimisation of the Pixel array size and power consumption.

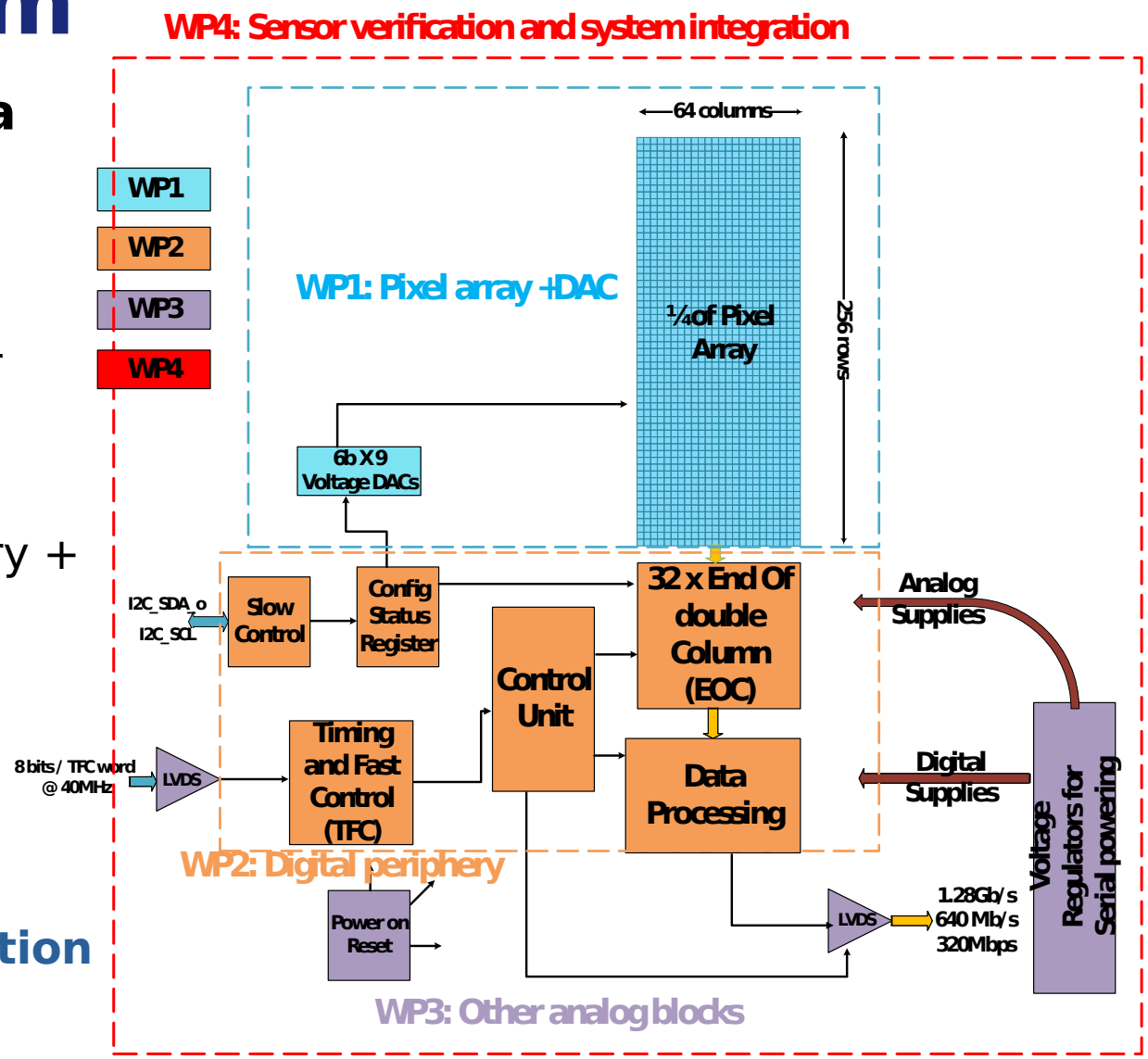
**WP2) Readout Periphery**

- RTL description of the digital readout periphery + P&R

**WP3) Other needed analogue blocks**

- Design of Shunt LDOs for serial powering
- LVDS transmitter and receiver
- Power On Reset

**WP4) Sensor verification and top-level integration**



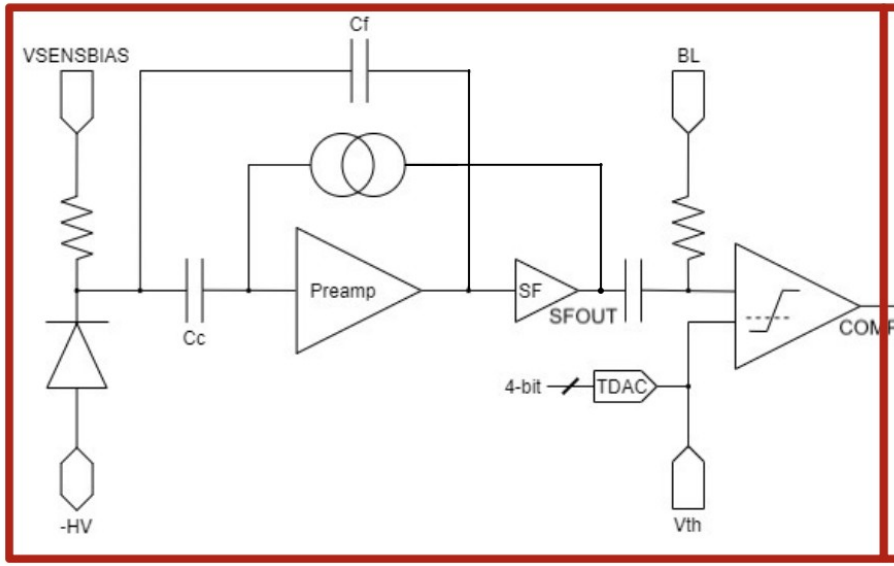
# Pixel Array Design

# WP1 - Pixel matrix

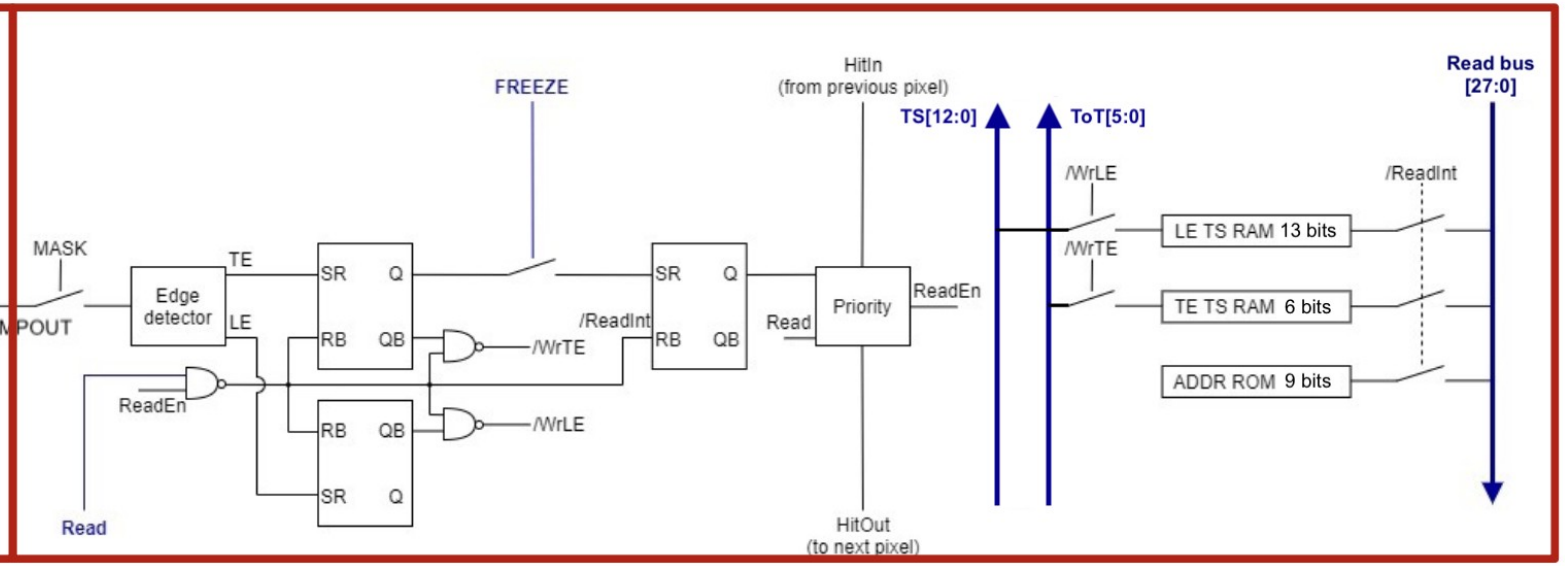
- **Pixel size 80 µm × 80 µm, Matrix size 256 rows × 64 columns (¼ of full size)**
- Each pixel includes
  - **Analogue readout**:
    - **Charge Sensitive Amplifier (CSA)**
    - Discriminator with a 4-bit trim-DAC for threshold tuning
  - **Digital readout**:
    - **Column-drain readout**
    - ToA @ 40 MHz, ToT @ 20 MHz

| | ToA | ToT | Address | Total |
|---|---|---|---|---|
| **# bits** | 12+1 | 5 | 9+5 | 32 |

**Analogue readout**



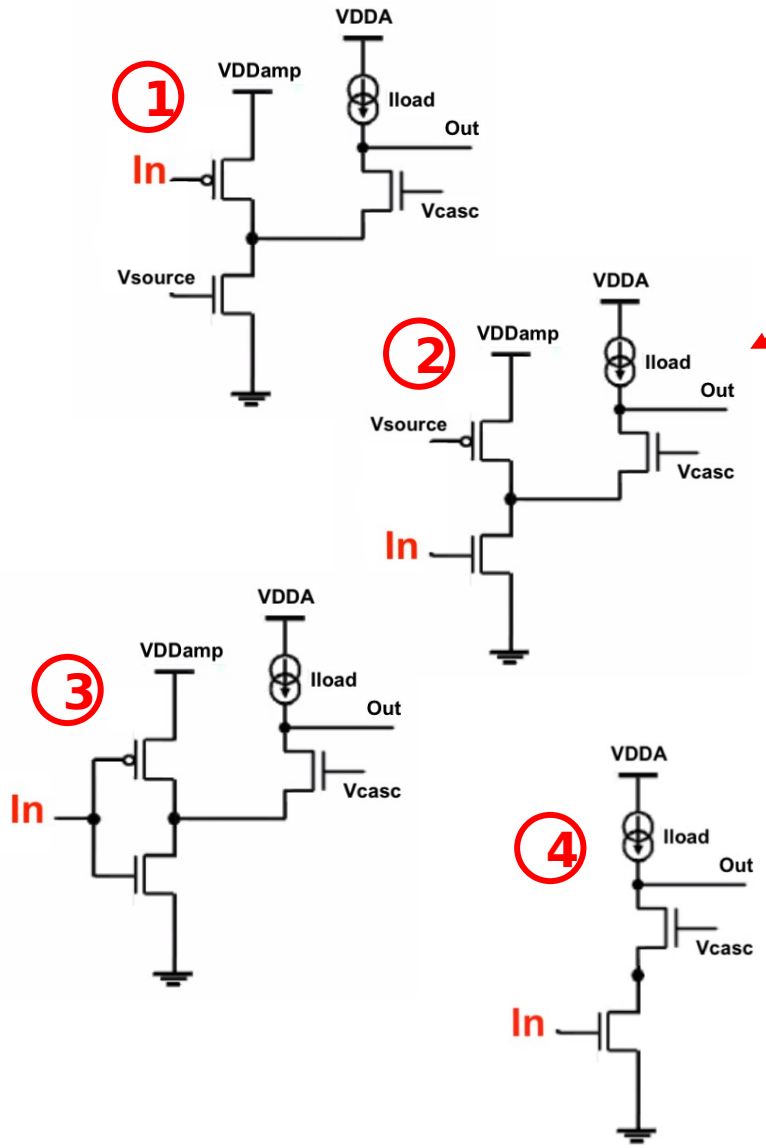

**Digital readout**

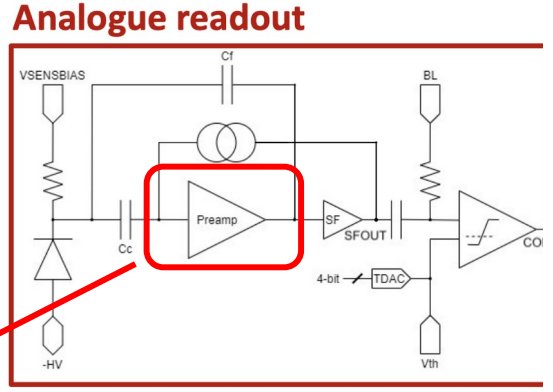


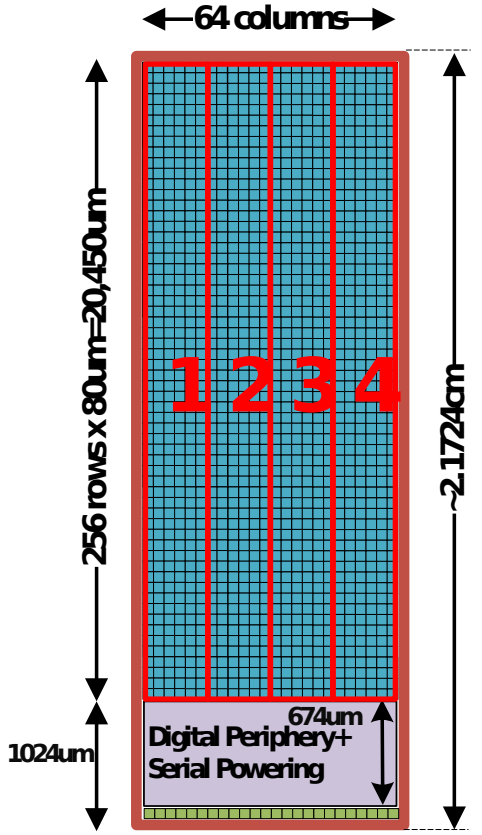
# WP1 - Pixel matrix

- Four Pixel flavours with different analogue front-end:
  1. **PMOS-in CSA**
     - based on RD50-MPW4 pixel
  2. **NMOS-in CSA**
     - based on Monopix pixel, higher gain and higher noise.
  3. **CMOS-in CSA**
     - self-biased, from Monopix, faster rising edge
  4. **Trans-impedance amplifier**
     - no need of feedback cap Cf, faster speed

- All pixel flavours are optimised to meet
  - 150 mW/cm$^2$ power consumption;
  - 99% in-time efficiency.

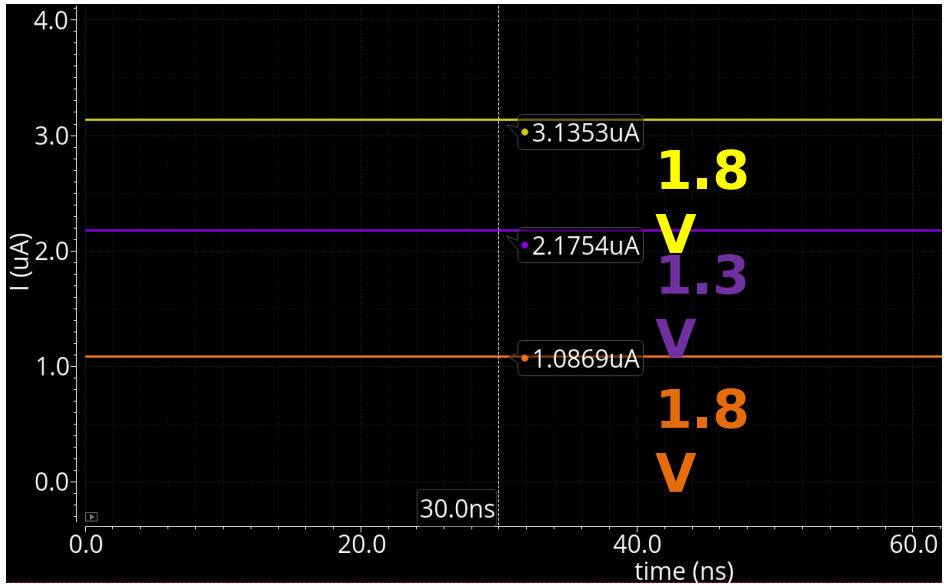


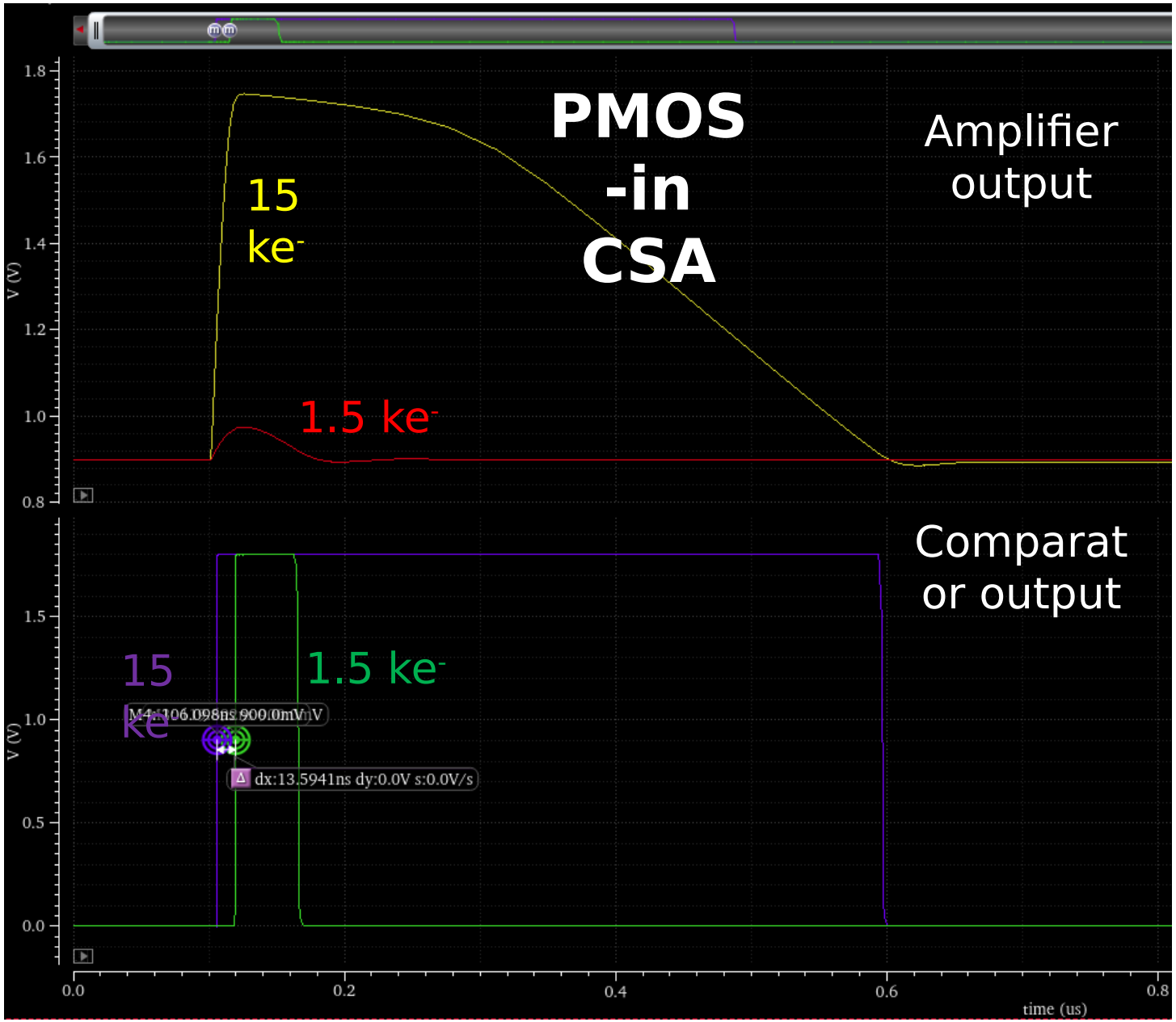



# Pixel matrix

- All pixel flavours:
  - ~ 10 µW/pixel -> ~ 150 mW/cm²

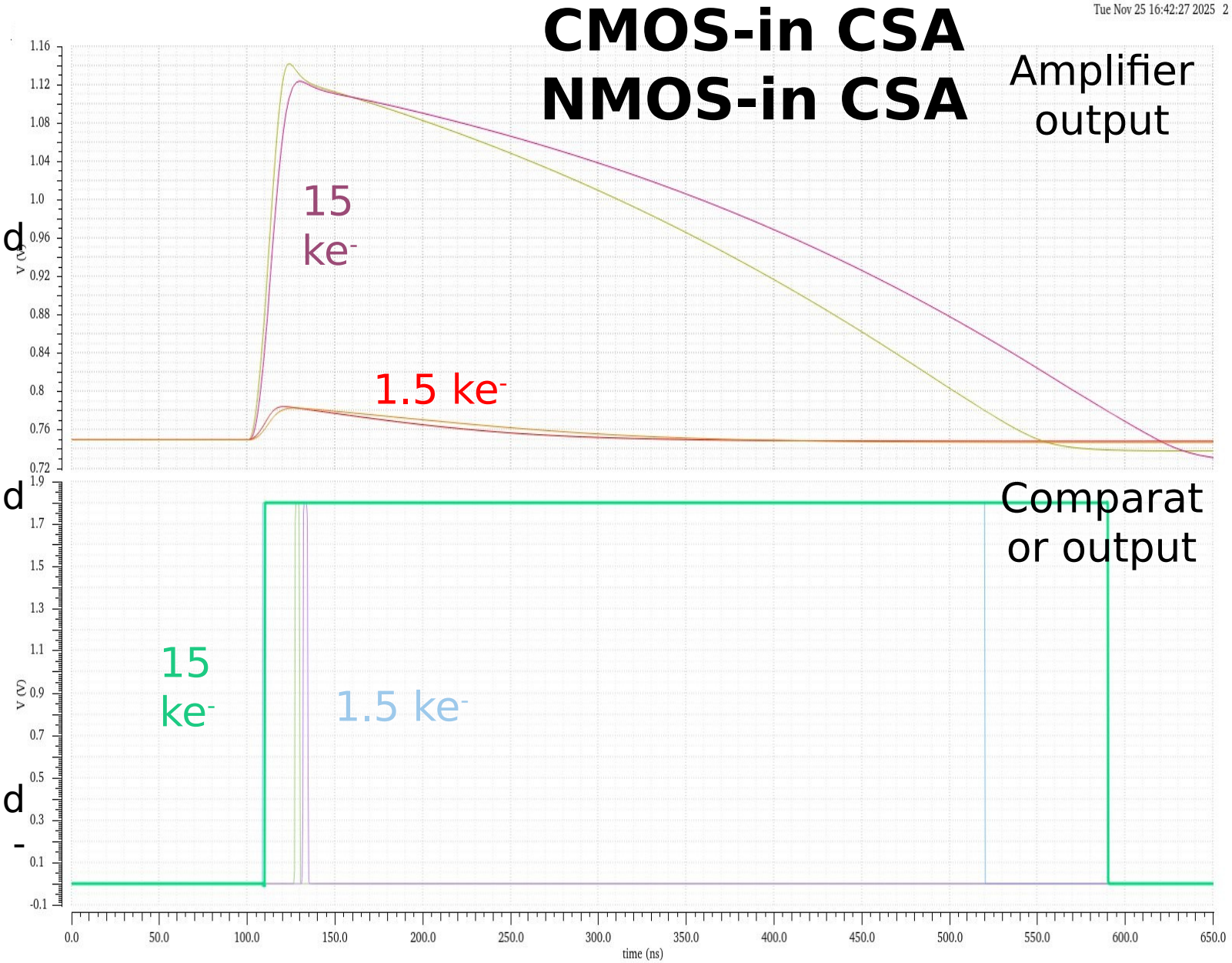



1. Pixel with **PMOS-in CSA**:
   - Rise time: 11 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals: 13.6 ns (Vth -> 5 x ENC)



# Pixel matrix

2. Pixel with **NMOS-in CSA**:
   - Rise time: 13 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals: 21.8 ns (Vth -> 1.5 ke⁻)
3. Pixel with **CMOS-in CSA**:
   - Rise time: 11 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals 18.5 ns (Vth -> 1.5 ke⁻)
4. Pixel with **Trans-impedance amplifier**:
   - Rise time: 12 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals: 8 ns (Vth -> 5 x ENC)



# Digital Readout design

# Digital periphery

- **Status:**

I. Verilog design **Done**

II. Block Verification: **Done**

**1) Digital periphery configuration with slow control**

**2) TFC operations**

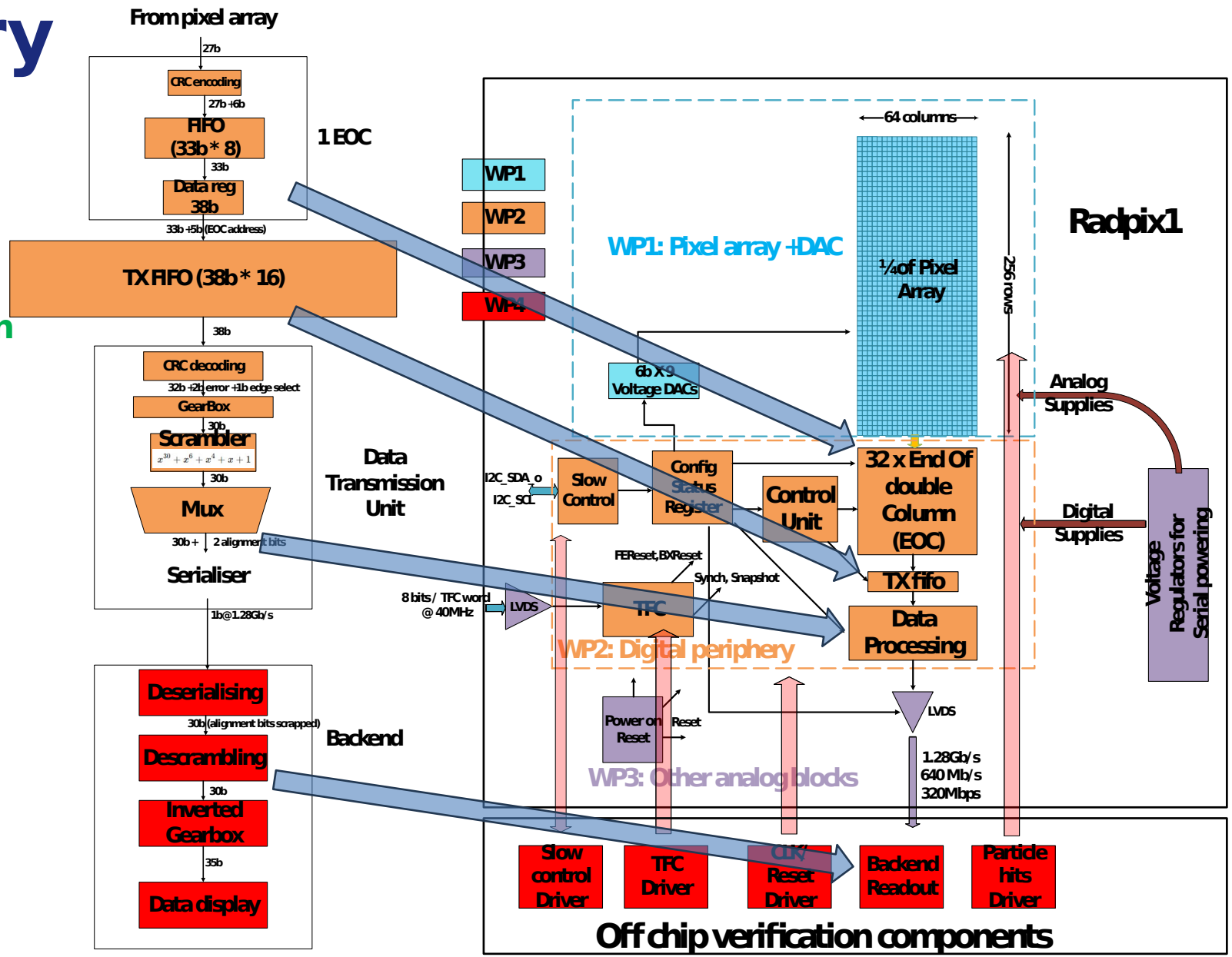
**3) Hit injection in pixel array**

**4) Data path from pixel array to backend.**

III. Integration: **Done**

**6) Synthesis and Place & Route**

**7) Top level virtuoso integration**



# Serial Powering

# WP3 - Serial powering

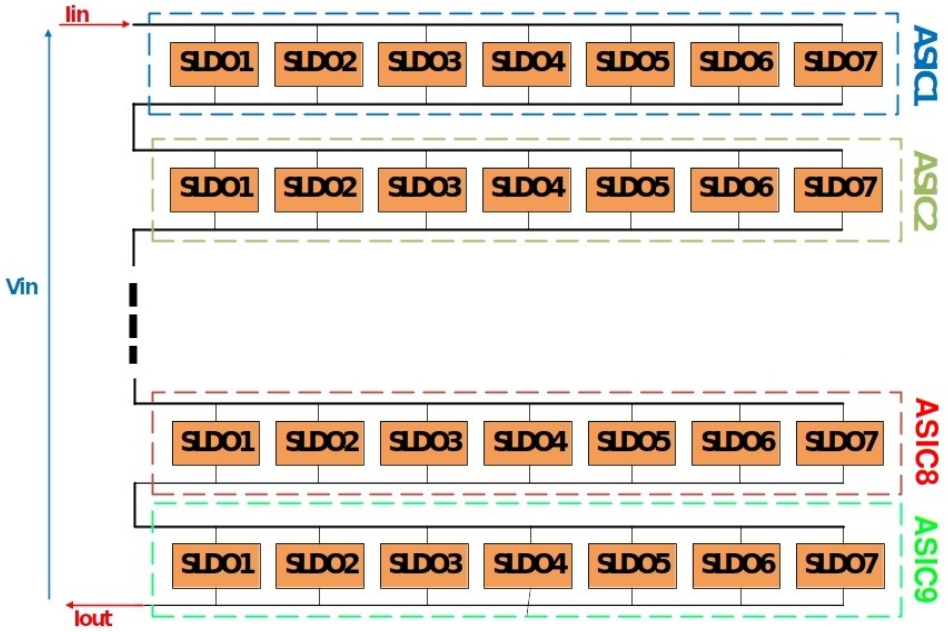
- **9 ASICs per serial grouping and 5 groups in parallel**

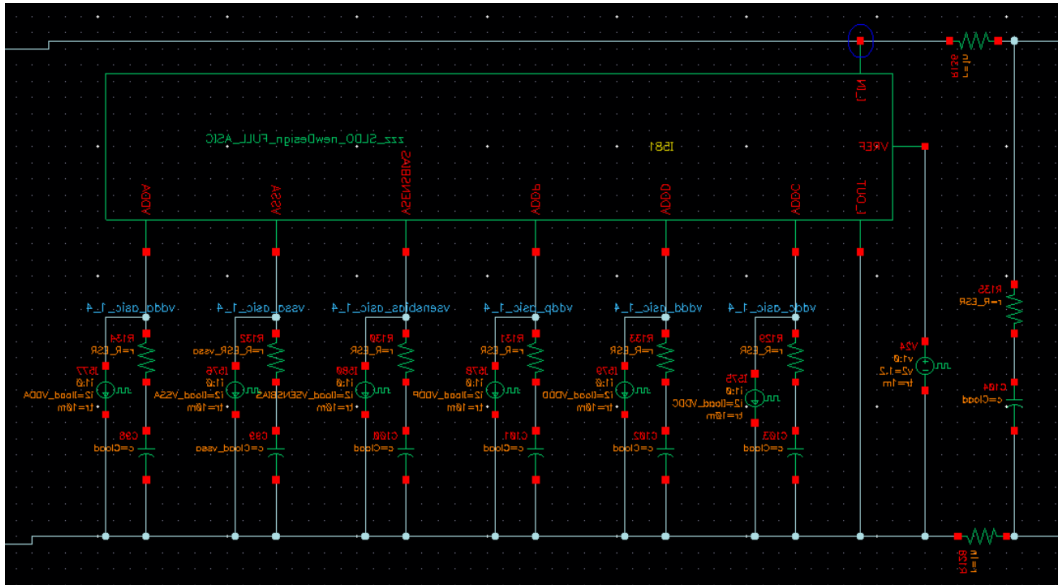
- **6 x SLDOs per ASIC**:

SLDO1: VDDD =>1.8V
SLDO2: VDDC =>1.8V
SLDO3: VDDP =>1.8V
SLDO4: VDDA =>1.8V
SLOD5:VNSENSBIAS =>1.8V
SLDO6: VSSA =>1.3V

§ Based on proven voltage regulators designs in chips beyond LHCb (**ATLAS, FEI…**)

§ Reference voltage **$V_{ref}$ provided by a bandgap** with DAC to adjust $V_{out}$



# WP3 - Serial powering

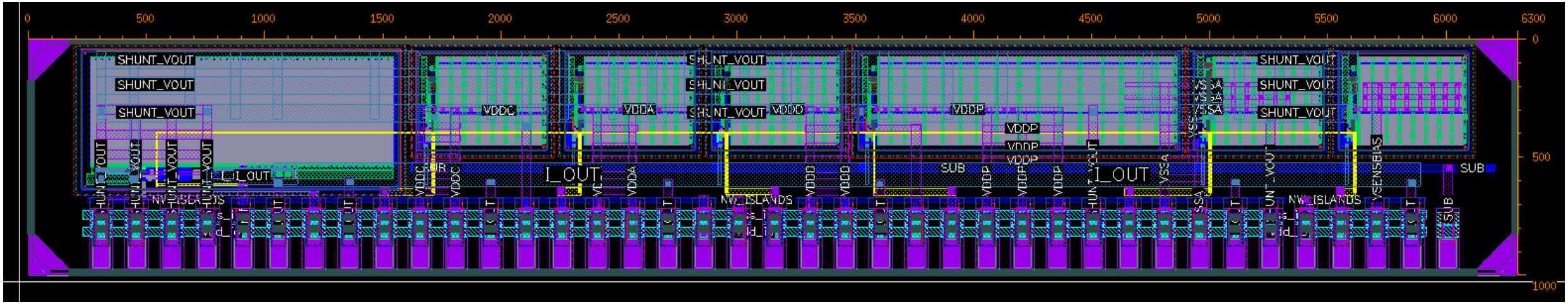
**Status**:

- Each SLDO provides **output currents from 40 up to 250mA (depending on which power domain)**

- Each SLDO chip includes **1 shunt** regulator **followed by 6 LDOs** for the various power domains (sized according to expected current consumption)

- Simulations include –
  - **Transient** startup (for full serial chain of 9 ASICs and parallel combination)
  - DC **voltage drops** from **post layout** extraction
  - **AC stability**
  - **Monte-carlo yield** simulations
  - Bondwire and **trace resistance** simulations.

- SLDO chip submitted in August 2026



# DAQ evaluation plan

# DAQ development and evaluation plan

- Use **MARS** as the DAQ system to maximise compatibility between institutes

- **Lab measurements**
  - **I-V curves**, with controlled temperature
  - Standalone chip block performance against chip specifications
    - Pixel matrix with **test pulses** and with **radioactive sources** (analogue output, S-curves, in-pixel trimming DAC optimisation)
    - Chip periphery functionality (TFC, LVDS at required speed)
    - Voltage **regulators** (as a **function of temperature, VDD** and process variations)
  - Full chip (pixel matrix + digital periphery powered with voltage regulators)
    - **Time resolution** (with scintillator setup)
    - **Power consumption**
    - **Hit rate**
  - Serial powering with > 1 RadPix chip

- **Irradiation studies and test beam evaluation**
  - **NIEL, TID, SEEs and test beams**
  - (efficiency, time resolution as a function
  - of HV, comparator threshold…)

| | |
|---|---|
| **Chip thickness [µm]** | 100, 200 |
| **NIEL [$n_{eq}$/cm²] at Ljubljana** | Several steps until 4E15 |
| **TID [Mrad] at Oxford or RAL** | Several steps until 250 MRad |

- **Multi-chip operation (*e.g.* RadPix on on-module hybrids/flexes)**

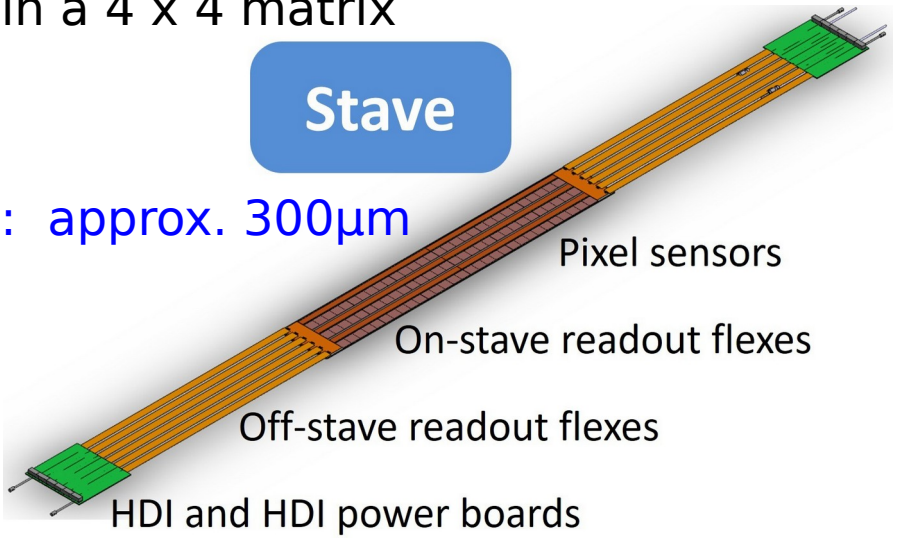
# Hybrid design and flex assembly

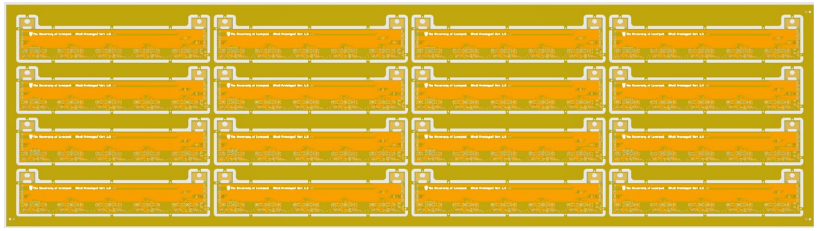
# Hybrid Flex for Full Size Mock-up - Status

- Circuits readied for manufacture and part (SMD) assembly
  - Targeting 160 circuits – aligned to MPix2
- Panelised to facilitate their assembly – 16 circuits per panel in a 4 x 4 matrix
  - 10 panels total

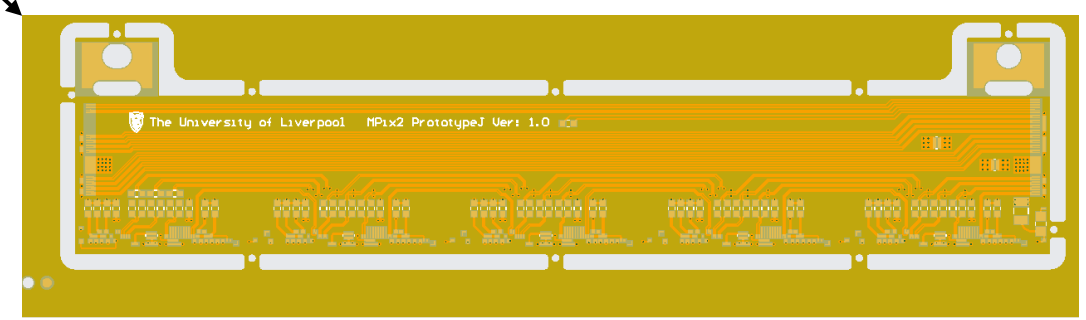
- Stack-up utilises 25µm Polyimide dielectrics, Build thickness:  approx. 300µm
  - 3 Cu-layers, Designed for $Z_{DIFF}$ of 100Ω excluding loading

- Circuits received at Liverpool



Panel of 16 circuits

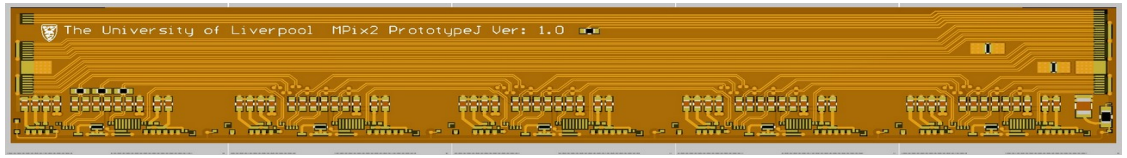



Single circuit detail

# Hybrids at Liverpool

**Q4 2025/Q1 2026**

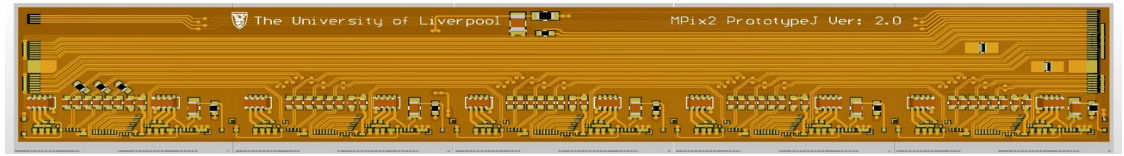
- First MightyPix2 **flexes for mechanical assemblies** for the checking out of tooling  become available
  - Come with realistic Bond pad fields and SMD part attachment



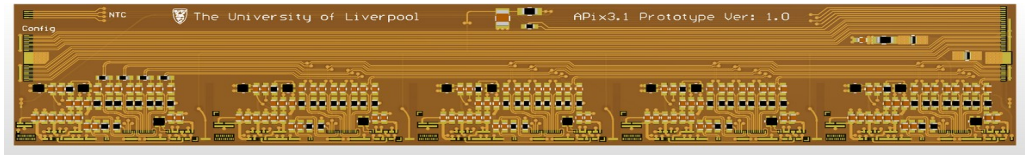

- **Stave Data Readout Flexes become available**, ports O/P data from MightyPix to Stave PP0 (patch panel zero) region for relay onto HDI boards

**2026 - ongoing**

- Full MightyPix2 electrical flex - **Preliminary layout** completed utilises full MightyPixel readout architecture
  - **Expect submission after successful testing of MPix2 Q4 2026/Q1 2027**



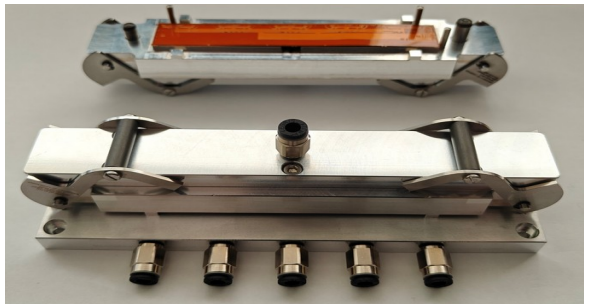

- **New Flex design for evaluation of Serial Powering** using existing AtlasPix3.1 chips – under manufacture
  - Adopted MightyPixel readout architecture with 5 x AtlasPix3.1 per flex - hooks up to existing Stave Data Readout flexes
  - Allowing full evaluation of a Stave Part Column assembly composed of 3 modules



# Flex Assembly at Liverpool

- Will make use of MPix2 Mechanical Flexes for assembly prototyping
  - Firstly, with non-SMD loaded flexes
  - Followed by SMD loaded flexes


- Using **Dummy chips provided by Manchester and Bonn**
- Tooling **designed in Liverpool** and **manufactured at Heidelberg** University
  - 2 sets of tooling being provided by Heidelberg – thank you

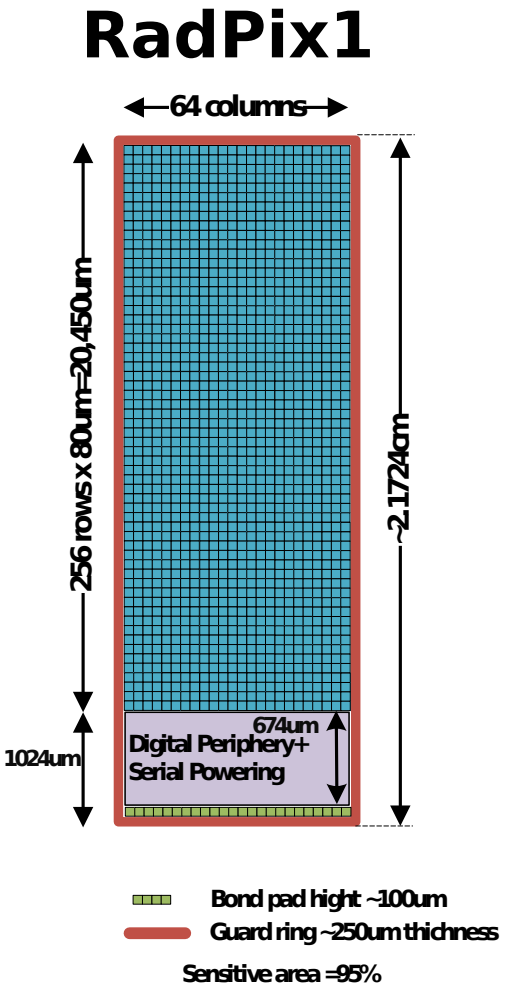


- Tooling is used to place flex on chips
- **Chip placement** is done by a precision **pick-and-place machine**
  - Amadyne catAP: Placement accuracy <0.008µm/3σ

- Dispensing of glue to flex can be done either
  - **Manually** using a stencil or by a **Glue robot** (Nordson EFD)

# Overview

- Optimisation of Pixel Matrix for power (150 mW/cm2) and speed (99% in-time efficiency) requirements with 4 different pixel flavours. **Meeting target.**
- Design of readout periphery for compatibility with LHCb protocols, and power budget. **Verilog blocks done, verification completed**
- Analogue blocks (LVDS transmitter & receiver, power-on-reset, voltage regulator for serial powering) **Ported to Lfoundry, Completed.**
- **LVDS Status: schematic, Corners simulations , layout & extraction completed**
- **Power on reset done**
- Design verification. **Established communication and configuration, slow control + high speed data out done. TFC verification done.**
- Development of ¼-size RadPix1 using LFoundry 150 nm has completed with the **final design submitted in August 2026 – SLDO chip also submitted in August 2026.**



# Development Plan