

LF 150 CERN/DRD3 run

Postprocessing/Dicing preparation

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Run status : timescale

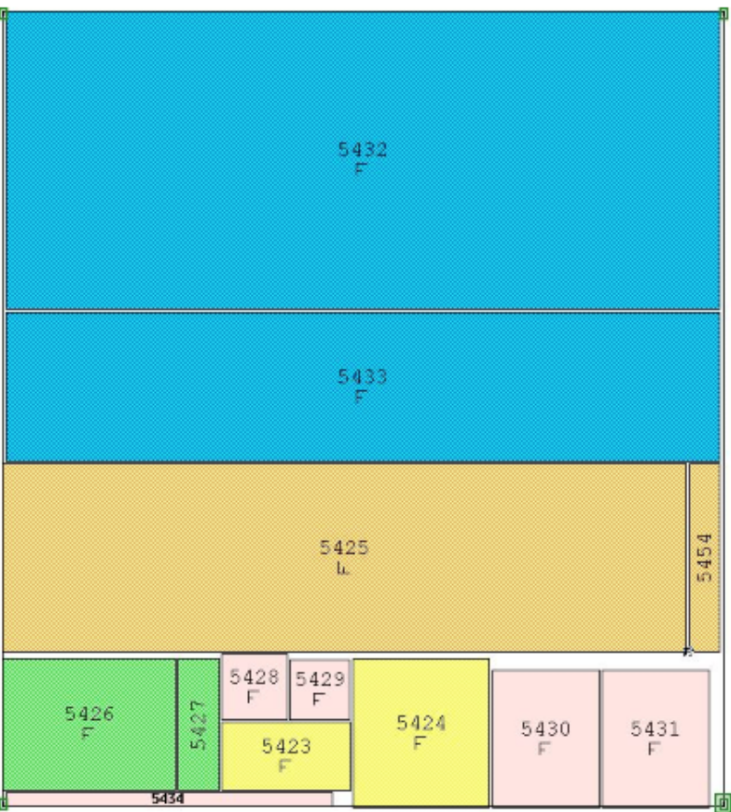
- Initial target was to have all BNs ready, DRC clean by end July, with some not precisely expressed tolerance for late comers...
- No hard stop was given by LF end July, allowed to continue iterating on design over summer
- LF started to push on us to finish beginning of September
- All BNs declared DRC clean on the 10th of September
- Masks fabricated end of September
- Wafer processing started 2nd October
- LFoundry aims at shipping finished wafers end of 2026

Reticle assembly

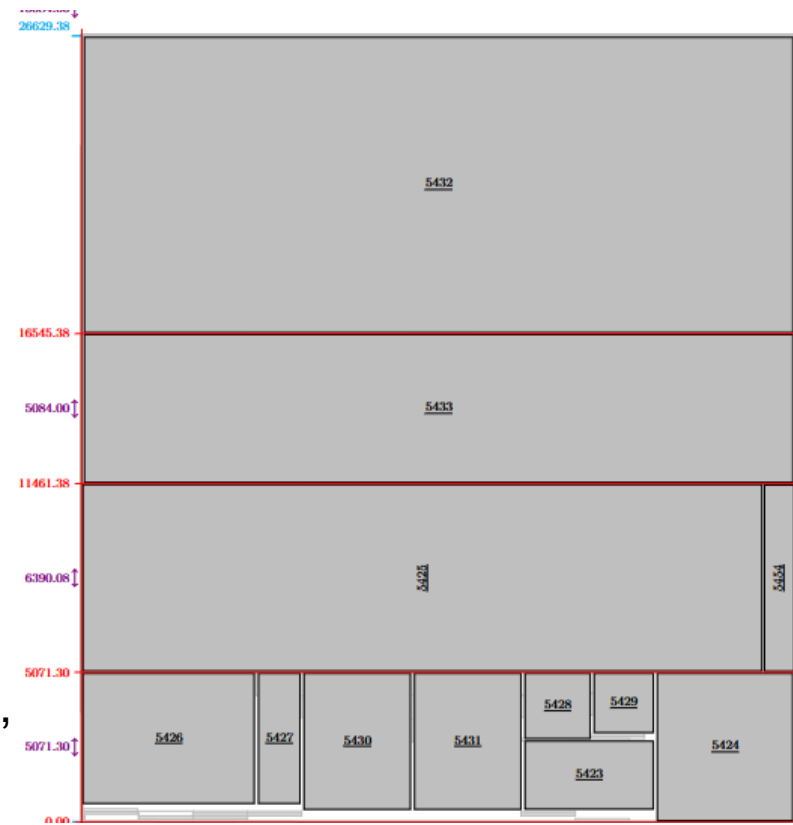
We tried to minimize the number of cuts by aligning as much as possible chips/groups of chips in the lower region

Had to flip Radpix1 to have its pads on the left (easily accessible) and minimize dicing conflicts with MiniCactus

This was discovered late, confirmed at the MEBES checking stage and implemented shortly before mask fabrication



LF initial proposal



Final implementation

Wafer map

waferMap Version 2.2.3			
Product	Y1E1	Description	
Fab	9	Scanner	ASML 5500/800
Wafer Dia.	200 mm	Edge Clr.	3.0 mm
Notch	Default	WL Parallel Ref.	Default

	X	Y
Die Size with Scribe (mm)	24.168	26.62938
Shift (mm)	0.0	0.6

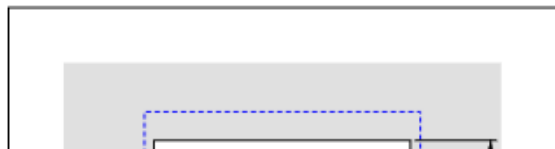
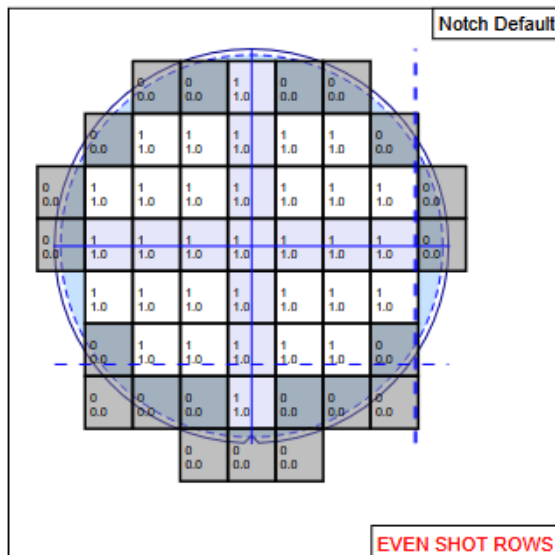
DPW & Shots	
Die Per Wafer	33.0
DPW on Yielding Shots	33.0
EFR Die (- corner)	3
Shots	54
Inner Shots	33
Partial Shots	0
Wafer Coverage Shots	54
Si Area Unused (mm ²)	1292.05
Si Area Unused (%)	4.11

Note we have 33 complete reticles per wafer

Some additional loss to be expected after PCM checks, will have to see back-end sheets when LF will communicate them to us

Reticle	
Die Per Reticle	1
Reticle Field Eff. (%)	77.3532
Lens Diameter (mm)	41.2300
Die Rotated	false
Forced DPR	true
Die Area (mm ²)	643.5789
Reticle Area (mm ²)	643.5789

	X	Y
Die Per Reticle	1	1
Step Size (mm)	24.168	26.62938
Step Maximum (mm)	26.0	32.0
Die Count +1: Die Size (mm)	13.0	16.0
Die Count +1: Delta (mm)	11.168	10.62938
Die Count +1: Eff. (%)	83.2168	92.9538



Wafer composition

Wfs Split	CZ >2kΩ·cm		Low res. Bulk Si / 30μm EPI, >3kΩ·cm		CZ 500-1100 Ω·cm	
	Si Type1		Si Type2		Si Type3	
	Main	Backup	Main	Backup	Main	Backup
Implant Set1	4		1	2	2	1
Implant Set2	4					
Implant Set3	3		1	2		
Total	11		2		2	

Main : 11 CZ 2k ohm cm, 2 epi 30 um, 2 CZ 500-1100 ohm cm

25 wafers produced in total, 15 main, 5 backup, 5 test. Backup wfrs can be purchased later, in case we need them. We were advised by LF to affect backup wafers to the less numerous types

Implant sets are relevant only for BN 5424/5423 (gain layer). Other BNs do not have these layers

Wafer reception and storage

- From Lfoundry's point of view, CERN is the owner of the wafers → they will be shipped there.
- Do we have identified medium term (months to years) storage space there ? Dry cabinet ?
- Will need also some handling capacity
(clean room to open boxes) to ship the wafers to different places

Known post-processing requirements

	RadPix1	Panther2	PS	BIG	TDC	GL-GR	GL-MiniCactusV2	LFPS2	X1	HV-Pix26	Monstera1
Post-processing (Y/N)	Y & N (one non-processed wafer for electrical tests)	Y	Y	Doesn't matter	N	Y (two HR wafers) N (one epi wafer)	Y (two HR wafers) N (one epi wafer)		Y		
If Y, what type	BS implant + met	BS implant + met	BS implant + met			BS implant + met	BS implant + met		BS implant + met		
Thickness [um]	150 200 (LHCb req.)	150-250 (or <150)	150-250 (or <150)	200 (ideal) >100,<300	No thinning	150 (one HR wafer) 200 (one HR wafer)	150 (one HR wafer) 200 (one HR wafer)		150		
# samples	>40*5	50	50	40	30-40	40*3	40*3		40*15		
TDC chips will be picked from whatever is available (TDC does not care about thinning or backside processing)											

LFPS 2 : 150u or 200u, postprocessing needed

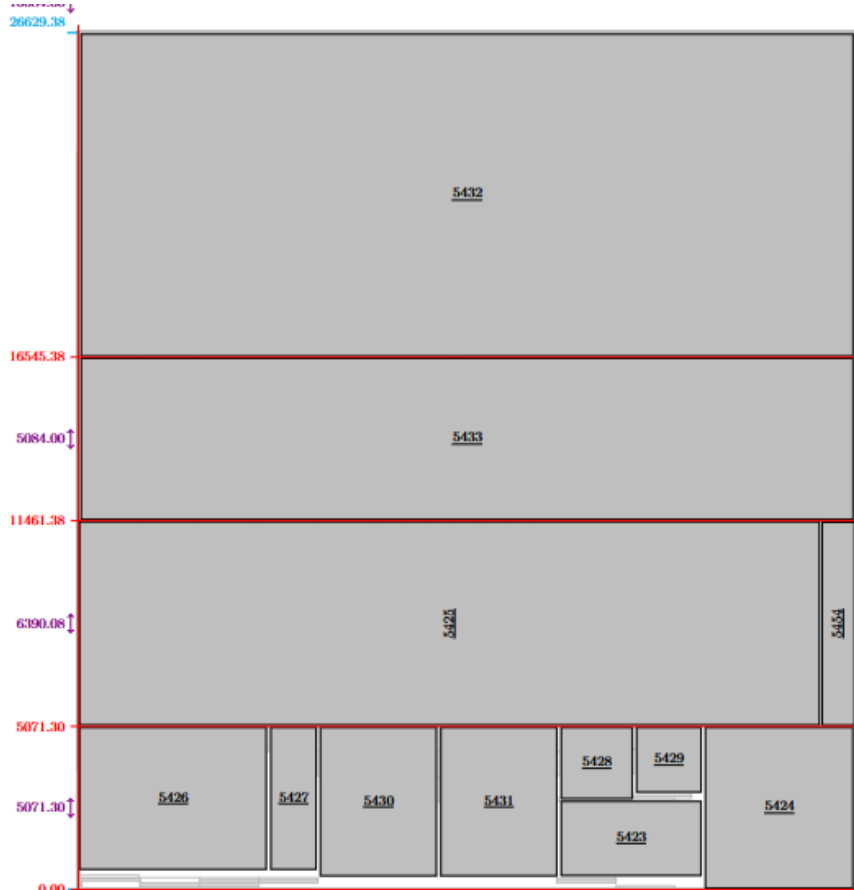
KIT : asked for a few wfrs not thinned, and will take in addition what is available from the thinned wfrs

Thicknesses required (smallest common denominators) : 100 u to 250 u ?

Zeroth-order proposal

- . CZ 500-1500 (2 wfrs) → could be handled by KIT (HV-Pix26, Monstera-1, Radpix1+SLDO) ?
 - . Epi implant set 1 (1 wfr), epi implant set 3 (1 wfr) : GL-GR, GL-MiniCactus+TDC+BIG (requires probably dicing per half wafer)
 - . CZ 2k implant set 1
 - 1 wfr 200 u (GL-GR, GL-MiniCactus, Panther2, TS, LFPS2, X1)
 - 1 wfr 150 u (GL-GR, GL-MiniCactus, Panther2, TS, LFPS2, X1)
 - 1 wfr 100 u (GL-GR, GL-MiniCactus, Panther2, TS, LFPS2, X1)
 - 1 wfr not thinned
 - . CZ 2k implant set 2 :
 - 1 wfr 200 u (GL-GR, GL-MiniCactus, Panther2, TS, LFPS2, X1)
 - 1 wfr 150 u (GL-GR, GL-MiniCactus, Panther2, TS, LFPS2, X1)
 - 1 wfr 100 u (GL-GR, GL-MiniCactus, Panther2, TS, LFPS2, X1)
 - . CZ 2k implant set 3 :
 - 1 wfr 200 u (GL-GR, GL-MiniCactus, Panther2, TS, LFPS2, X1)
 - 1 wfr 150 u (GL-GR, GL-MiniCactus, Panther2, TS, LFPS2, X1)
 - 1 wfr 100 u (GL-GR, GL-MiniCactus, Panther2, TS, LFPS2, X1)
 - 1 wfr not thinned
 - . Big chips (HV-PIX26, Monstera2, Radpix1+SLDO) could be picked from (almost) all the available wfr
- CZ 2k implant set 2 second priority vs set 1 and set 3, can use different thicknesses

Dicing conflicts/independance



HV-Pix26, Monstera-1, (Radpix1+SLDO) can be picked independantly

LFPS2, X1, Panther2, TS can be picked after these

Extracting BIG and/or TDC conflicts with GL-GR, MiniCactus and X1

Extracting SLDO separately from Radpix1 conflicts with MiniCactus V2. No pb if Radpix1 and SLDO picked as one block

Need to know how many standalone SLDO, TDC, BIG are needed ?

Is there a specific wafer they need to be taken from ? These three chips do not have any sensor, could be taken on epi wfrs ?

- Consider dicing by half wafer to extract these ?

Dicing

- Dicing technique : blade dicing. Laser not possible, metal layers not blocked in dicing paths.
- Known companies (list not exclusive)
 - DISCO : Japanese, has offices in France (Rousset), Germany (München), Italy (Catania), UK (London)
 - SERMA : France (La Rochelle)
 - OPTIM : France (Rousset)
 - ALTER : Franco-Italo-Germano-Spanish, has offices in France (Toulouse), Spain (Sevilla), UK (Edinburgh, Glasgow)
- Have to understand how to share costs
 - Company accepts separate orders for one unique operation
 - One institute places the order and gets reimbursed by others
 - Could we have CERN place such orders and issue invoices to the groups (as happened for the submission) ?

Known company : post-processing

- IBS (Ion Beam Services), Rousset, France
- Has processed several wafers from MPW/engineering runs in the past
- They typically outsource thinning and dicing, they do mostly ion implant, and did final metallization
- They don't do metallization anymore, but said they can help finding suitable companies
- They have accepted in the past shared orders (but put a small charge for the administrative handling on their side)

Cost estimates at IBS (2024)

- Thinning : 2100 euros per wafer. Thickness independant.
No setup cost
- Post-processing : 2250 euros setup cost per batch of 4 wafers. Post-processing itself (backside boron implant, RTA, metallization at the time) : 600 euros/wafer
- Dicing, picking of 20-30 chips/wafer : 2000 euros/wafer
- These estimates are likely to be higher now.

Questions

- How many chips for each group ?
- Thicknesses and postprocessing type ?
- How do we group operations ?
- How do we share costs ?