Lecture 3
Semiconductor tracking detectors

Eva Vilella

Department of Physics
University of Liverpool
Oliver Lodge, Liverpool L69 7ZE, UK

vilella@hep.ph.liv.ac.uk

Outline

1. Introduction

- Advantages/Disadvantages of semiconductor detectors
- Basic semiconductor properties
- Principle of operation – The pn junction
- Charge collection and diffusion
- Why silicon?
- Signal-to-noise ratio
- Radiation damage

2. Types of semiconductor detectors

- Microstrip detectors
- Double sided silicon detectors
- Hybrid pixel detectors
- 3D detectors
- New pixel technologies

3. Examples of silicon tracking detectors in old and present experiments

Advantages/Disadvantages of semiconductor detectors

✓ **Semiconductor detectors have high density**

- Large energy loss dE/dx in a short distance
- Diffusion effect is smaller than in gaseous detectors
  → achievable position resolution better than 10 μm

✓ **Low ionization energy (few eV per e^--h^+ pair) compared to**

- Gaseous detectors (20-40 eV per ion-pair) or
- Scintillators (400-1000 eV to create a photon)

✓ **Large experience in industry with ASIC technology (silicon)**

✓ **High intrinsic radiation hardness**

× **No internal amplification, i.e. small signal**

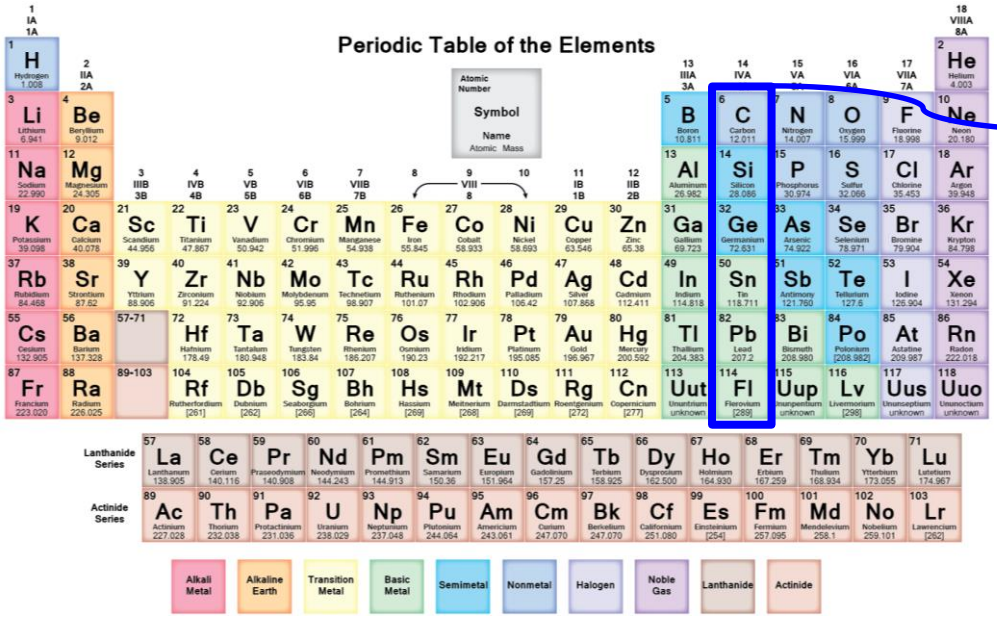
- With few exceptions

× **High cost per surface unit**

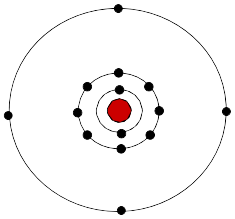
- High number of readout channels
- Large power consumption → Cooling

What is a semiconductor?

- Low resistivity → “conductor”
- High resistivity → “insulator”
- **Intermediate resistivity → “semiconductor”**
  - conductivity lies between that of conductors and insulators
  - generally crystalline in structure for IC devices



Group IV semiconductors
Each element in group IV has 4 electrons in its outer most atomic shell

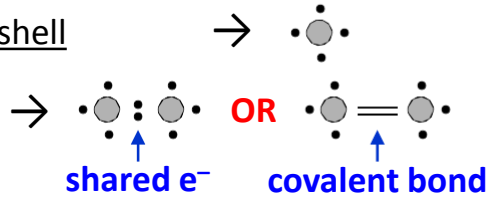


A silicon atom

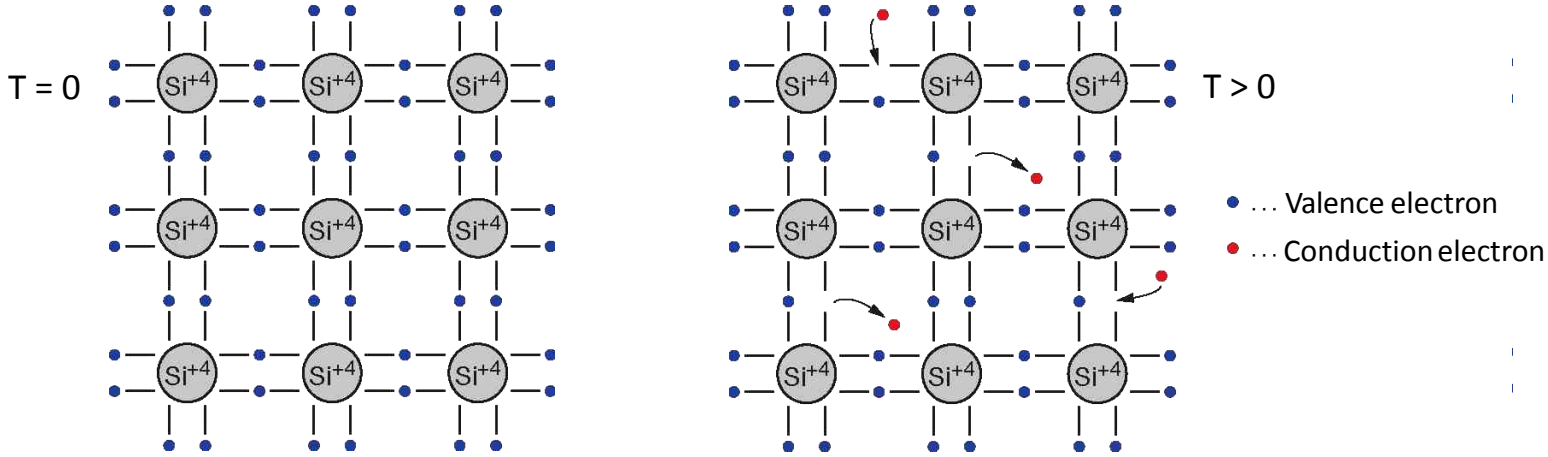
2 electrons in the first atomic shell
8 electrons in the second atomic shell
4 electrons in the third outermost atomic shell **(Valence electrons)**

Silicon crystal lattice (2D)

- Representation of a silicon atom with 4 e^- in the valence shell
- Two silicon atoms can come together to form a covalent bond by sharing 2 e^- among themselves

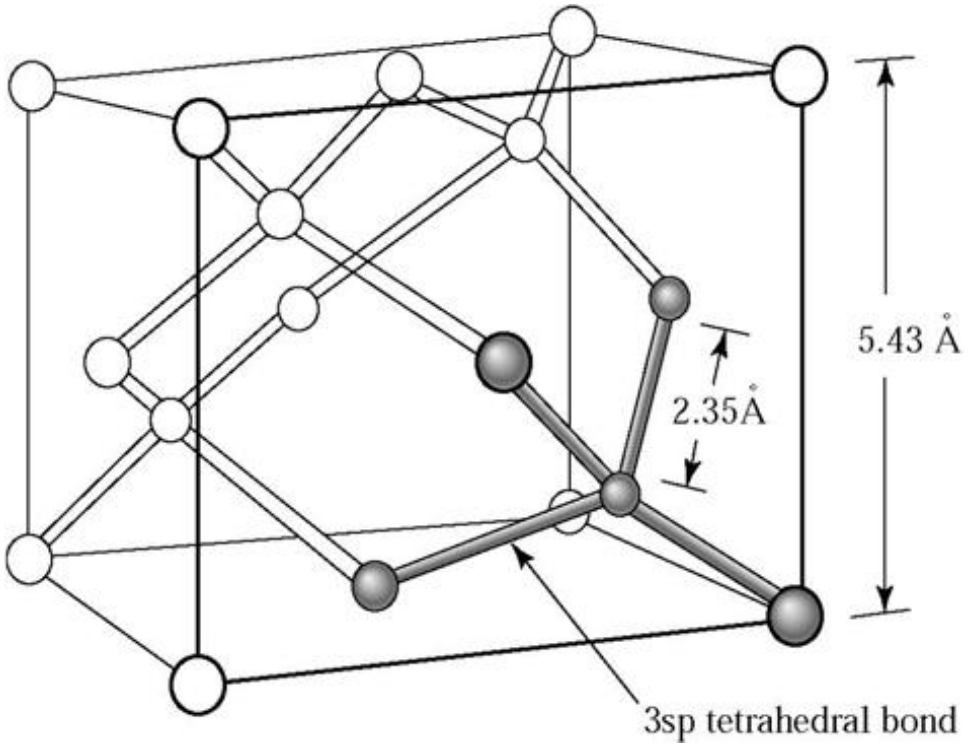


- **Bond model.** Example of a column IV elemental semiconductor (2dim projection):



- Each atom has 4 closest neighbours → the 4 e^- in the outer shell are shared (covalent bonds)
- At low temperature all e^- are bound
- At higher temperature thermal vibrations break some of the bonds → free e^- cause conductivity (e^- conduction). The remaining open bonds attract other e^- → The "holes" change position (h^+ production).

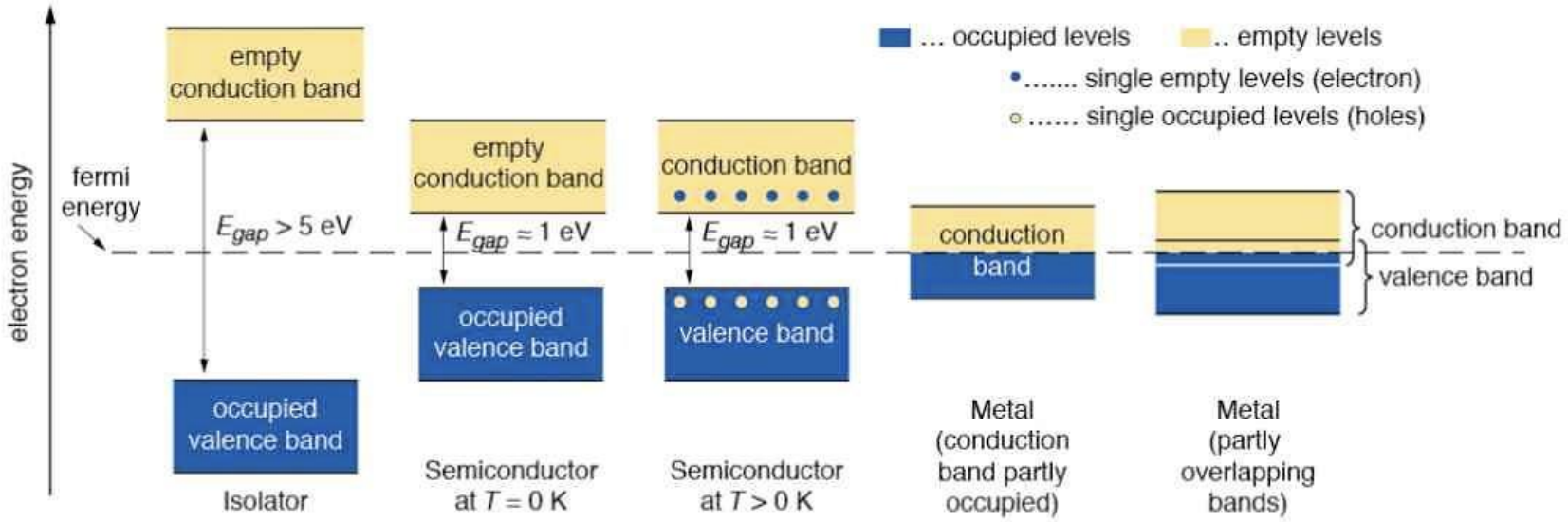
Silicon crystal lattice (3D)



- Each silicon atom is surrounded by 4 other silicon atoms in a tetrahedral configuration
- Silicon atomic density = 5×10^{22} cm^{-3}

Energy bands

- Isolated atom → e^- have only discrete energy levels
- Solid state material → atomic levels merge to **energy bands** → **conduction and valence bands**
- In semiconductors, the conduction and valence bands are separated by an energy gap → **the band gap**. In an insulator, this gap is larger.



Intrinsic carrier concentration



Generation: The breaking of a bond to generate an e^--h^+ pair



Recombination: An e^- combines with a h^+ to form a bond

- Due to the small band gap in semiconductors, electrons already occupy the conduction band at room temperature.
- Electrons from the conduction band may recombine with holes.

- A thermal equilibrium is reached between generation and recombination.
  - Charged carrier concentration → $n_e=n_h=n_i$
  - This is called **intrinsic carrier concentration** (for each conduction electron exists a corresponding hole):

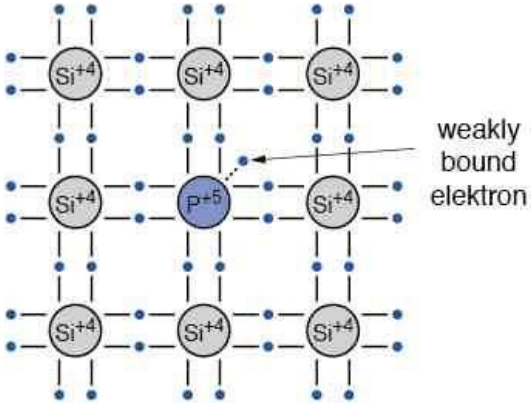
$$n_i = \sqrt{n_e n_h} \cdot exp\left(-\frac{E_g}{2kT}\right) \propto T^{3/2} \cdot exp\left(-\frac{E_g}{2kT}\right)$$

- In ultrapure silicon, the intrinsic carrier concentration is → **$n_i=1.45\cdot10^{10}$ cm^{-3}**
- With approximately 1022 atoms/cm^3, about 1 in 1012 silicon atoms is ionised.

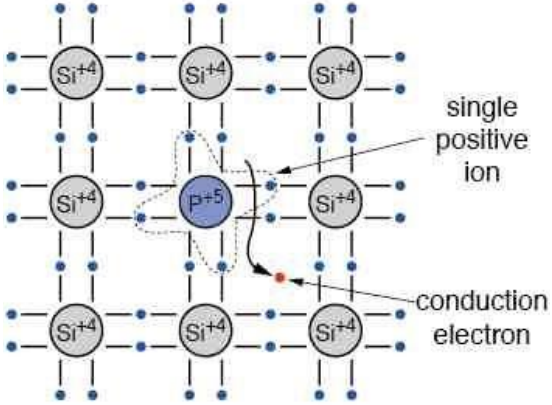
Doping

- In intrinsic silicon (T > 0) → some electrons are excited across the band gap into the conduction band, leaving behind an electron vacancy or hole in the lattice → **charge flowing**
- With an external V_{bias} → both the electron and the hole can move across the material
- **Doping** → **intentional introduction of impurities into intrinsic silicon to modulate its intrinsic properties (increase current flow). Extrinsic semiconductor.**
- **Doping with a group V element (e.g. P, As, Sb).** The 5th valence electrons are weakly bound.

The doping atom is a **donor**



The released conduction e$^-$ leaves a positively charged ion

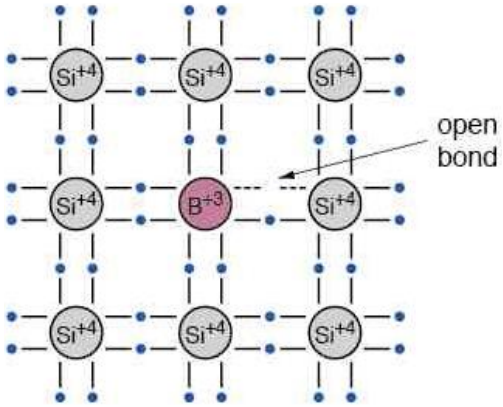


- In n-type semiconductor → the dopant contributes extra electrons, dramatically increasing the conductivity

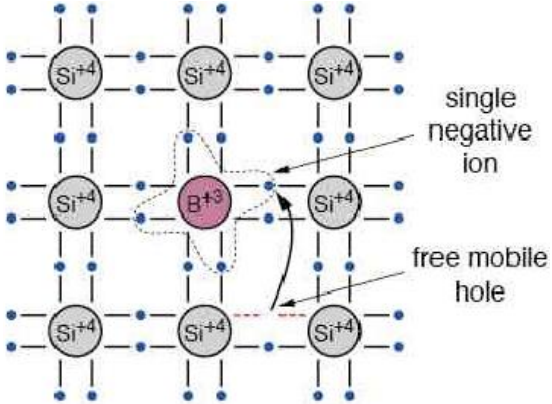
Doping

- In intrinsic silicon (T > 0) → some electrons are excited across the band gap into the conduction band, leaving behind an electron vacancy or hole in the lattice → **charge flowing**
- With an external V_{bias} → both the electron and the hole can move across the material
- **Doping** → **intentional introduction of impurities into intrinsic silicon to modulate its intrinsic properties (increase current flow). Extrinsic semiconductor.**
- **Doping with a group III element (e.g. B, Al, Ga, In).** One valence bond remains open. It attracts electrons from neighbouring atoms.

The doping atom is an **acceptor**



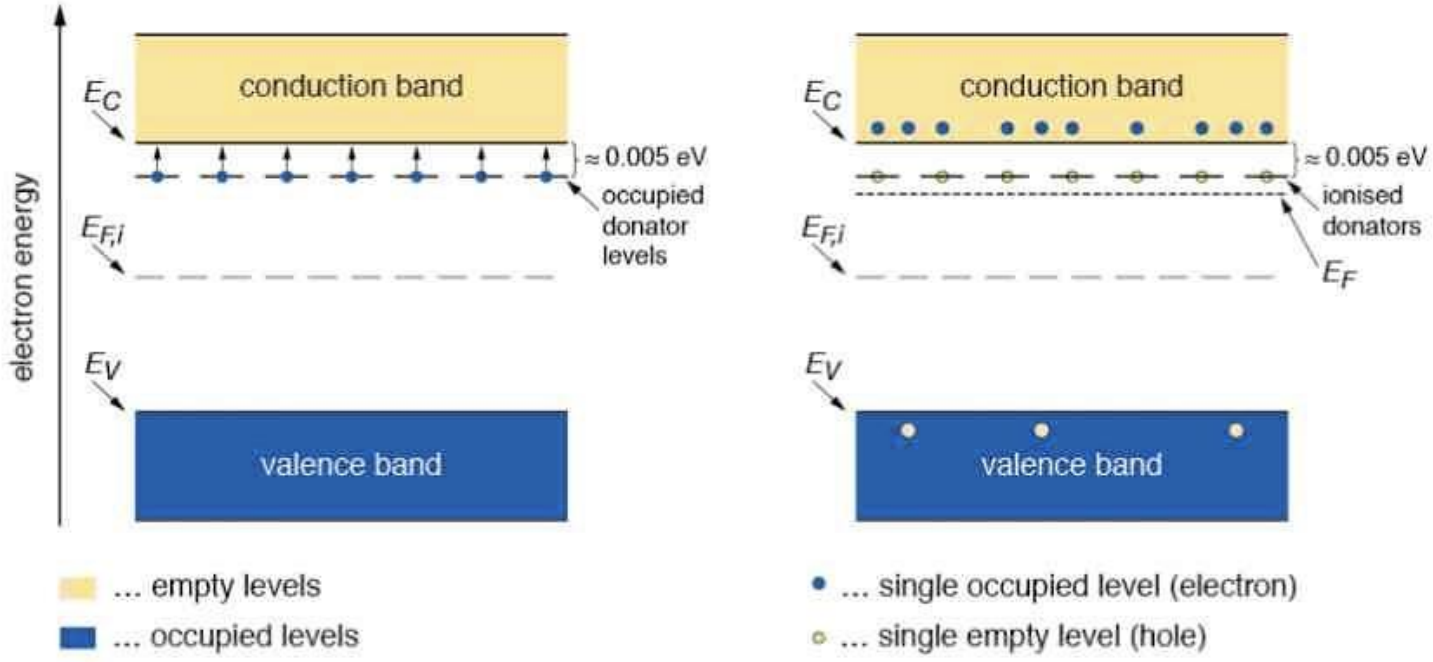
The acceptor atom in the lattice is negatively charged



- In p-type semiconductor → the dopant produces extra vacancies or holes, which likewise increase the conductivity

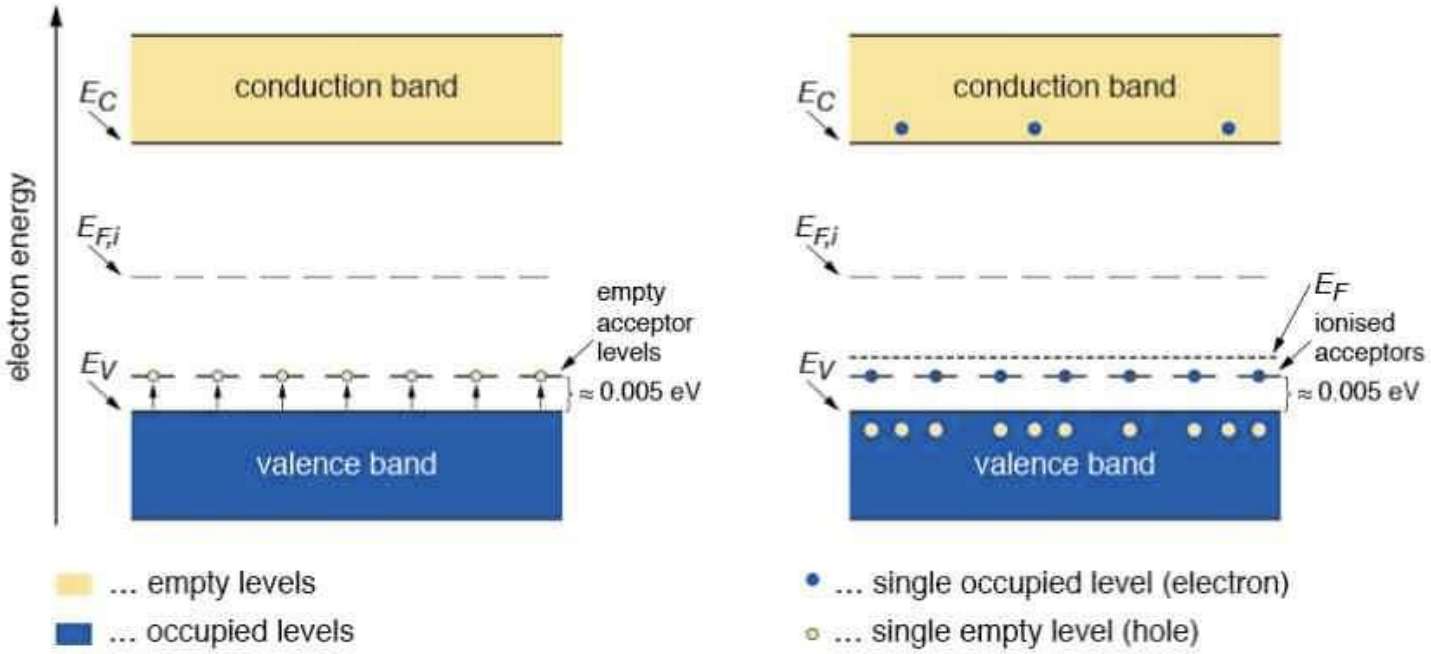
Doping and energy bands

- Energy level of a **donor** → just **below** the edge of the **conduction band**.
- At room temperature → most electrons are raised to the conduction band.
- The Fermi level E_F moves up.



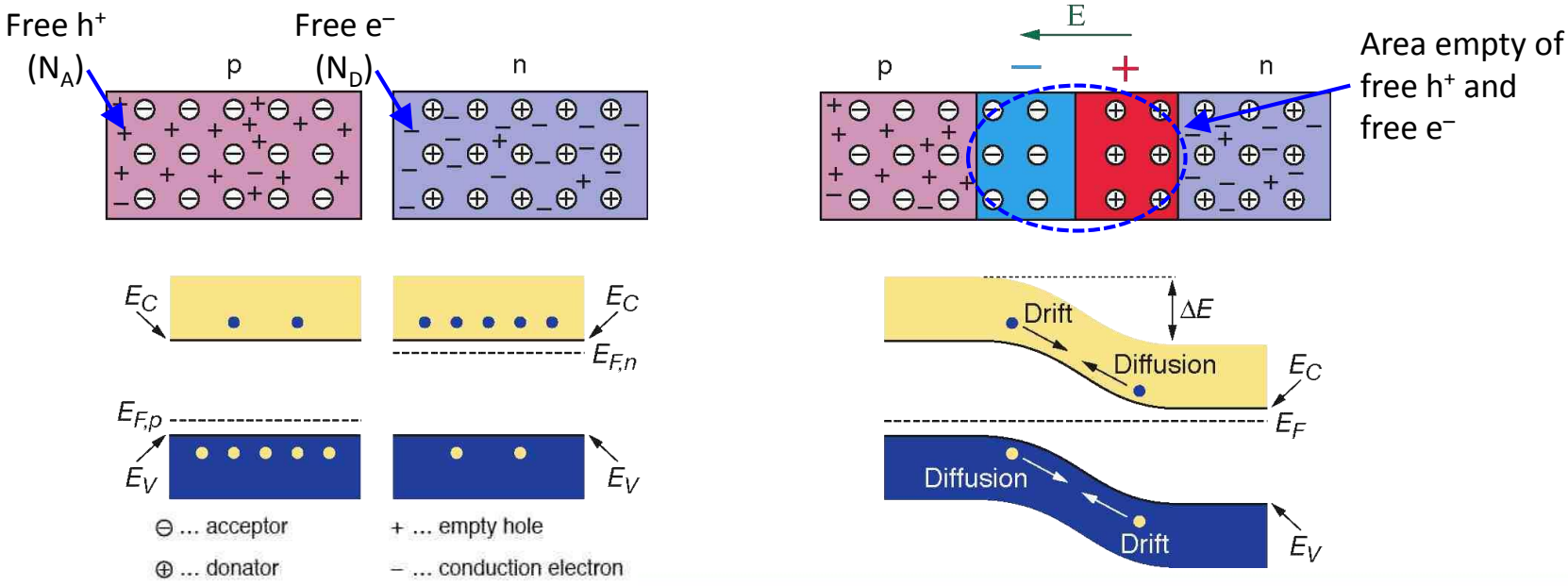
Doping and energy bands

- Energy level of an **acceptor** → just **above** the edge of the **valence band**.
- At room temperature → most levels are occupied by electrons leaving holes in the valence band.
- The Fermi level E_F moves down.



The pn junction

- Interface of an n-type and p-type semiconductor → the difference in the Fermi levels cause diffusion of extra carries to the other material (h^+ from the p-type to the n-type, and e^- from the n-type to the p-type) until thermal equilibrium is reached.
- At this point the Fermi level is equal. The remaining ions create a space charge and an electric field stopping further diffusion.
- The stable space charge region is empty of free charge carries and is called the **depletion zone**.



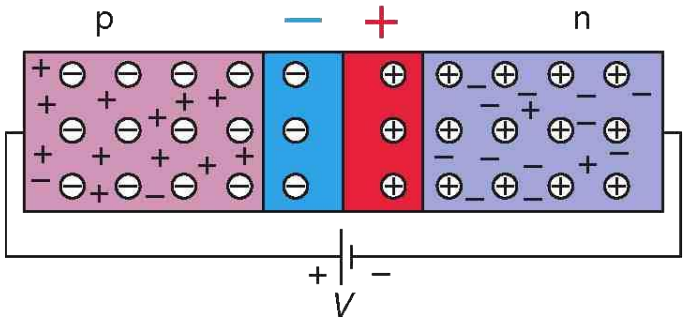
The pn junction

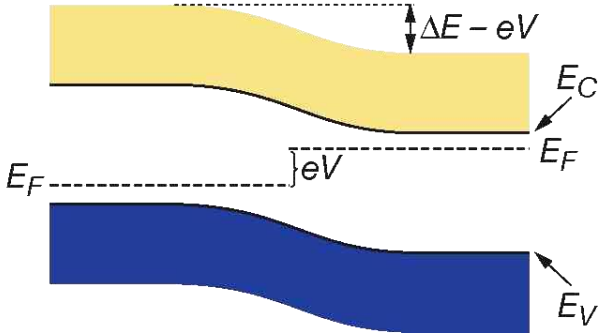
- Application of an external voltage (V):
  - * V_+ to the **p-type semiconductor (anode)**
  - * V_- to the **n-type semiconductor (cathode)**
  - * e^- from the n-type and h^+ from the p-type are pushed towards the junction
  - * The depletion region becomes narrower

- $W = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q}\frac{N_A+N_D}{N_A N_D}|V|}$, where N_A and N_D are the positive and negative doping, respectively, in cm^{-3}, and $|V|$ the external voltage

- The potential barrier becomes smaller and diffusion across the junction becomes easier.
- The current across the junction increases significantly.

p-n junction with forward bias

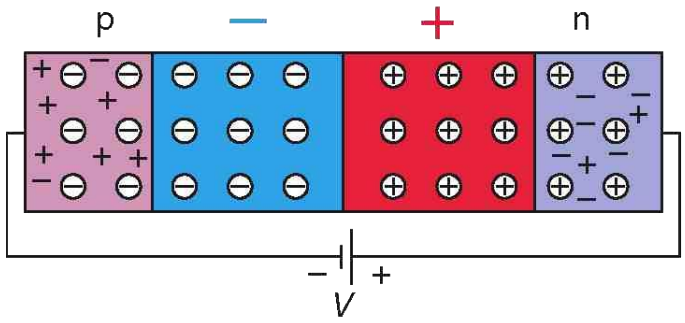




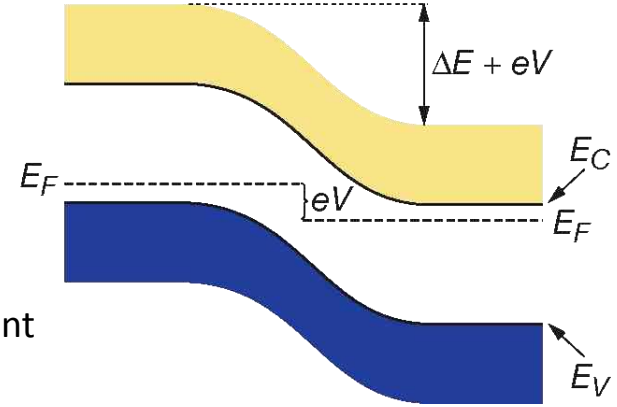
The pn junction

- Application of an external voltage (V):
  - * V_+ to the **n-type semiconductor (cathode)**
  - * V_- to the **p-type semiconductor (anode)**
  - * e^-/h^+ are pulled out from the depletion zone
  - * The depletion region becomes larger

p-n junction with reverse bias



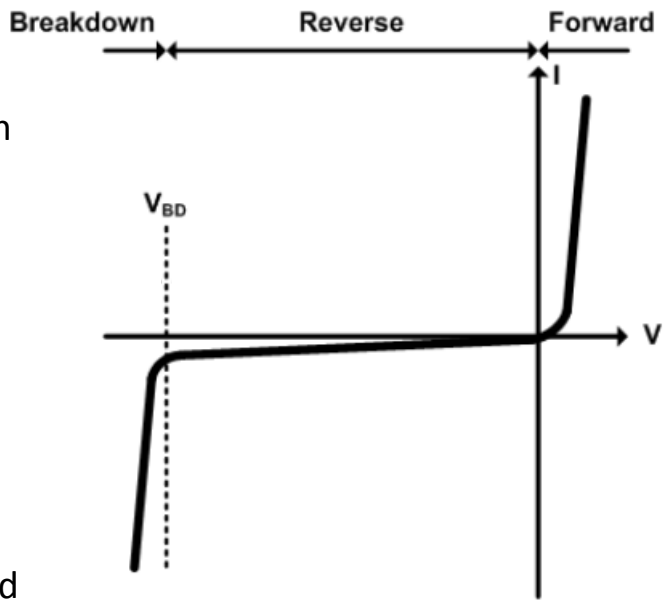
- $W = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q}\frac{N_A+N_D}{N_A N_D}|V|}$, where N_A and N_D are the positive and negative doping, respectively, in cm^{-3}, and $|V|$ the external voltage



- The potential barrier becomes higher and diffusion across the junction is suppressed.
- The current across the junction is very small ("leakage current").
- **A silicon detector is operated in reverse bias!!** Leakage current is important (dominated by thermally generated e^--h^+ pairs).

The pn junction – I(V) and basic equations

- Typical **current-voltage** of a pn junction:
  - Exponential current increase in forward bias
  - Small saturation in reverse bias until reverse breakdown

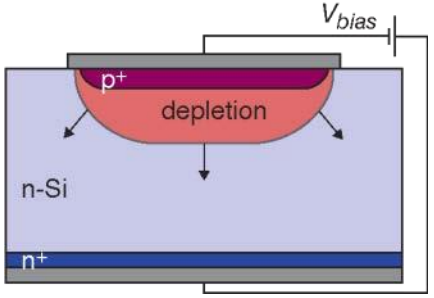


- **Ideal diode equation** → $I = I_0 \left[exp\left(\frac{qV}{kT}\right) - 1 \right]$, where I_0 is the reverse saturation current

- **Depletion width** → $W = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q}\frac{N_A+N_D}{N_A N_D}|V|}$, where N_A and N_D are the positive and negative doping, respectively, in cm^{-3}, and $|V|$ the external voltage

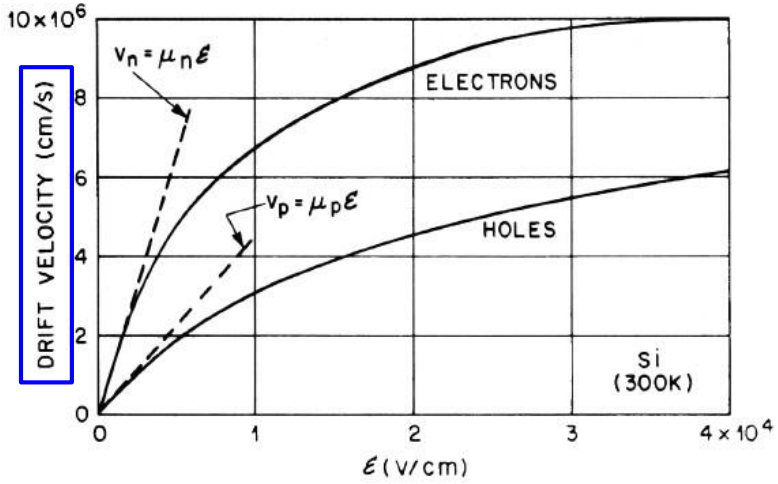
- **Capacitance** → $C_D = \frac{\varepsilon_0\varepsilon_r}{W} \cdot A$, where A is the area of the diode

- **Resistivity** → $\rho = \frac{1}{q(\mu_e n + \mu_h p)}$, where μ_e and μ_h are the electron an hole mobilities, respectively, and *n* and *p* are the electron and hole densities.

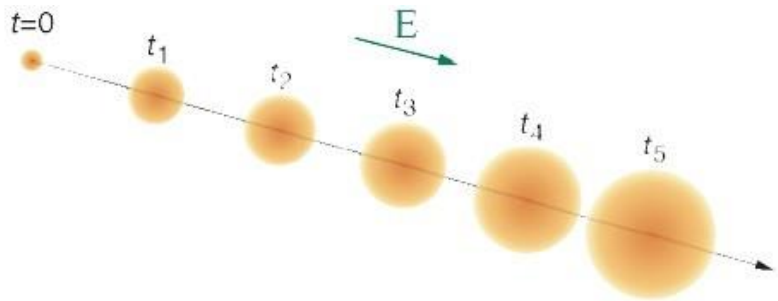


Charge collection and diffusion

- **e^--h^+ pairs created in the depletion region move under the $\vec{E}$ (drift)**
  - $\boldsymbol{v_{e,h}(x) = \mu_{e,h} E(x)}$
  - $\mu_e = 1500\ cm^2/Vs, \mu_h = 450\ cm^2/Vs$ (in silicon)
- The time required for a carrier to traverse the depletion region (the sensitive volume) is the collection time.
  - $t_d = x/\mu E\ (x)$



- It is also possible to have **diffusion** created by random thermal motion.
- The width of the charge cloud after a time t is given by:
  - $\boldsymbol{\sigma = \sqrt{2Dt_d}}$, where D is the diffusion coefficient $D = \mu kT/q$, μ the charge carrier mobility, k the Boltzman constant, T the temperature and q the electron charge.



Drift in E-field + diffusion

Why silicon?

- **Some properties of silicon crystals**
  - **Small bandgap** E_g=1.12 eV → E(e^--h^+)=3.6 eV (≈ 30 eV in gas detectors)
  - **High specific density** 2.33 g/cm^3; dE/dx (MIP)≈3.8 MeV/cm≈106 e^--h^+/μm (≈ 100 e^--ion/cm in gas)
  - **High carrier mobility** μ_e=1450 cm^2/Vs, μ_h=450 cm^2/Vs → fast charge collection (< 30 ns)
  - **Very pure** < 1ppm impurities
  - **Rigidity** It allows thin self supporting structures
  - **Large experience in industry (also with ASIC technology)**
  - **High intrinsic radiation hardness**

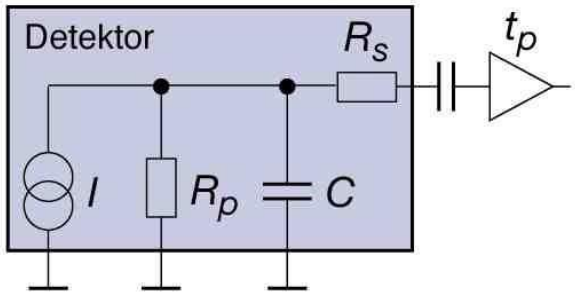
- **Alternative semiconductors**
  - Diamond
  - Gallium arsenide (GaAs)
  - Silicon Carbide (SiC)
  - Germanium

	Diamond	SiC (4H)	GaAs	Si	Ge
Atomic number Z	6	14/6	31/33	14	32
Bandgap Eg [eV]	5.5	3.3	1.42	1.12	0.66
E(e^-/h^+) [eV]	13	7.6/8.4	4.3	3.6	2.9
Density [g/cm^3]	3.51	3.22	5.32	2.33	5.32
e^- mobility [cm^2/Vs]	1800	800	8500	1450	3900
h^+ mobility [cm^2/Vs]	1200	115	400	450	1900

Signal-to-noise ratio

- The **signal** generated in a silicon detector depends essentially only on:
  - thickness of the depletion zone
  - dE/dx of the particle
- The **noise** in a silicon detector system depends on various parameters:
  - detector capacity (usually the dominant noise source in a detector system)
  - leakage current
  - biasing scheme
  - readout electronics
- Noise is typically given as **equivalent noise charge (ENC)** –It is the noise at the input of the amplifier in elementary charges:

$$ENC = \sqrt{ENC_C^2 + ENC_I^2 + ENC_{Rp}^2 + ENC_{Rs}^2}$$



- One of the most important parameters of a detector is the **signal-to-noise ratio (SNR)**. A good detector should have a large SNR.

Radiation damage

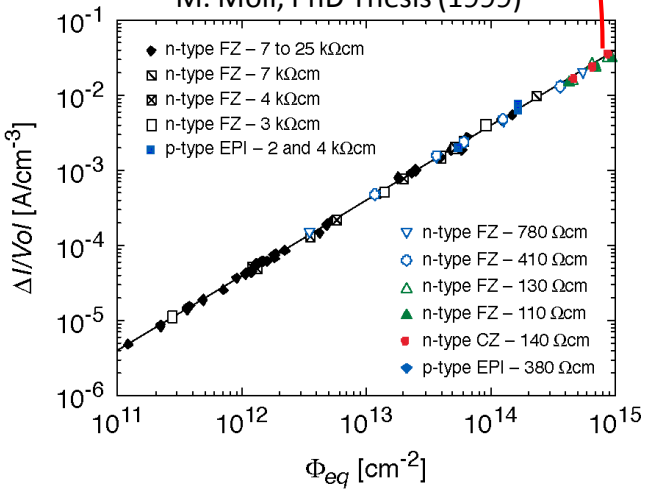
- Particles (radiation) interact:
  - **with electrons** → it is used for particle detection and results in temporarily effects only
  - **with atoms** → it may cause permanent changes (**defects**) in the detector bulk
    → defects may change with time. One distinguishes between primary defects and secondary defects (secondary defects appear with time caused by moving primary defects).
- One distinguishes between:
  - **bulk damage** → damage inside the detector bulk → dislocated atoms from their position in the lattice.
    → caused by massive particles → primarily by neutrons, protons and pions.
  - **surface damage** → damage introduced in the surface layers due to charges generated in the oxide. Due to the isolating character of the oxide, these charges cannot disappear and lead to local concentrations.
    → primarily produced by photons and charged particles.

Radiation damage

Irradiation induced leakage current linear dependence with integrated flux

- **Bulk damage** → **Defects** in the semiconductor lattice create energy levels in the band gap between the valence and conduction band.
- **Consequences** (depending on the position of the energy levels):
  1. Modification of the effective doping concentration
     - Shift of the **depletion voltage**
     - Caused by shallow energy levels (close to the band edges)
  2. Trapping of charge carriers
     - Reduced **lifetime** of charge carriers
     - Mainly caused by deep energy levels
  3. Easier thermal excitement of e^--h^+
     - Increase of the **leakage current**

In ten years of LHC operation, the currents of the innermost layers increase by 3 orders of magnitude!
M. Moll, PhD Thesis (1999)



- One distinguishes between **point defects** and **cluster defects** (depending on the energy of the input particle). **Point defects anneal with time**.
- Other transformations → an atom might be transformed in another type (i.e. a silicon atom in a phosphor atom with the subsequent beta decay → the new atom acts as a regular dopant –either as a donor or acceptor).

Radiation damage

- **Surface defects (defects in the oxide) →** Ionizing radiation creates charges in the oxide.
- The mobility of electrons in SiO_2 is much larger than the mobility of holes

  → electrons diffuse out of the oxide, holes remain semi permanent fixed
  → the oxide becomes positively charged due to these fixed oxide charges

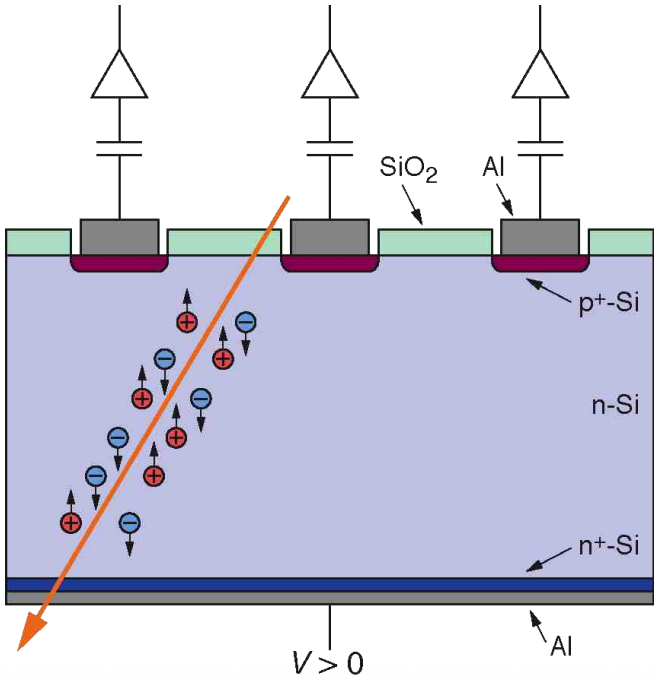
- **Consequences for the detector**:
  1. Reduced electrical separation between implants
  2. Increase of inter-strip capacitance
  3. Increase of detector noise
  4. Decrease of position resolution
  5. Increase of surface leakage current

- Radiation damage is also a very critical issue for the readout electronics!

Microstrip detectors (DC or AC coupled)

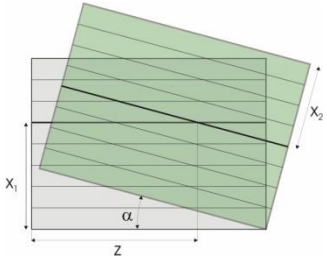
- Through going charged particles → create e^--h^+ pairs in the depletion zone (≈30.000 pairs in standard detector thickness).
- These charges drift to the electrodes → creation of a drift current (signal).
- The signal is amplified by an amplifier connected to each strip.
- From the signals on the individual strips (segmentation), the position of the through going particle is deduced.

- **A typical n-type Si strip detector:**
  - p^+n junction
    $N_D \approx 10^{15}$ cm^{-3}, $N_A \approx$ 1-5·10^{12} cm^{-3}
  - n-type bulk: $\rho > 2k\ \Omega cm$
    thickness 300 µm
  - Operating voltage < 200 V
  - n^+ layer on backplane to improve ohmic contact
  - Aluminum metallization
  - Highest field closest to the collecting electrodes (where most of the signal is induced)



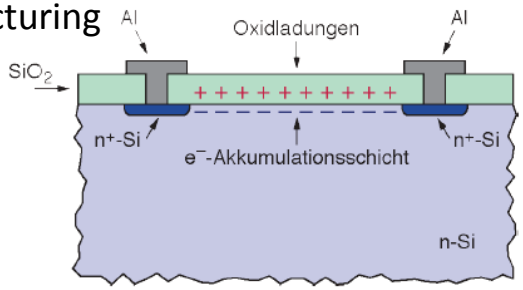
Double sided silicon detectors

- **Advantages:**
  - ✓ More elegant way for measuring 2 coordinates than using stereo modules
  - ✓ Saves material

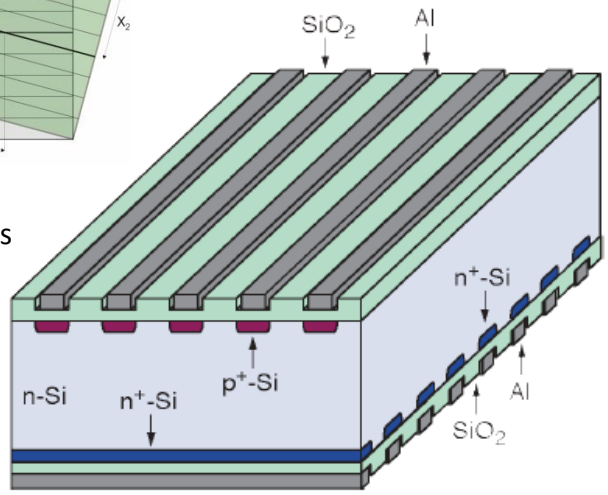


Stereo modules

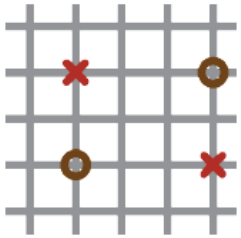
- **Disadvantages:**
  - × Needs special strip insulation of n-side (p-stop, p-spray techniques)
  - × Very complicated manufacturing and handling procedures
  - × Expensive



Positive oxide charges cause electron accumulation layer



Scheme of a double sided strip detector (biasing structures not shown)

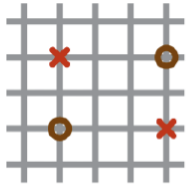


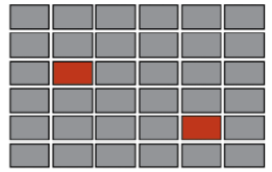
Real hits
"Ghosts"

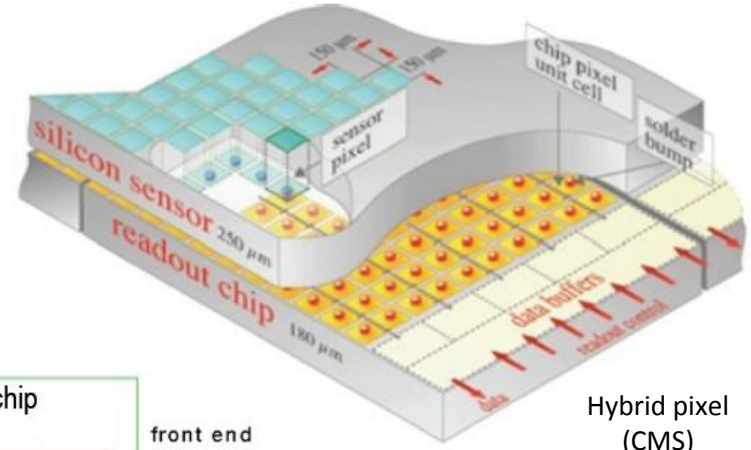
  - × Ghost hits at high occupancy

Hybrid pixel detectors

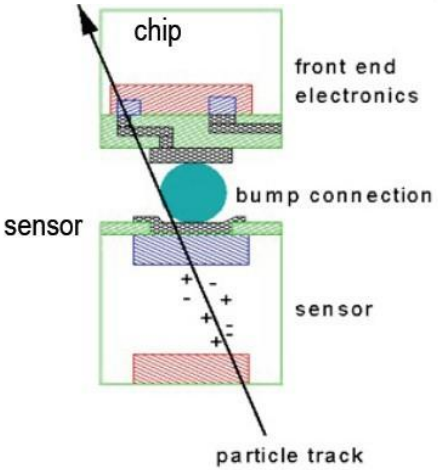
- Segment silicon to diode matrix with high granularity (true 2D reconstruction)
- Readout electronics with same geometry
- Connection by bump bonding
- **Advantages:**
  - ✓ Pixel detectors produce unambiguous hits
  - ✓ Small pixel area
    - → Low detector capacitance (≈1 fF/pixel)
    - → Large signal-to-noise ratio (e.g. 150:1)
  - ✓ Small pixel volume
    - → Low leakage current (≈1 pA/pixel)
- **Disadvantages:**
  - × Large number of readout channels
    - → Large number of electrical connections
    - → Large bandwidth
    - → Large power consumption
- Used in ATLAS, ALICE, CMS and LHCb



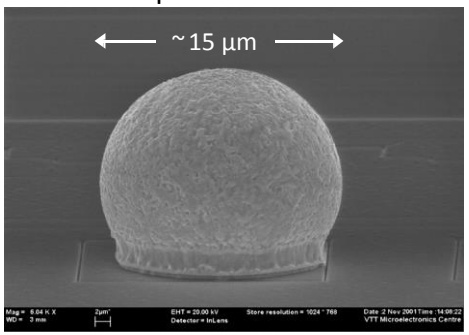




Hybrid pixel (CMS)



Solder Bump: Pb-Sn

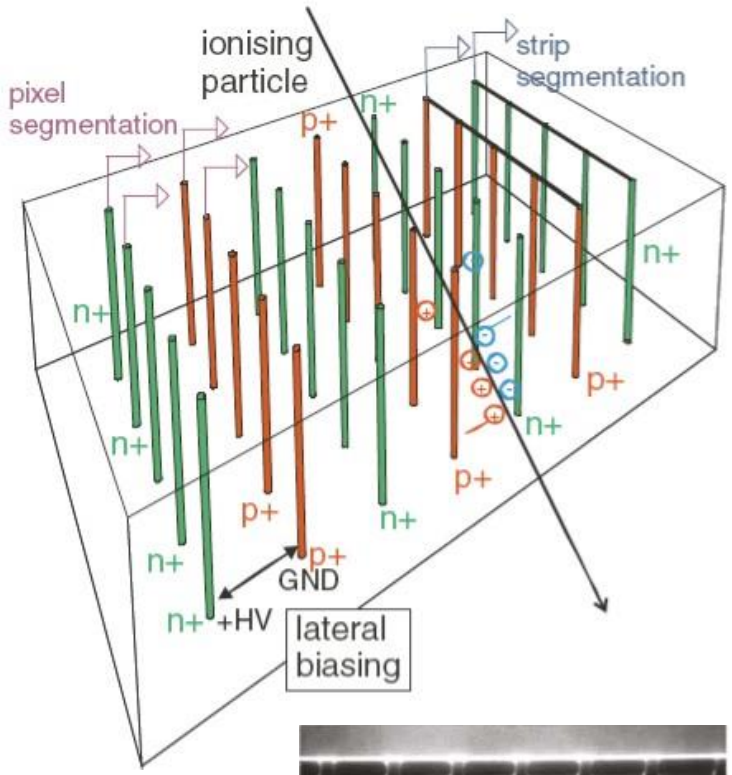


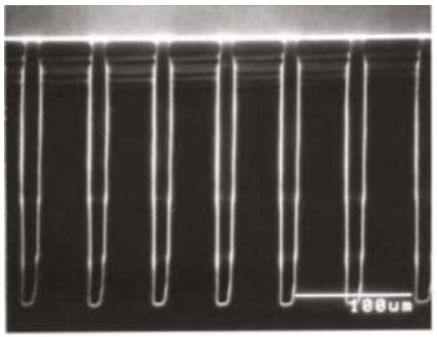
3D detectors

- Doped electrodes penetrating vertically through detector substrate
- Deep holes are etched into the silicon
  - Filled with n^+ and p^+ material
  - Voltage is applied between
  - Depletion is sideways

- Increased radiation hardness due to small distances between the electrodes
- Very low depletion voltages
- Very fast, since charge carries travel shorter distances
- But production is expensive and complex

- Very radiation tolerant detectors, in discussion for inner detector layers at SLHC

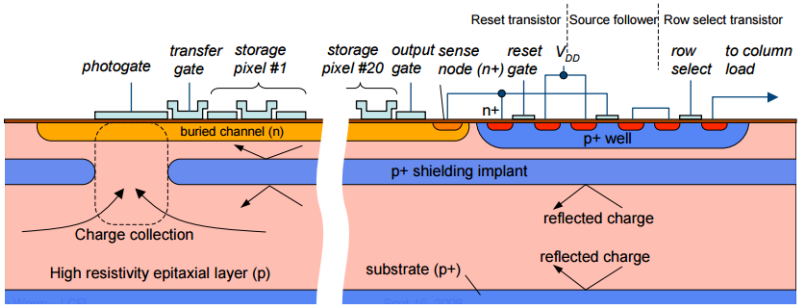




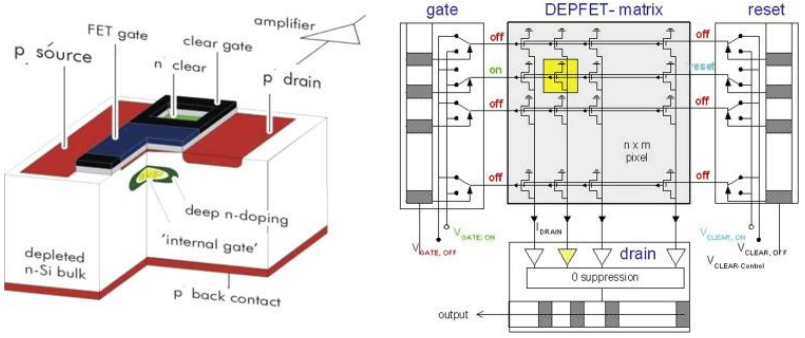
Picture from CNM-IMB (CSIC), Barcelona

New pixel technologies

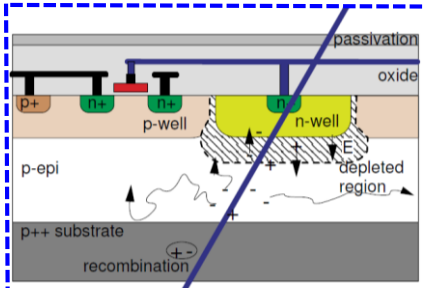
- **Huge number of new developments!!**



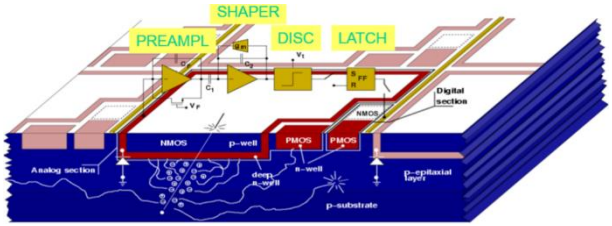
ISIS (In-Situ Storage Image Sensor) & other CCDs



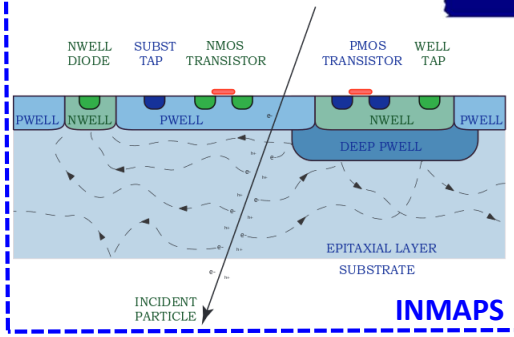
DEPFET (DEPleted Field Effect Transistor)



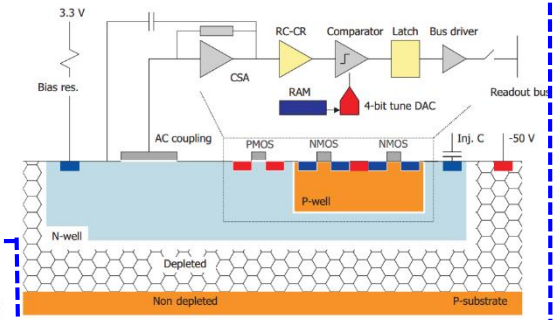
MAPS (Monolithic Active Pixel Sensor)



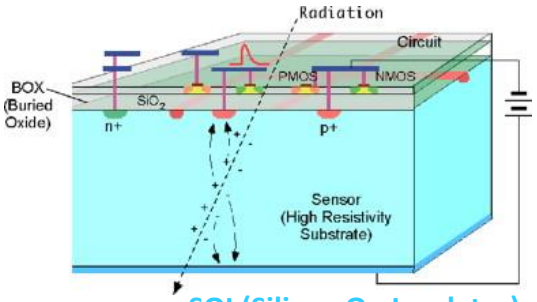
DNW MAPS



INMAPS



HV-CMOS or HV-MAPS (High Voltage)



SOI (Silicon On Insulator)

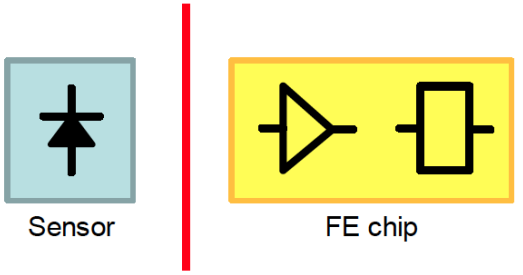
- **New trend in HEP…**

Exploit industry standard <u>CMOS</u> and <u>High-Voltage CMOS</u> technologies to develop a new generation of fast and radiation tolerant position sensitive detectors.

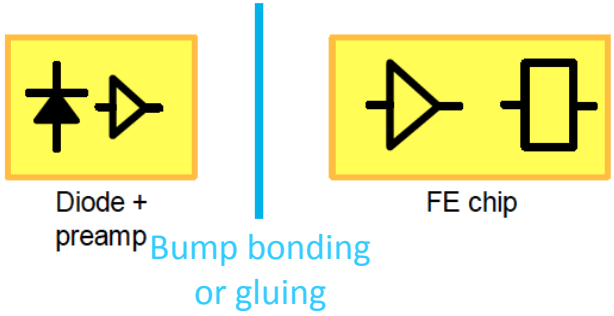
Why are CMOS/HV-CMOS so attractive?

- CMOS and HV-CMOS are industry standard technologies
  → **leading edge performance and low-cost**
- In-pixel amplification
- In-pixel processing electronics are also possible
  → **very strong signal at pixel output**
- **Readout and digitization electronics can be integrated on the same chip** with the pixel array
- Very small pixel sizes are possible → **high granularity**
- Low leakage current + small sensor capacitance
  → **excellent noise performance**
- **High signal-to-noise ratio**
- Low power consumption
- **100% fill-factor** is possible
- **Back-thinning to 50 µm** is possible whilst sensor performance is unaffected
- Good speed and good radiation tolerance (HV-CMOS, HV-MAPS)

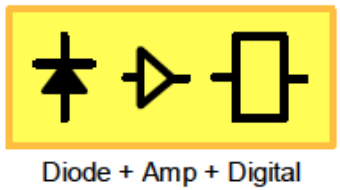
Hybrids:



Hybrid HV-CMOS:

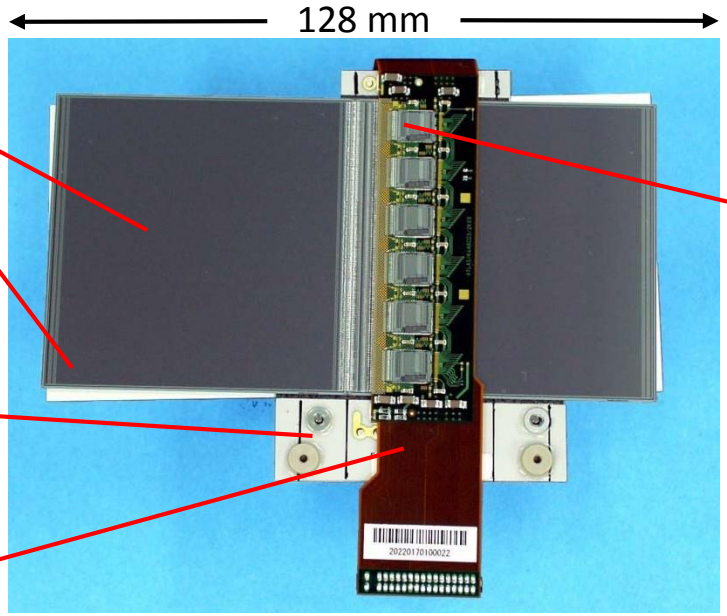


Monolithic MAPS and HV-MAPS:



Detector module

- *"The basic building block of silicon based tracking detectors"*
- **Example: ATLAS SCT Barrel Module → 4 silicon sensors with centre-tapped readout electronics**



SCT = SemiConductor Tracker
TPG = Thermal Pyrolytic Graphite

Silicon sensors (x4)
- 64 x 64 mm^2
- p-in-n, single sided
- AC-coupled
- 768 strips
- 80 µm pitch/12 µm width

Mechanical support
- TPG baseboard
- BeO facings

Hybrid (x1)
- flexible 4 layer copper/kapton hybrid
- mounted directly over two of the four silicon sensors
- carrying front-end electronics, pitch adapter, signal routing, connector

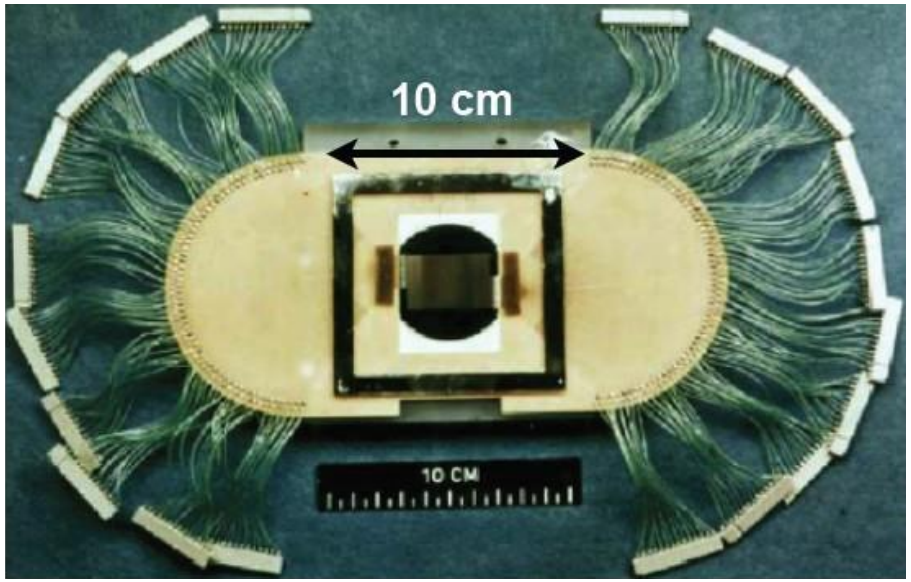
ASICs (x12)
- ABCD chip (binary readout)
- DMILL technology
- 128 channels

Wire bonds (~3500)
- 25 µm Al wires

ATLAS – SCT
- 15.522 strip sensors
- 2.112 barrel modules
- 1.976 forward modules
- 61 m^2 silicon, 6.3·10^6 strips

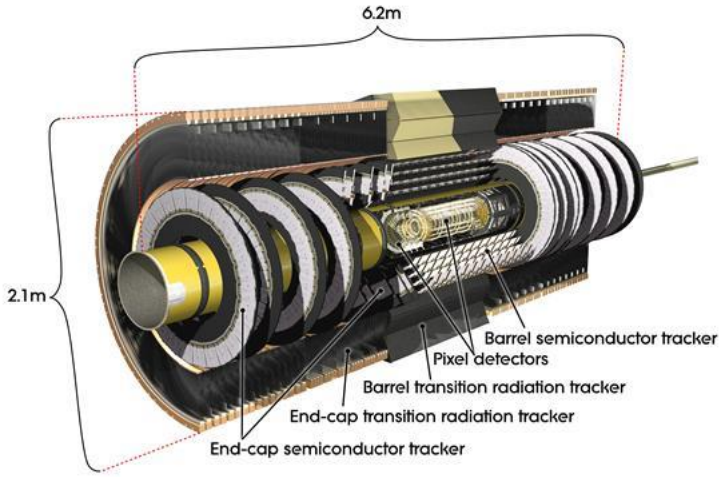
From NA11 at CERN…

- *First use of a position-sensitive silicon detector in a HEP experiment (1981)*
- ***Silicon was an exotic tracking medium…***
- **Aim:**
  * Measure lifetime of charm mesons (decay length 30 µm) → spatial resolution better 10µm required
- **NA11 detector:**
  * 1200 diode strips with 20 µm pitch on 24 x 36 cm^2 active area
  * 250-500 µm thick bulk material
  * 8 silicon detectors (2 in front, 6 behind the target)
  * 4.5 µm resolution

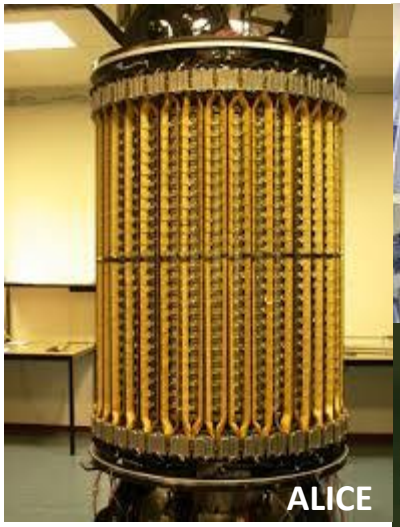


… to present time

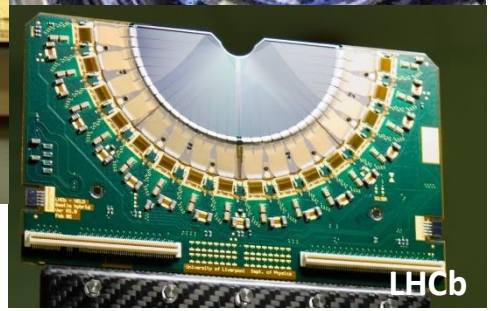
- ***Silicon has become a common tracking medium!!***
- **ATLAS**
  - Pixel detector: 80M pixels in 1.7 m^2 of silicon
    1.744 modules with 46.080 readout channels per module
  - SCT: 4.088 two-sided modules
    > 6M readout strips
    60 m^2 2 of silicon
- **CMS**
  - The largest silicon detector ever built!
  - Pixels: 65M
  - Strips: 15200 modules
    10M detector strips
    80M readout chips
- **ALICE**
  - Pixel sensors
  - Drift detectors
  - Double sided strip detectors
- **LHCb** VELO: Si Strips



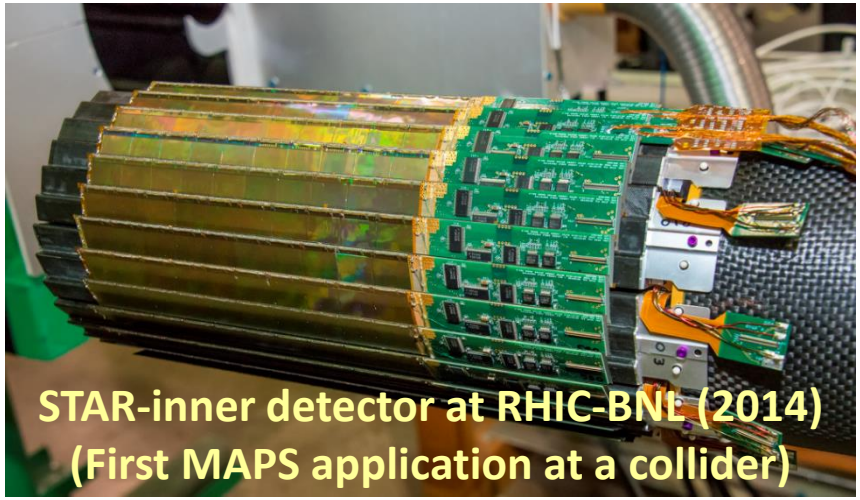
ATLAS inner detector

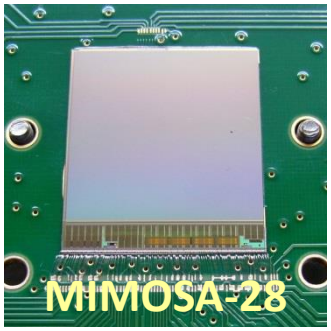






… and future - MAPS sensors in HEP



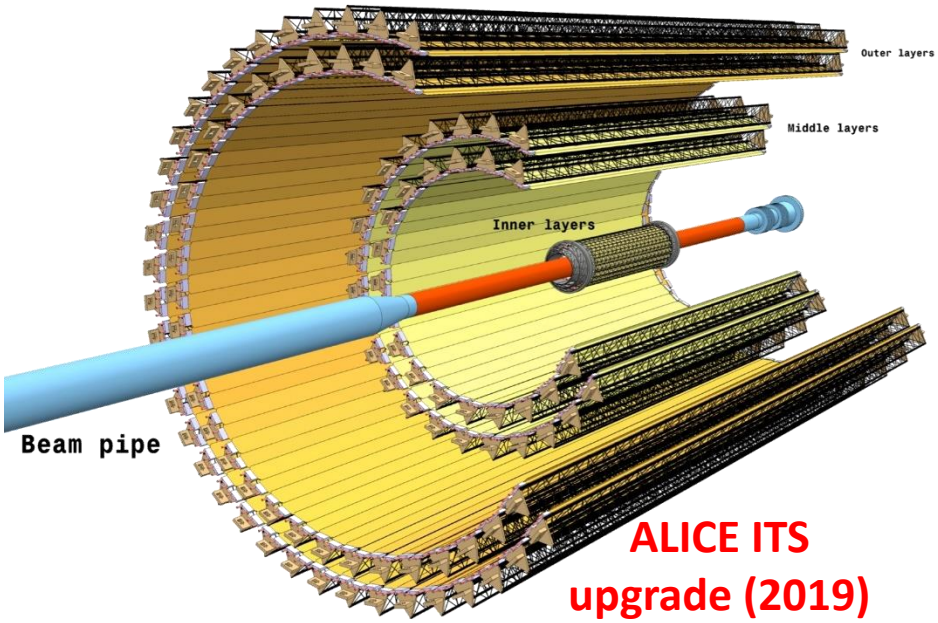


MIMOSA-28 (ULTIMATE)

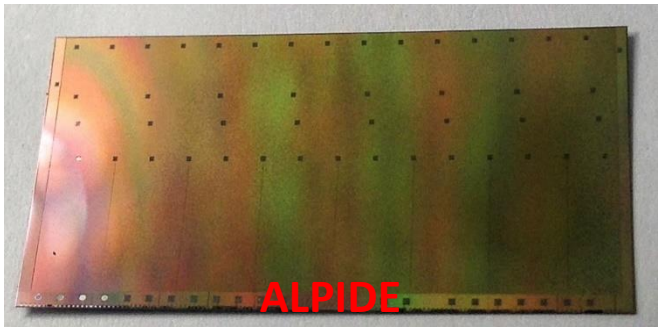
- **Chip size** 20.22 mm x 22.71 mm
- **Sensor matrix** 928 x 960 pixels (~0.9M pixels)
- **Pixel pitch** 20.7 µm x 20.7 µm
- **Techno. process** AMS 0.35 µm OPTO (twin well)
  TID 150 krad
  NIEL few 10^{12} 1 MeV n_{eq}/cm^2
- **Epitaxial layer** 15 µm (>400 Ω·cm)
- **Fabrication** 2011

- **Readout electronics:**
  - in-pixel amplification
  - correlated double sampling
  - EOC with discriminator
  - zero suppression
  - on-chip memory to store digital signals
  - readout mode by rows (185.6 µs)

… and future - MAPS sensors in HEP



ALICE ITS upgrade (2019)



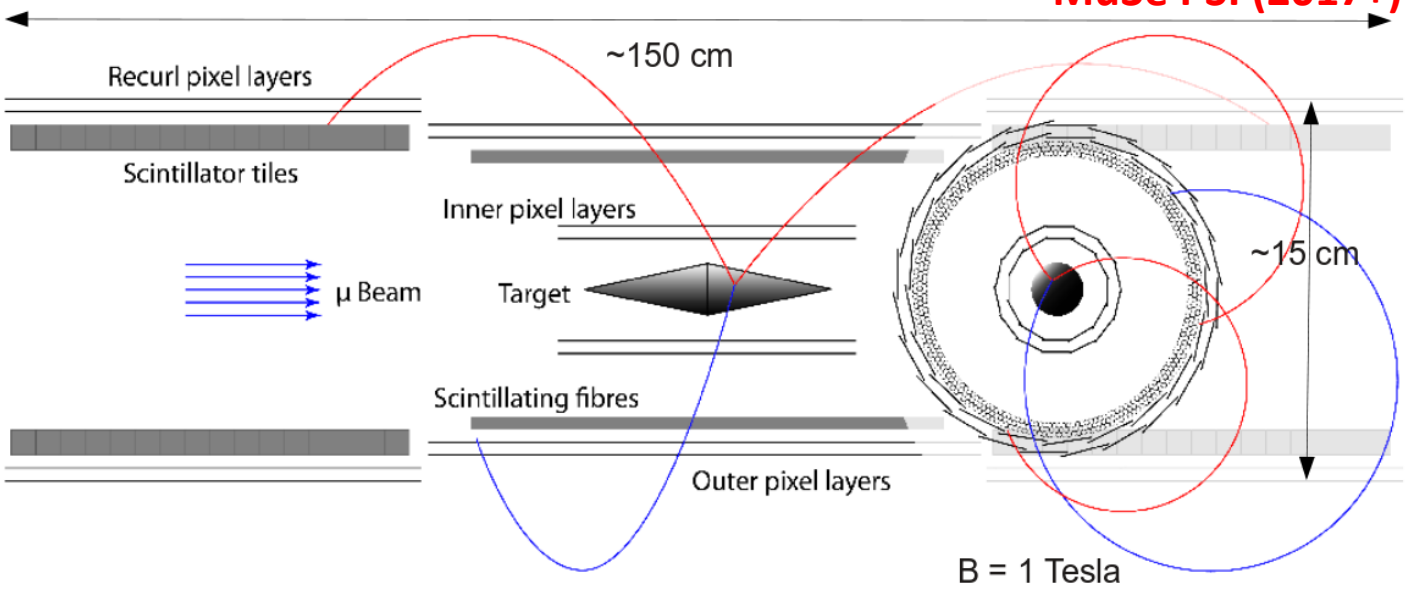
ALPIDE

- **Chip size** 15 mm x 30 mm
- **Sensor matrix** 512 x 1024 pixels (>0.5M pixels)
- **Pixel pitch** 28 µm x 28 µm
- **Techno. process** TowerJazz 180 nm (quad. well)
  TID 700 krad
  NIEL 10^{13} 1 MeV n_{eq}/cm^2
- **Epitaxial layer** 18-40 µm (>1k Ω·cm)
- **Fabrication** 2014 (CERN, INFN, CCNU, Yonsei)

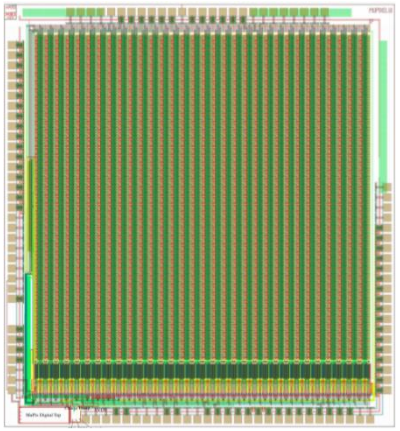
- **Readout electronics:**
  - in-pixel amplification/discrimination
  - integration time ~4 µs
  - hit recording and pixel address generation
  - data-driven readout (async. priority encoder)
  - readout time α to chip occupancy
    - 1 hit/column (foreseen) → ~10 µs

… and future - HV-MAPS sensors in HEP

Mu3e PSI (2017+)



MuPix7



- **Mu3e experiment** → Search for new physics beyond the Standard Model by looking at the lepton flavor violating decay $\mu^+ \rightarrow e^+e^-e^+$
- **It is the first experiment that will see HV-MAPS (MuPix) operate in a real application!**
- Pixel size → 103 μm x 80 μm
- Time resolution → 14.2 ns (with sensor operated at 300 mW/cm^2)
- Sensor thinned down to 50 μm
- Currently working towards **MuPix8**, **a large area chip (HR) that will be submitted in 2016**

Use of silicon sensors in HEP

- The number of readout channels in silicon tracking systems for particle physics experiments shows a continuously increasing trend !!!

