



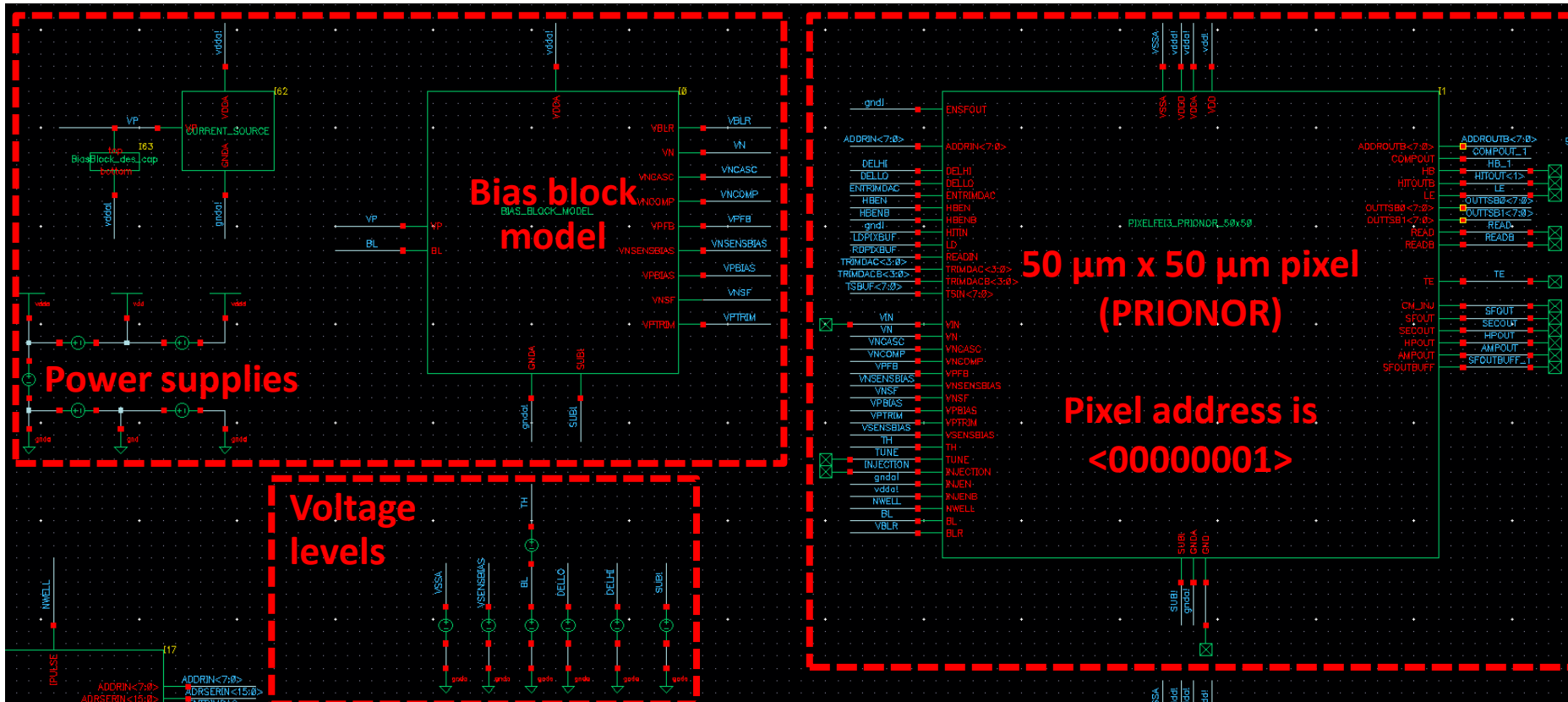
RD50-MPW1

Post-layout simulations

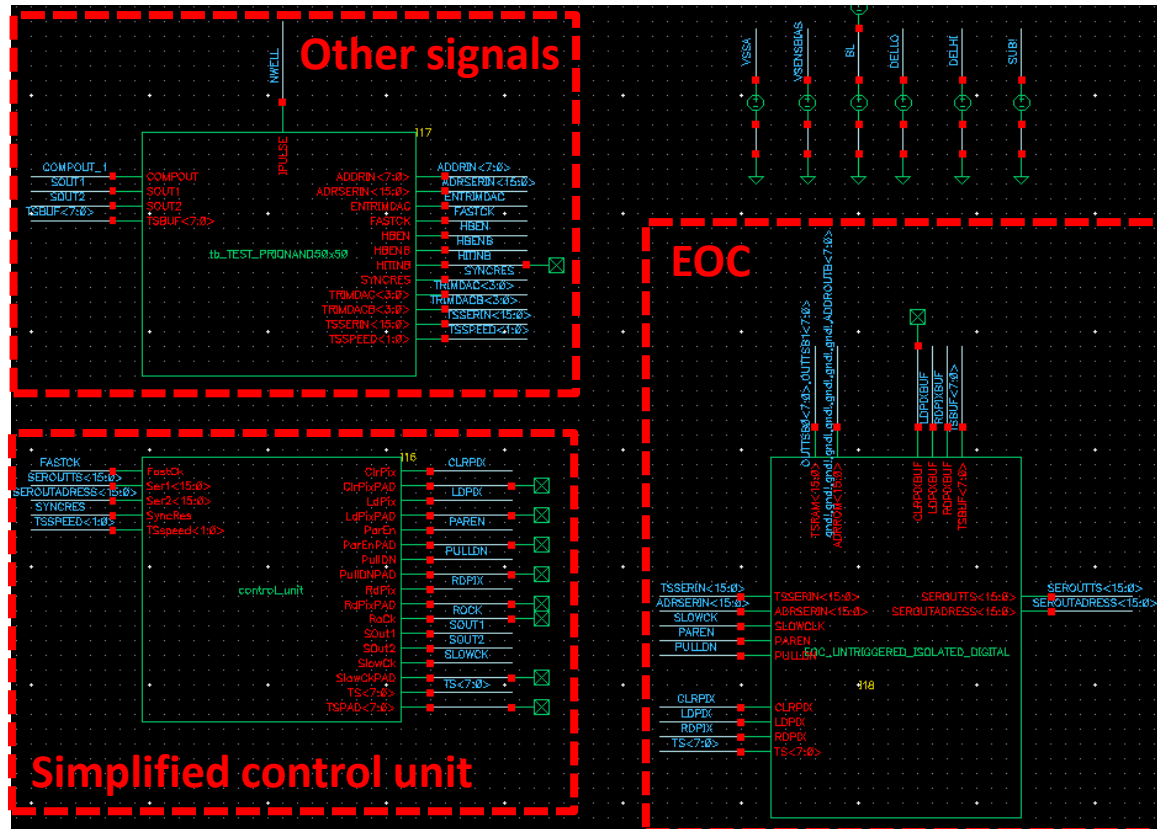
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- **ADDROUTB<7:0>, OUTTSB0<7:0> and OUTTSB1<7:0>** are sent from the pixel output to the EOC input



- There is one EOC circuit per column in the matrix (so, one EOC circuit in this testbench)



Virtuoso® Hierarchy Editor Editing: (LFRUN2_TEST_GEN_2019_RAIMON TEST_PRIONAND50X50_4PIXELS config)

File Edit View Plugins Help cadence

Top Cell Global Bindings

Library: LFRUN2_TEST_GEN_2019_RAIMON
Cell: TEST_PRIONAND50X50_4PIXELS
View: schematic

Open Edit ADE L

Library List: basic analogLib LFRUN2_TEST_GEN_2019_RAIMON
View List: verilogs veriloga behavioral functional module av_extracted schematic spectre symbol
Stop List: symbol spectre
Constraint List:

Table View Tree View

Cell Bindings

Library	Cell	View Found	View To Use	Inherited View List
LFRUN2	BUF_X16_ISOLATED_DIGITAL_LV	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2	BUF_X1_ISOLATED_DIGITAL_LV	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2	DFS_X1_ISOLATED_DIGITAL_LV	schematic	schematic	verilogs veriloga behavioral functional module av_extract...
LFRUN2	EOC_1BIT_CELL_INV_ISOLATED_DIGITAL_LV	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2	EOC_1BIT_CELL_ISOLATED_DIGITAL_LV	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2	EOC_UNTRIGGERED_ISOLATED_DIGITAL	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2	INV_X1_ISOLATED_DIGITAL_LV	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	1_MIRROR_VPBIAS	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	2_MIRROR_VBLR	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	3_MIRROR_VNCASC	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	4_MIRROR_VNSF	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	5_MIRROR_VN_1102	av_extracted		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	6_MIRROR_VPFB	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	7_MIRROR_VNSENSBIAS	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	8_MIRROR_VPTRIM	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	9_MIRROR_VNCOMP	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	BIAS_BLOCK_MODEL	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	BiasBlock_des_cap	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_BIAS_BLOCK	CURRENT_SOURCE	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_PIXELS	PIXELFEI3_PRIONAND_50x50	av_extracted	av_extracted	verilogs veriloga behavioral functional module av_extract...
LFRUN2_PIXELS	PIXELFEI3_PRIONOR_50x50	av_extracted	av_extracted	verilogs veriloga behavioral functional module av_extract...
LFRUN2_TEST_GEN_2019_RAIMON	BUF_XX20	functional		verilogs veriloga behavioral functional module av_extract...
LFRUN2_TEST_GEN_2019_RAIMON	ClkReset	verilogs		verilogs veriloga behavioral functional module av_extract...
LFRUN2_TEST_GEN_2019_RAIMON	SENSOR_FM_NEW	verilogs		verilogs veriloga behavioral functional module av_extract...
LFRUN2_TEST_GEN_2019_RAIMON	SlowClockGen	functional		verilogs veriloga behavioral functional module av_extract...
LFRUN2_TEST_GEN_2019_RAIMON	TEST_PRIONAND50X50_4PIXELS	schematic		verilogs veriloga behavioral functional module av_extract...
LFRUN2_TEST_GEN_2019_RAIMON	control_unit	functional		verilogs veriloga behavioral functional module av_extract...
LFRUN2_TEST_GEN_2019_RAIMON	tb_TEST_PRIONAND50x50	verilogs		verilogs veriloga behavioral functional module av_extract...
analogLib	cap	spectre		verilogs veriloga behavioral functional module av_extract...
analogLib	pcapacitor	spectre		verilogs veriloga behavioral functional module av_extract...
analogLib	presistor	schematic		verilogs veriloga behavioral functional module av_extract...
analogLib	res	spectre		verilogs veriloga behavioral functional module av_extract...
analogLib	vdc	spectre		verilogs veriloga behavioral functional module av_extract...

Namespace: CDBA Filters: OFF Update: Needed

1(3) >



ADE L (6) - LFRUN2_TEST_GEN_2019_RAEMON TEST_PRIONAND50X50_4PIXELS_V2 config

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help

Design Variables

Name	Value
1 BL	900m
2 DELHI	400m
3 DELLO	1.2
4 N_BLR	47
5 N_VN	8
6 N_VNCASC	12
7 N_VNCOMP	17
8 N_VNFB	32
9 N_VNSENSBIAS	16
10 N_VNSF	24
11 N_VPBIAS	26
12 N_VPFB	32
13 N_VPTRIM	30
14 VDD	1.8
15 VHV	-60
16 VSENSBIAS	1.8
17 VSSA	1.5
18 VTH	50m
19 V_PULSE	1.8
20 electrons	587n

Analyses

Type	Enable	Arguments
1 tran	<input checked="" type="checkbox"/>	0 1m conservative

Outputs

Name/Signal/Expr	Value	Plot	Save	Save
1 0_Charge_electrons	4.031K	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
2 1_Charge_electrons_NWELL	-4.432K	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
3 2_Power_VDDA	3.2u	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
4 AMPOUT		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
5 SFOUT		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
6 COMPOUT_1		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
7 COMPOUT_2		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
8 HITOUT_1		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
9 HITOUT_2		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
10 LE		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
11 TE		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
12 I1/I0/WRINTLEB		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
13 I1/I0/WRINTTEB		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
14 I1/I0/RDINTB		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
15 ADDR0UTB<7>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
16 ADDR0UTB<6>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
17 ADDR0UTB<5>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
18 ADDR0UTB<4>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
19 ADDR0UTB<3>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
20 ADDR0UTB<2>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
21 ADDR0UTB<1>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
22 ADDR0UTB<0>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
23 SER0UTADDRESS<15>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
24 SER0UTADDRESS<14>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
25 SER0UTADDRESS<13>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes
26 SER0UTADDRESS<12>		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes

I plot the address of the pixel (that sees the particle hit) at

- pixel output
- EOC output,

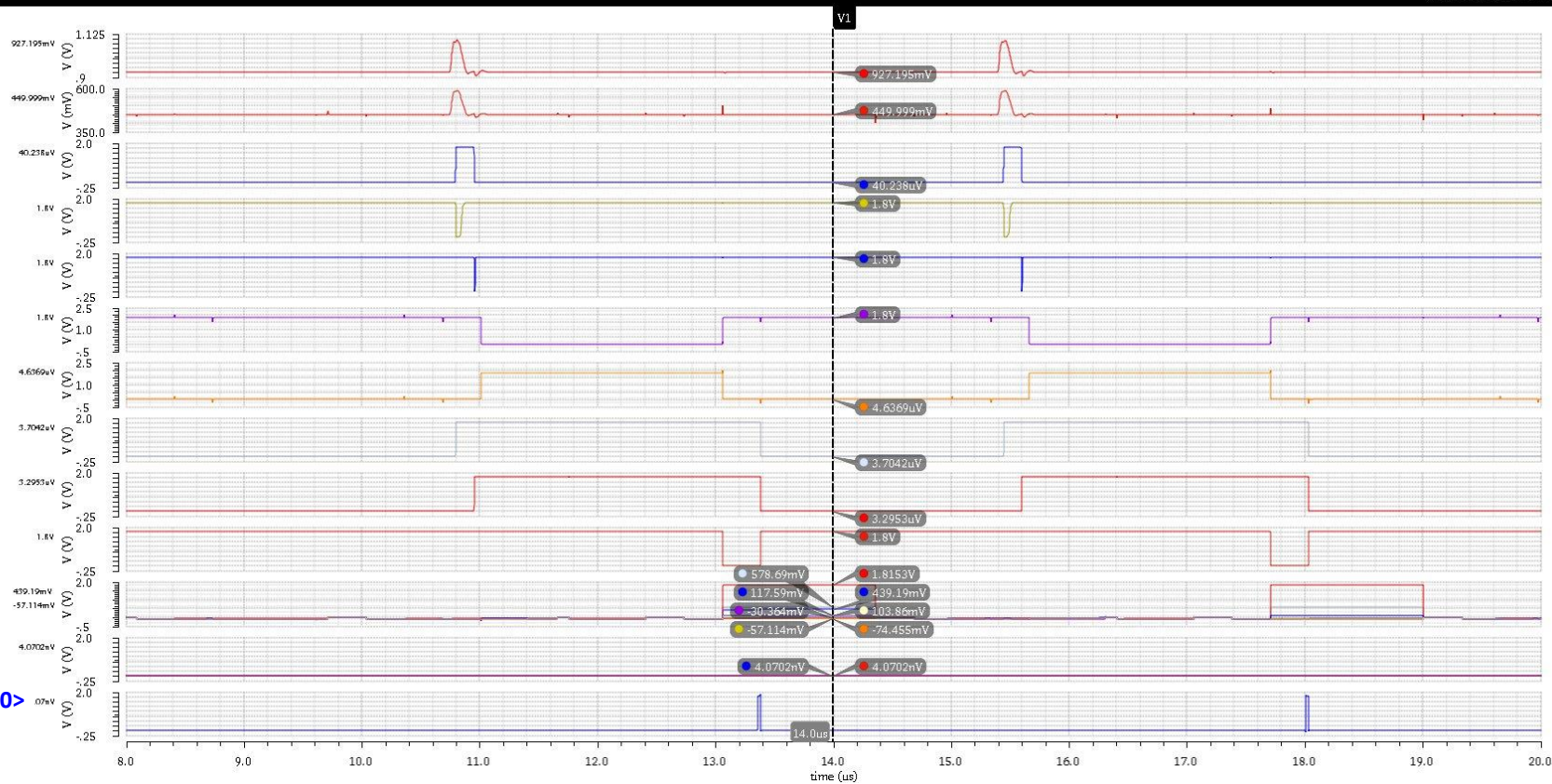
but not at the CU output.

Readout speed does not play a role in these simulations.



Transient Response

- AMPOUT
- SFOUT
- COMPOUT
- LE
- TE
- HITOUT_1
- HITOUT_2
- WRINTLEB
- WRINTTEB
- RDINTB
- ADDRROUTB
- SEROUTADDRESS <15:1>
- SEROUTADDRESS<0>





ADDRROUTB<7:0>

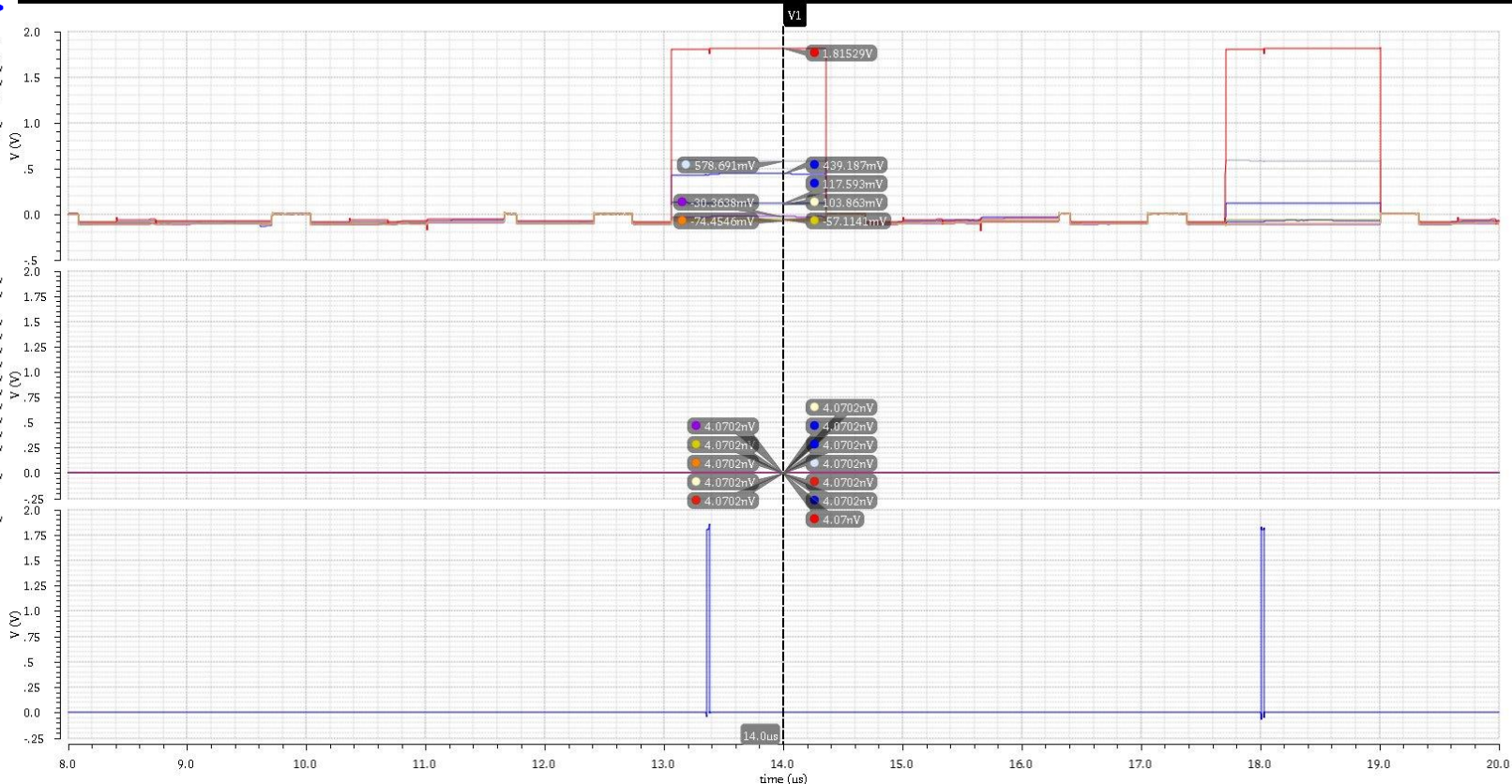
ADDRROUTB<7>	439.187mV
ADDRROUTB<2>	117.593mV
ADDRROUTB<3>	-57.1141mV
ADDRROUTB<5>	-30.3638mV
ADDRROUTB<1>	578.691mV
ADDRROUTB<0>	1.81529V
ADDRROUTB<4>	-74.4546mV
ADDRROUTB<6>	103.863mV

SEROUTADDRESS<15:1>

SEROUTADDRESS<15>	4.0702nV
SEROUTADDRESS<14>	4.0702nV
SEROUTADDRESS<7>	4.07nV
SEROUTADDRESS<15>	4.0702nV
SEROUTADDRESS<11>	4.0702nV
SEROUTADDRESS<4>	4.0702nV
SEROUTADDRESS<8>	4.0702nV
SEROUTADDRESS<5>	4.0702nV
SEROUTADDRESS<10>	4.0702nV
SEROUTADDRESS<9>	4.0702nV
SEROUTADDRESS<6>	4.0702nV
SEROUTADDRESS<12>	4.0702nV
SEROUTADDRESS<2>	4.0701nV
SEROUTADDRESS<1>	4.07nV
SEROUTADDRESS<3>	4.0702nV

SEROUTADDRESS<0>

SEROUTADDRESS<0>	4.07nV
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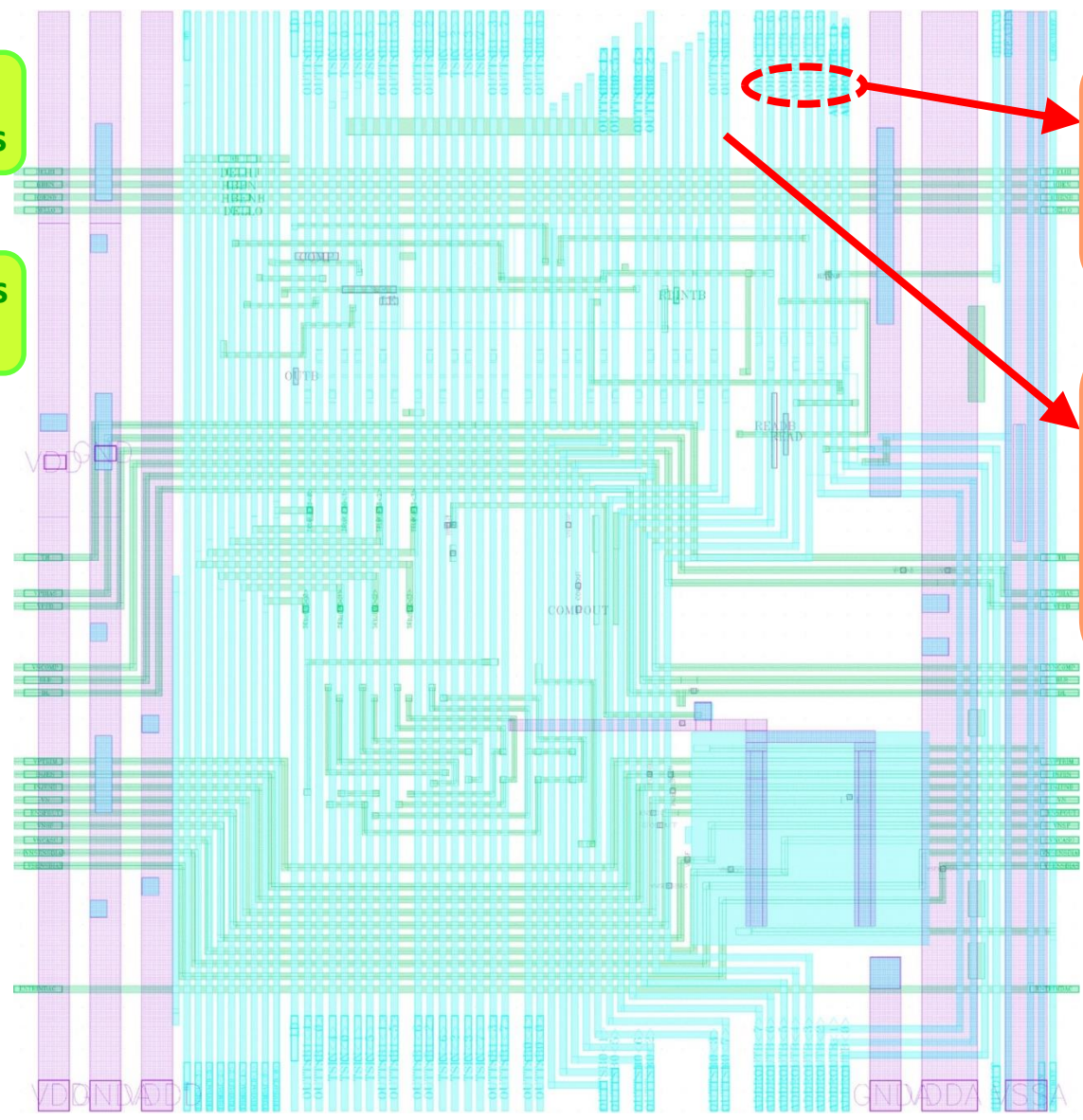
- There is some coupling between neighbouring lines: ADDRROUTB<0> = 1.8 V and ADDRROUTB<1> = 0.57 V (ADDRROUTB<1> should be 0 V, as ADDRROUTB = <00000001>)



Pixel layout

I only show the metal routing lines

Metal routing lines = 0.32 μm



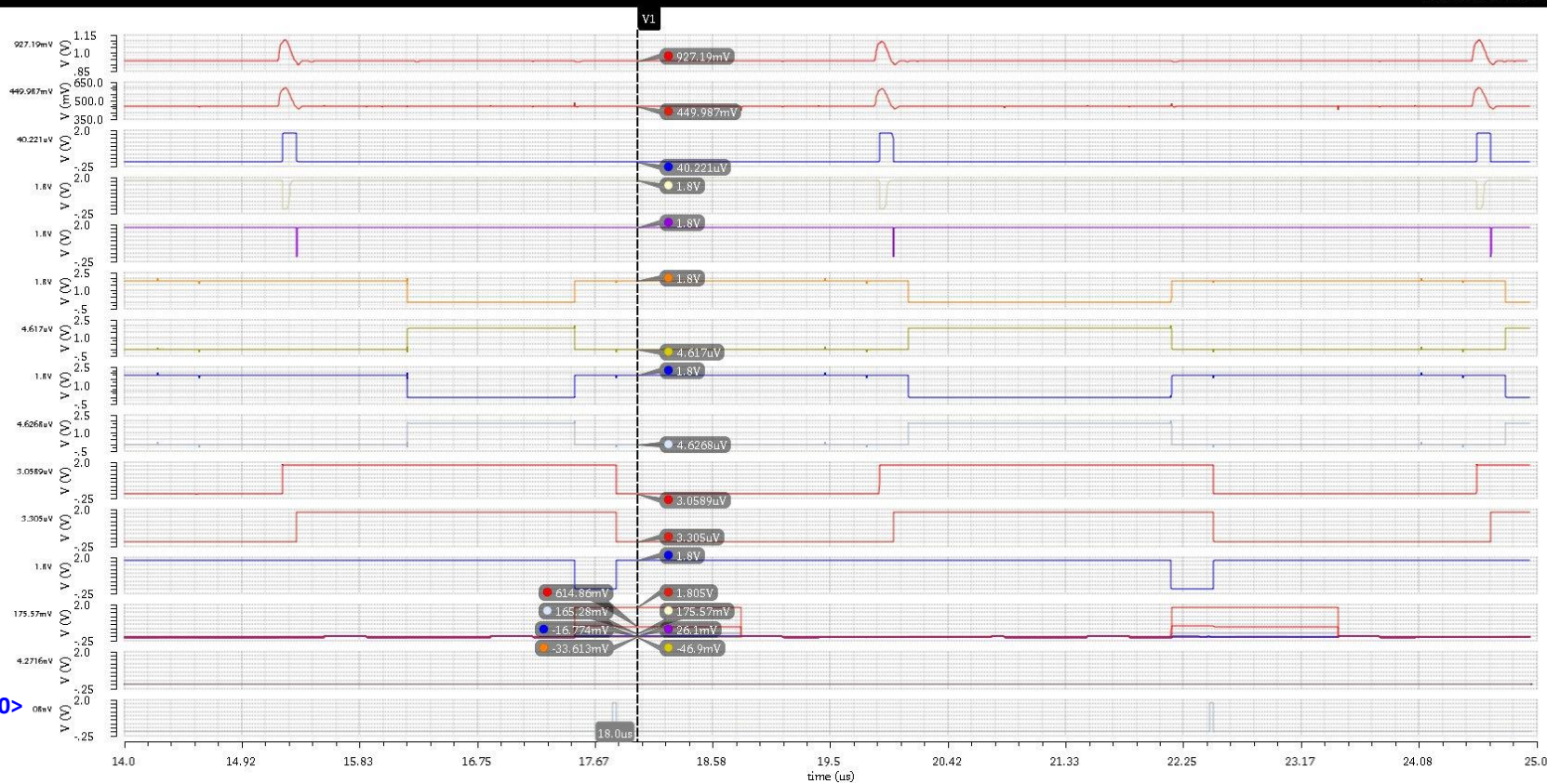
These lines are ADDROUTB<7:0> (7 = left, 0 = right). Spacing between them is 0.32 μm.

This line is OUTTSB0<7> (time-stamp). There is xtalk between OUTTSB0<7> and ADDROUTB<7>.



Transient Response

- AMPOUT
- SFOUT
- COMPOUT
- LE
- TE
- HITOUT_1
- HITOUT_2
- HITOUT_3
- HITOUT_4
- WRINTLEB
- WRINTTEB
- RDINTB
- ADDROUTB
- SEROUTADDRESS <15:1>
- SEROUTADDRESS<0>



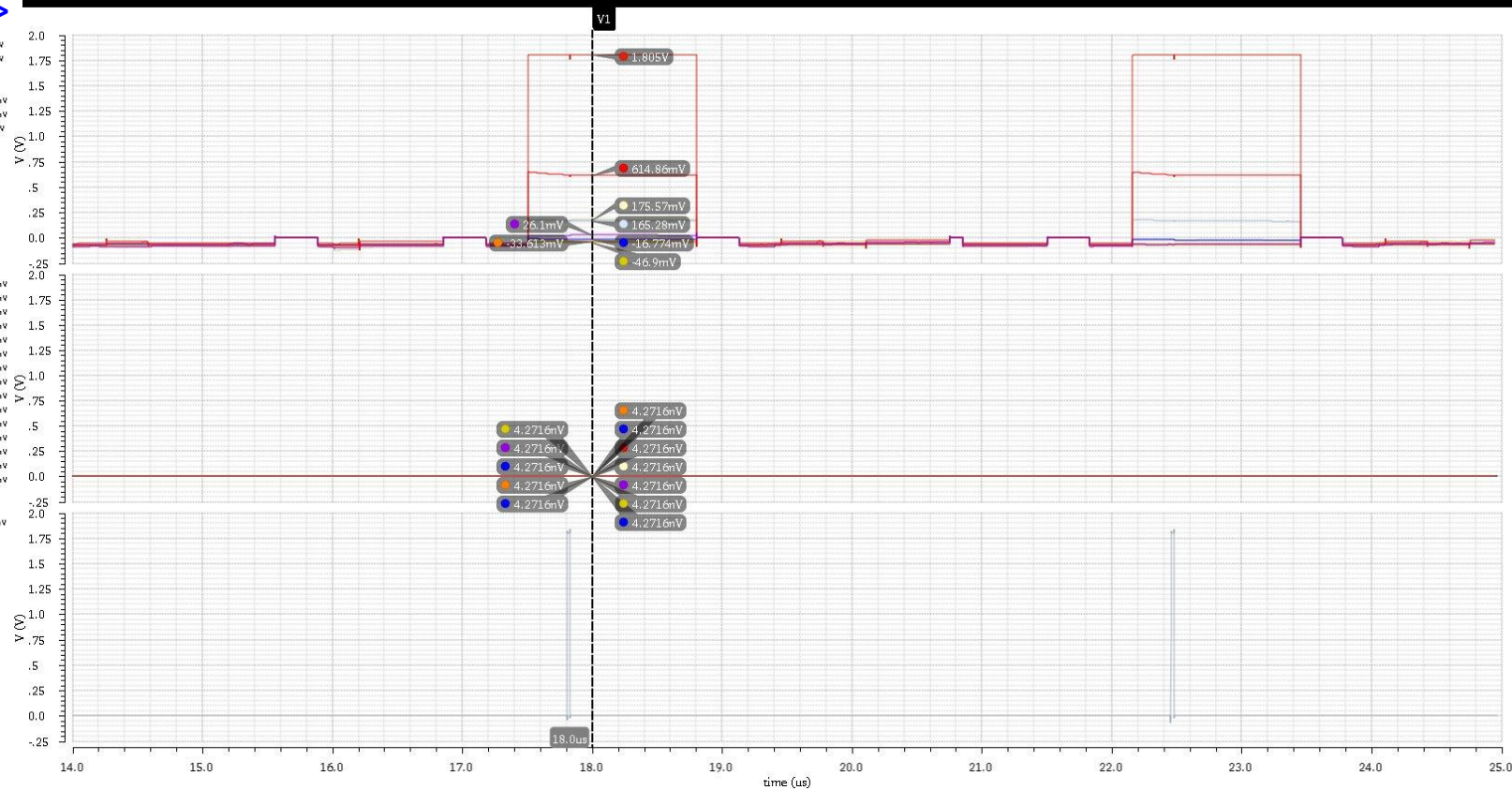
ADDRROUTB<7:0>

/ADDRROUTB<7>	175.57mV
/ADDRROUTB<2>	165.28mV
/ADDRROUTB<0>	1.809V
/ADDRROUTB<4>	-46.9mV
/ADDRROUTB<3>	-16.774mV
/ADDRROUTB<5>	-33.613mV
/ADDRROUTB<1>	614.86mV
/ADDRROUTB<6>	26.1mV

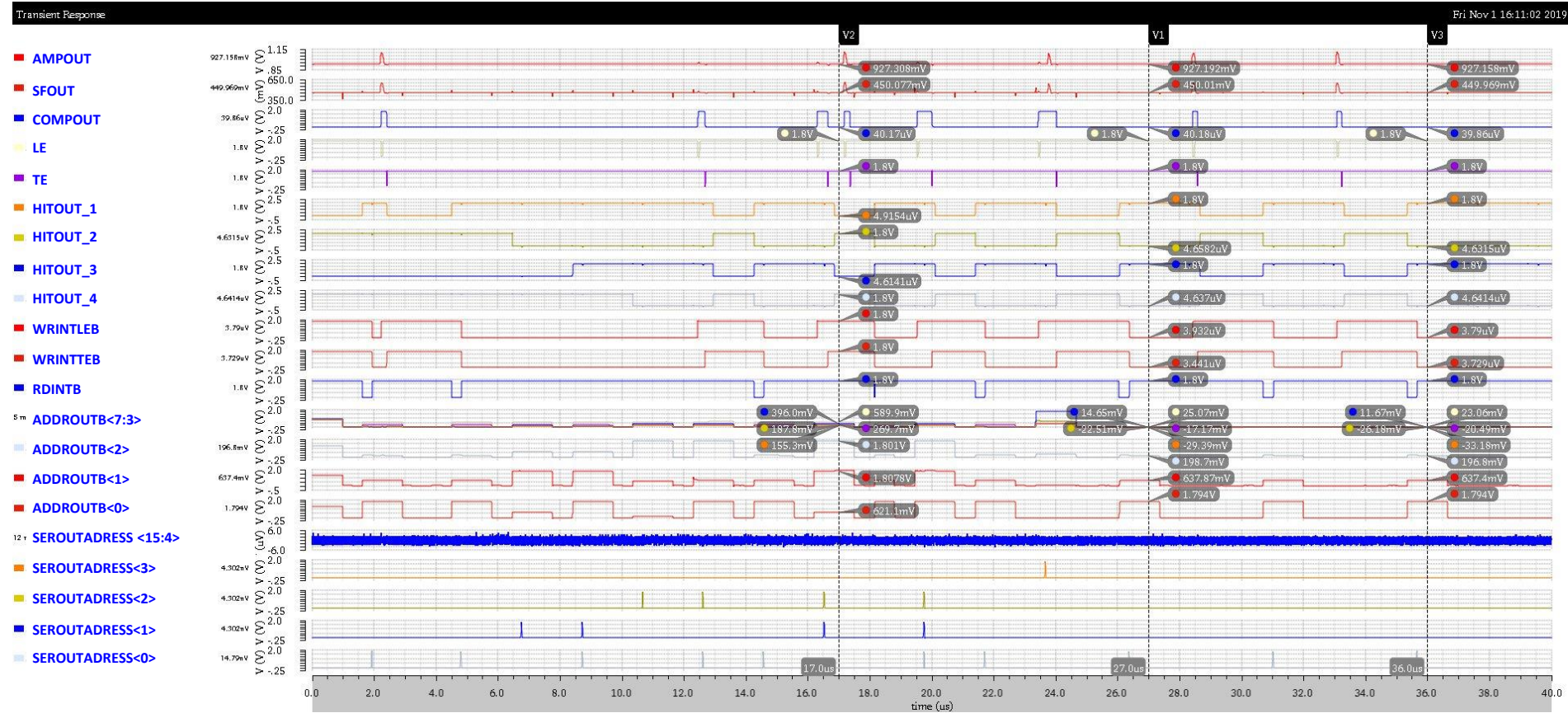
SEROUTADDRESS<15:1>

/SFRROUTADRFBSS<15>	4.2716V
/SFRROUTADRFBSS<9>	4.2716V
/SFRROUTADRFBSS<10>	4.2716V
/SFRROUTADRFBSS<15>	4.2716V
/SFRROUTADRFBSS<4>	4.2716V
/SFRROUTADRFBSS<6>	4.2716V
/SFRROUTADRFBSS<2>	4.2716V
/SFRROUTADRFBSS<11>	4.2716V
/SFRROUTADRFBSS<14>	4.2716V
/SFRROUTADRFBSS<8>	4.2716V
/SFRROUTADRFBSS<5>	4.2716V
/SFRROUTADRFBSS<3>	4.2716V
/SFRROUTADRFBSS<7>	4.2716V
/SFRROUTADRFBSS<1>	4.2716V
/SFRROUTADRFBSS<12>	4.2716V
/SFRROUTADRFBSS<0>	107.08mV

SEROUTADDRESS<0>



- The voltage of ADDRROUTB<1> increases with the number of pixels in the simulation!
- But still it is not enough to flip the bit, as SEROUTADDRESS<1> = '0'.



- I don't understand what is going on from 0 to 24 - 26 μ s. It seems some sort of *initial transient* (it also happens when there are less pixels, but it is a lot shorter).



ADDROUTB<7:0>

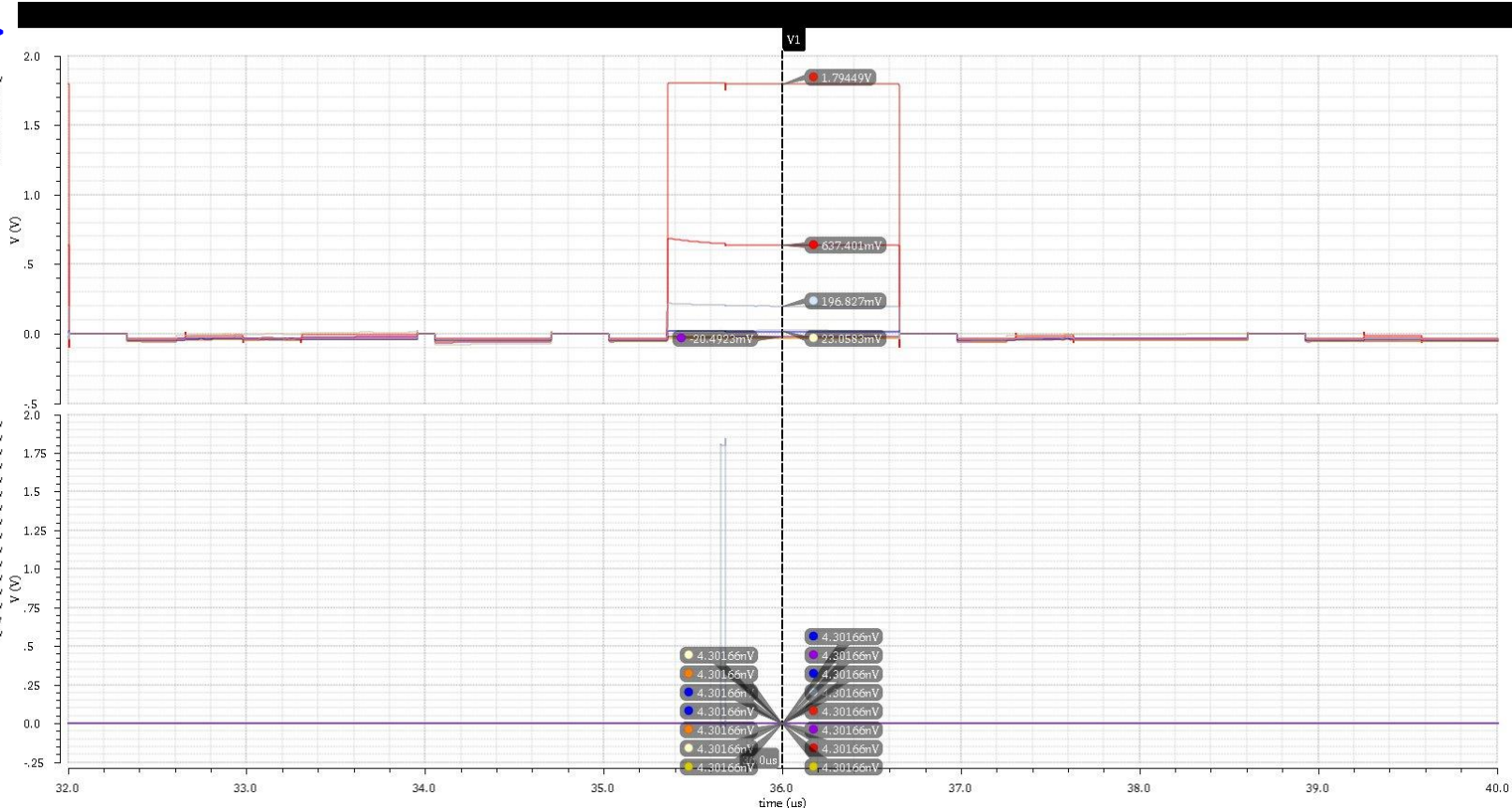
ADDROUTB<0>	1.79449V
ADDROUTB<6>	-20.4923mV
ADDROUTB<7>	23.0583mV
ADDROUTB<4>	-36.179mV
ADDROUTB<5>	-33.176mV
ADDROUTB<3>	11.6679mV
ADDROUTB<1>	637.401mV
ADDROUTB<2>	196.827mV

SEROUTADDRESS<15:1>

SEROUTADDRESS<15>	4.30166mV
SEROUTADDRESS<7>	4.30166mV
SEROUTADDRESS<6>	4.30166mV
SEROUTADDRESS<13>	4.30166mV
SEROUTADDRESS<14>	4.30166mV
SEROUTADDRESS<2>	4.30166mV
SEROUTADDRESS<12>	4.30166mV
SEROUTADDRESS<9>	4.30166mV
SEROUTADDRESS<4>	4.30166mV

SEROUTADDRESS<0>

SEROUTADDRESS<0>	14.789mV
SEROUTADDRESS<4>	4.30166mV

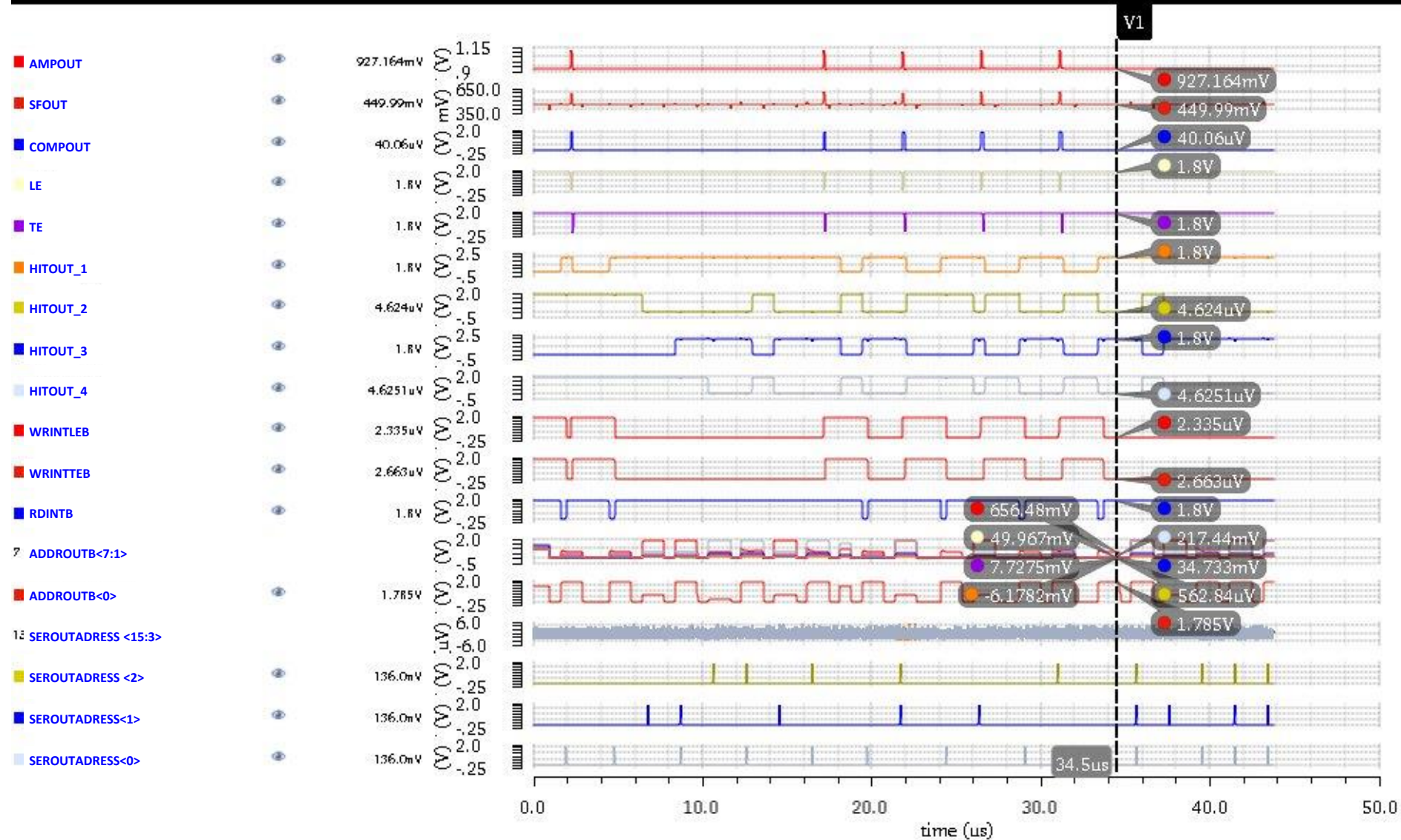


- ADDROUTB<0> = 1.8 V and ADDROUTB<1> = 0.63 V
- Still no bit flipping in SEROUTADDRESS (after the *initial transient*)



Transient Response

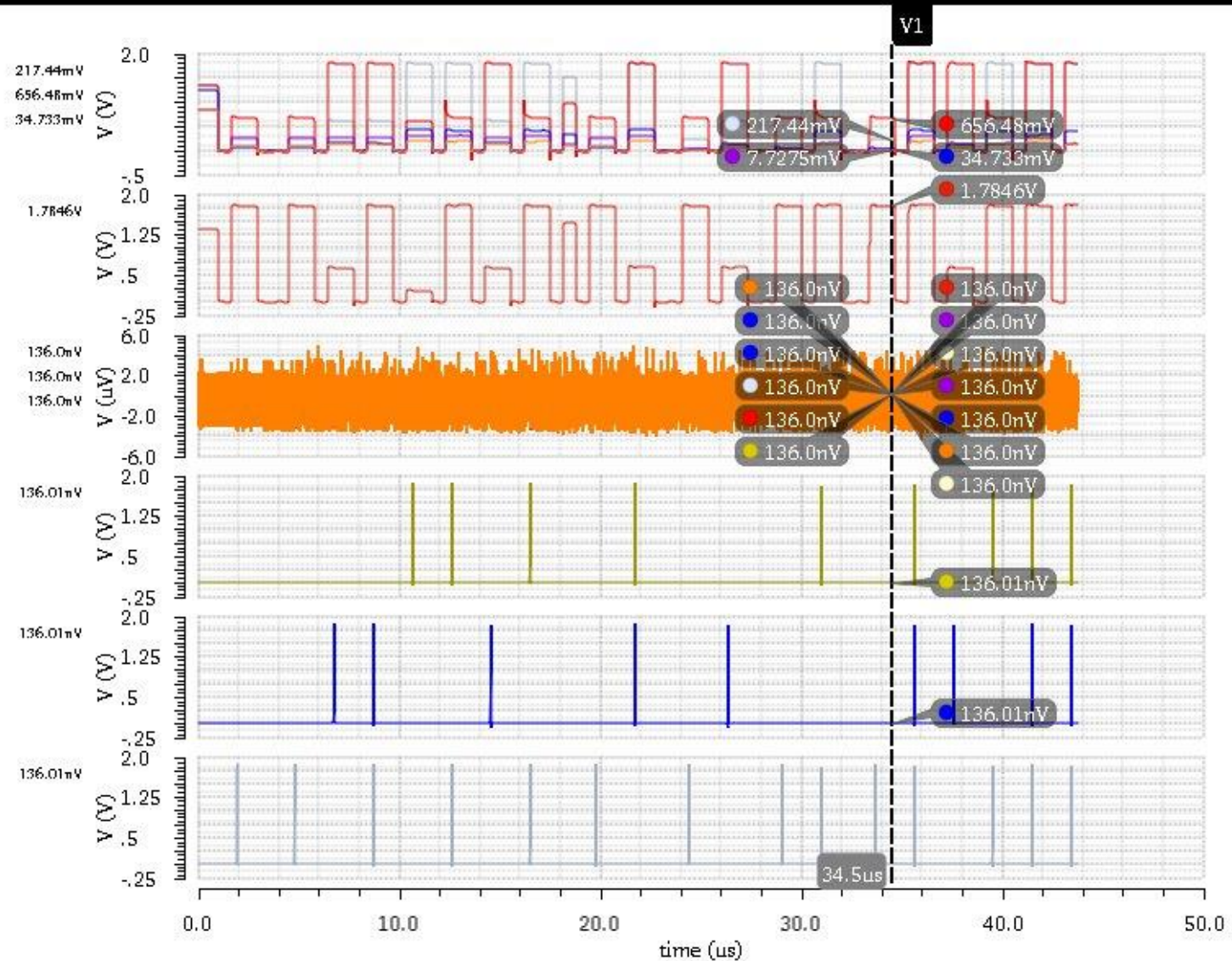
Fri Nov 1 19:21:56 2019





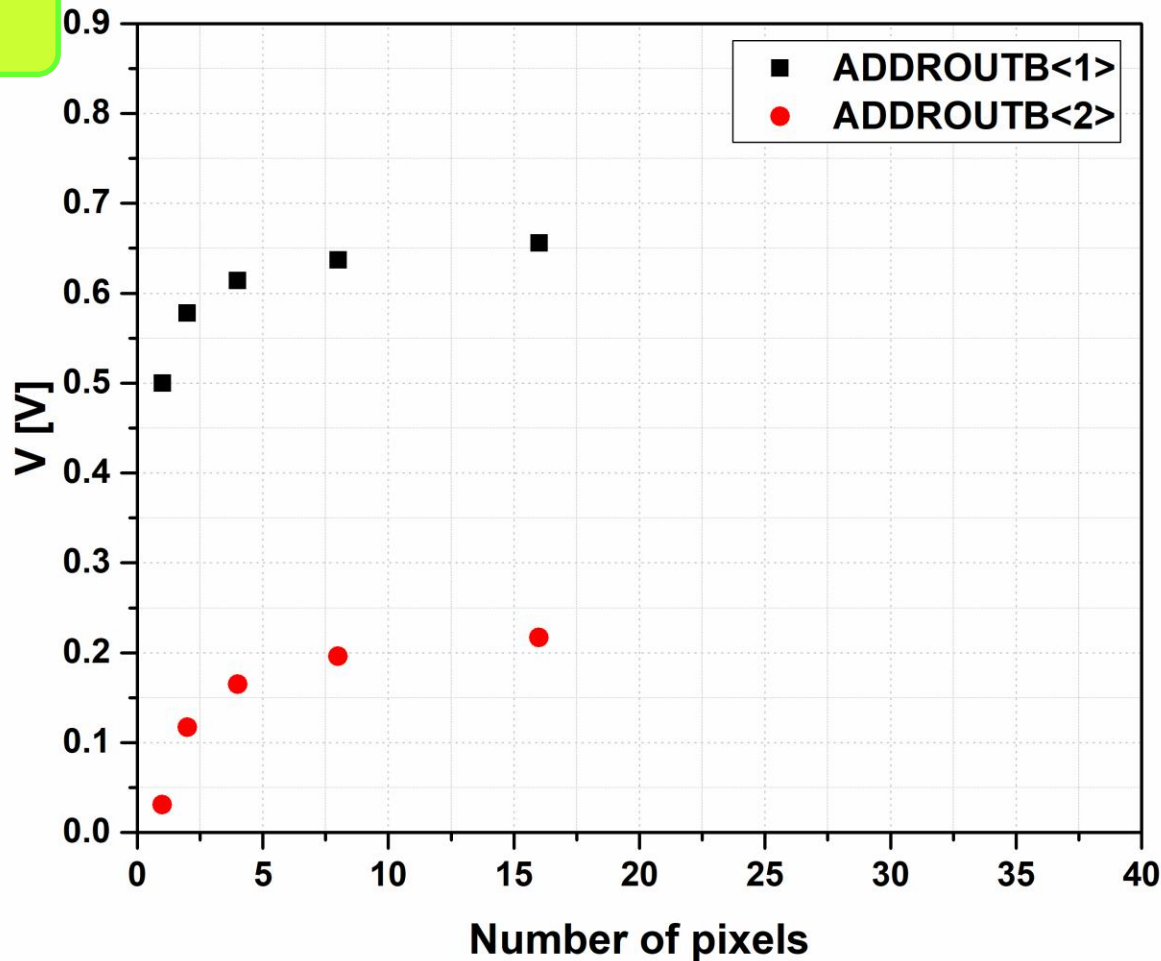
Transient Analysis

- ADDR0UTB<7:1>
- ADDR0UTB<0>
- SER0UTADDRESS<15:1>
- SER0UTADDRESS<2>
- SER0UTADDRESS<1>
- SER0UTADDRESS<0>





ADDROUTB<0> =
1.8 V



$\Delta V = \Delta Q / C$
I always inject
the same amount
of charge ($4k e^-$)
to one pixel. I
should see a
linear behaviour?