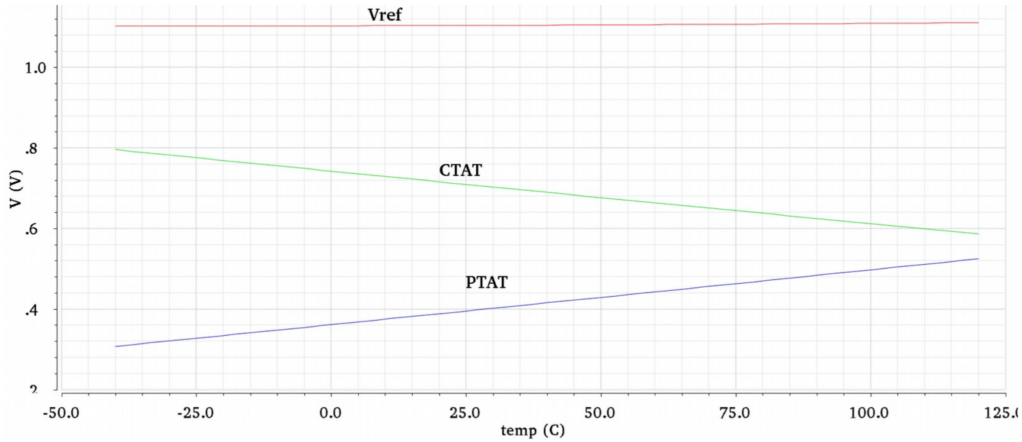
ANNUAL MEETING

HVCMOS ASIC DESIGN

28/04/21

What is a bandgap reference?

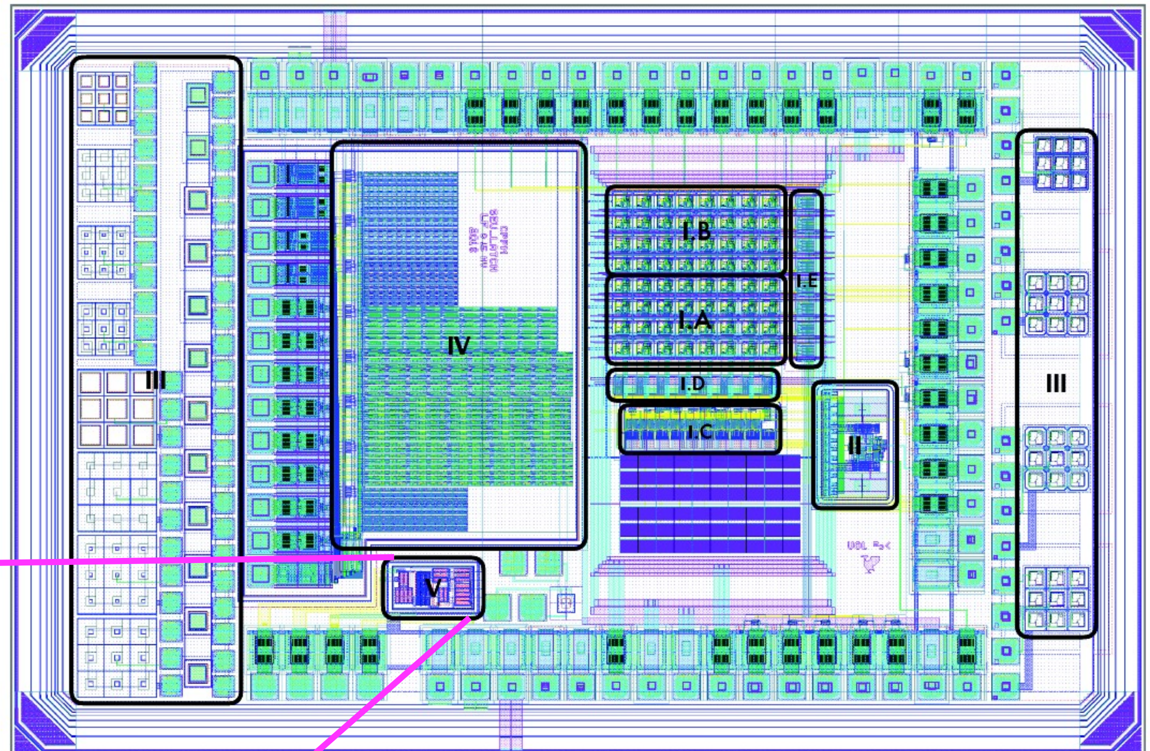
- An ideal Bandgap voltage reference generates a DC voltage that is independent of:
  - Temperature
  - Power Supply
  - Process Variations

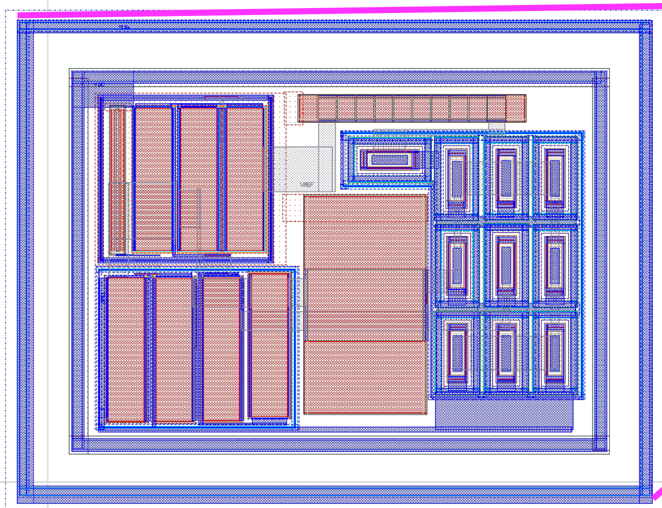


- A precise voltage reference is need for many applications including:
  - A/D and D/A Converters
  - LDO Voltage Regulators
  - Linear Regulators

RD50-MPW2 Floorplan – January 2019 Submission

I	PIXEL Matrix
II	Analog Buffer
III	Test Structures
IV	SEU Tollerant Memory
V	Bandgap

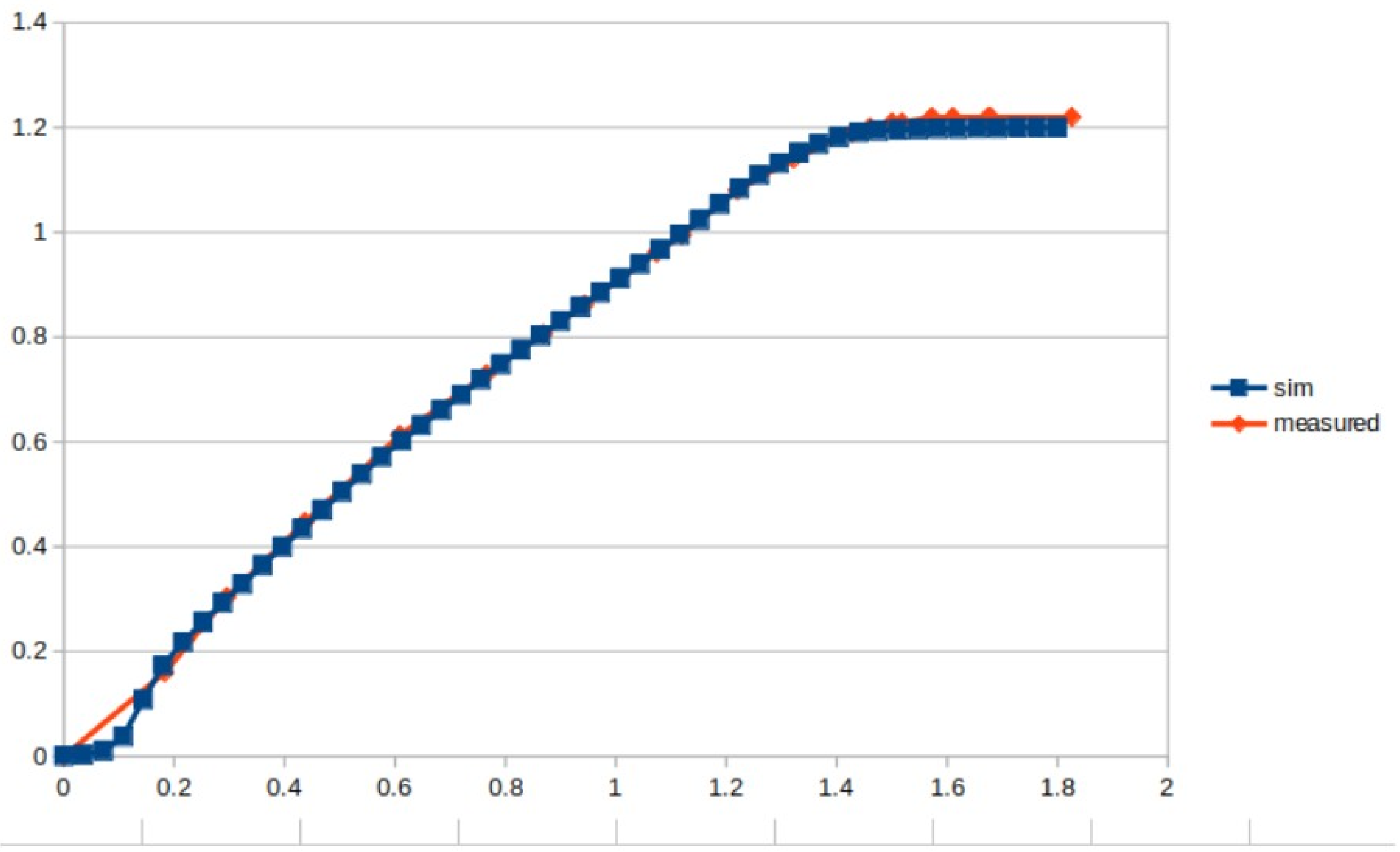




- RD50-MPW2 Submitted in January 2019
- Chip received from manufacture in February
- 2020

RD50-MPW2 MEASUREMENTS – Bandgap Reference

- Measured Results for the bandgap reference circuit designed for RD50-MPW2 show almost perfect agreement with simulated expectation
- Output voltage is extremely stable in the operating range (1.4 to 1.8 V)
- This will allow for bias voltages throughout the chip to be derived from a much more stable source than previous designs

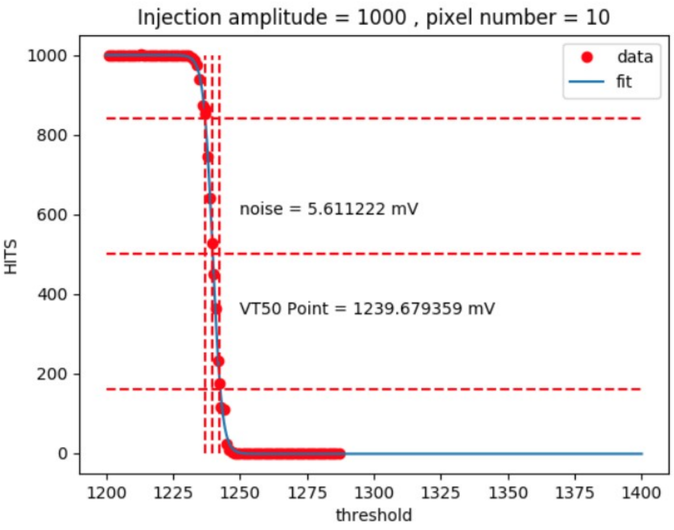


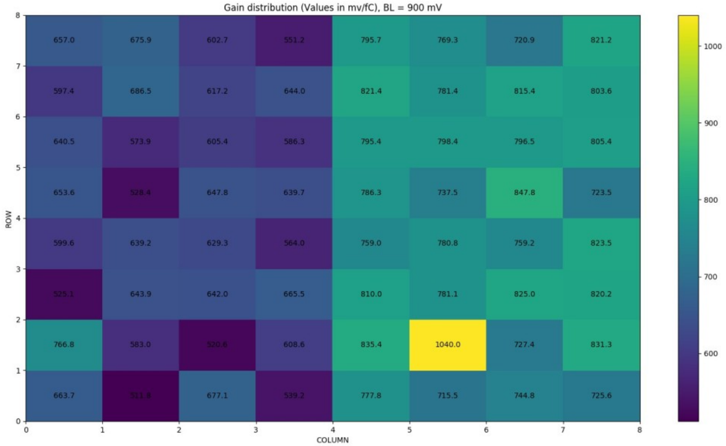
RD50-MPW2 ACTIVE PIXEL MATRIX MEASUREMENTS

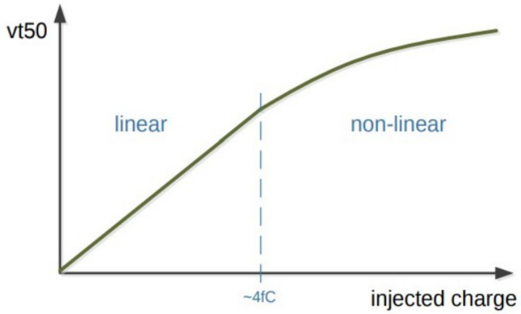
- Software and firmware developed to configure,
- readout and analyse RD50-MPW2

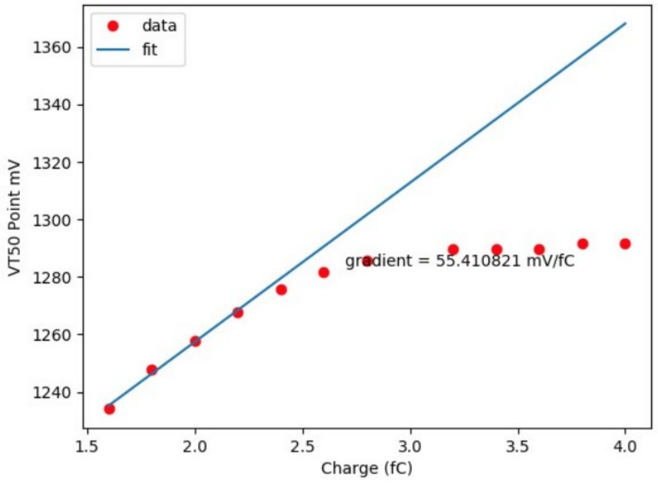
- Measurements including S-curves, Response Curves
- DAC trimming, Gain calculations and pixel to pixel gain
- and noise distributions

- MPW2 has now
- been very well
- characterised



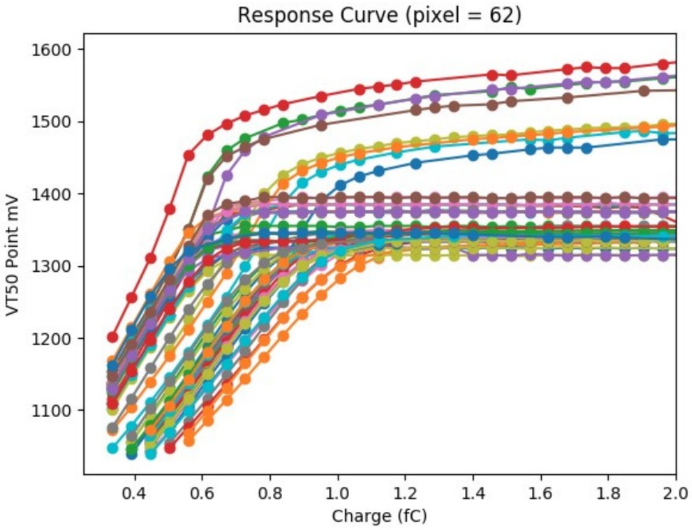


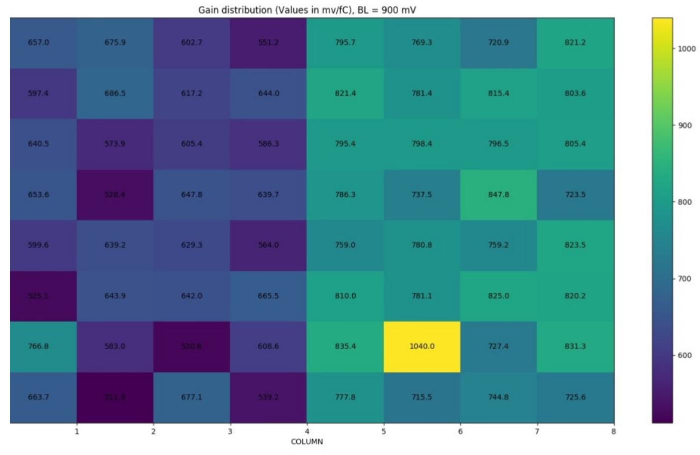


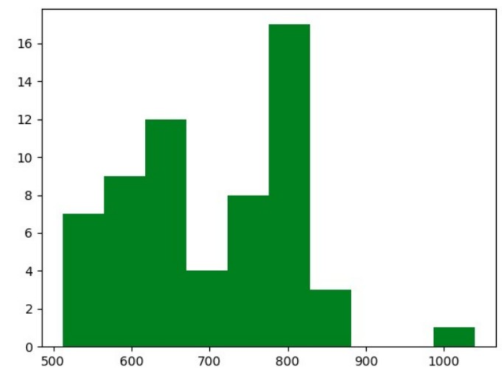


- Plotting the VT50 point of these S-curves as a function of injection amplitude gives us the gain of the pixel

RD50-MPW2 MEASUREMENTS



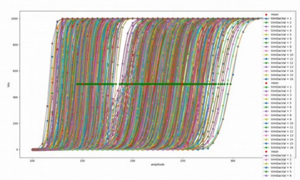




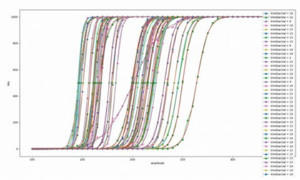
- Gain distribution shows 2 distinct patterns of gain values
  - This is expected as the matrix contains 2 flavours of pixel (switched reset and continuous) split between the right and left sides of the matrix

  - The 2 different gains can be seen represented as the gradients of the response curves (top left), the colour difference in the 2d Gain map of the matrix (middle) or the 2 peaks of the gain histogram (top right)

BEFORE SELECTION



AFTER SELECTION

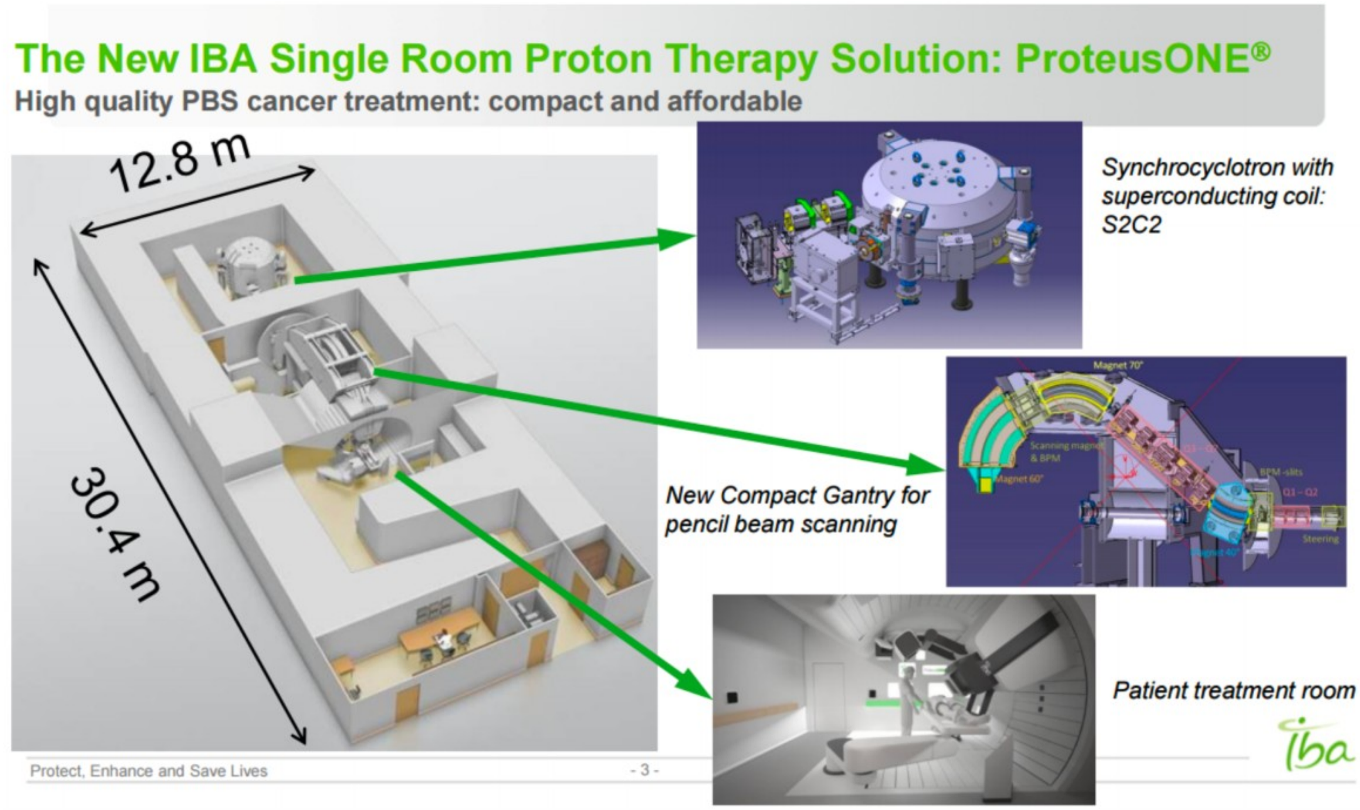


RD50-MPW2 TESTBEAM

IBA Proteus One – S2C2 synchrocyclotron characteristics

Protons delivered in bunches with a 1 kHz reputation rate

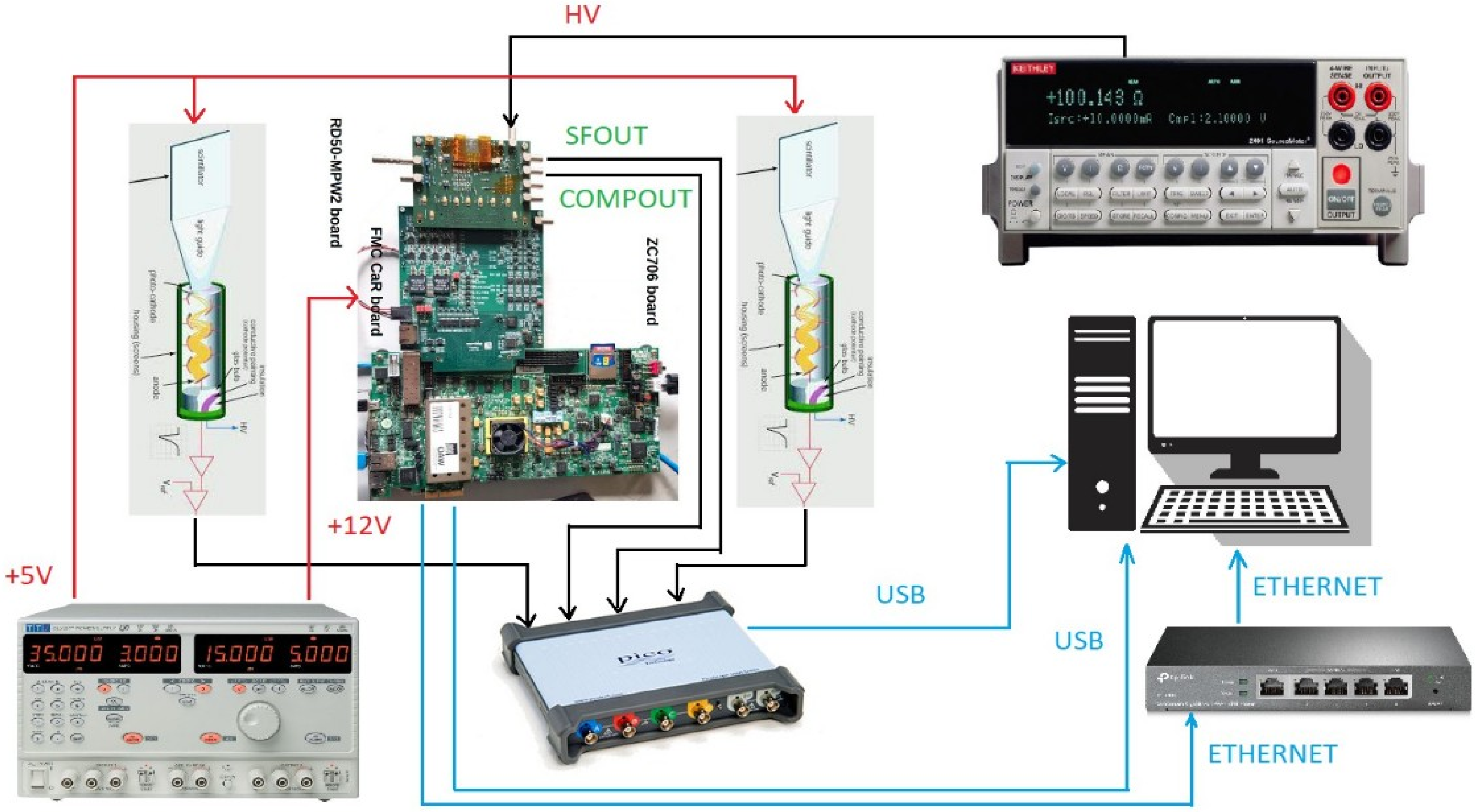
- Bunch length: 10us
- Min. Protons/s: 10^7
- Min. Protons/bunch: 10^5
- Beam energies from 70-229 MeV
- Min beam spot size: 3.5mm radius
- Gantry angles from 0 - 270deg



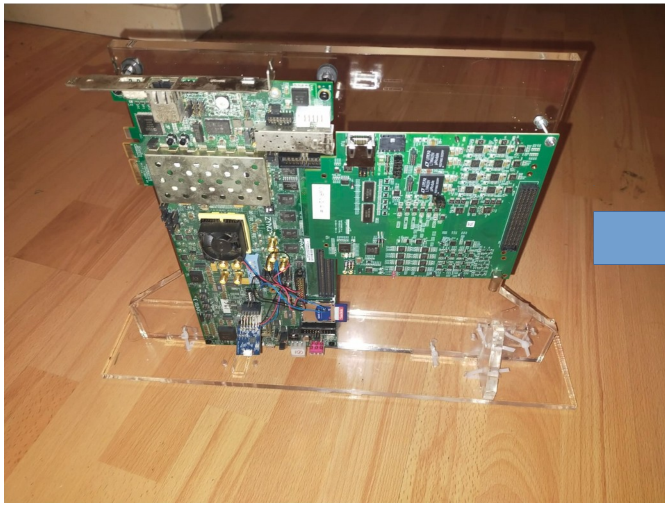
With thanks to F. Risser (IBA)

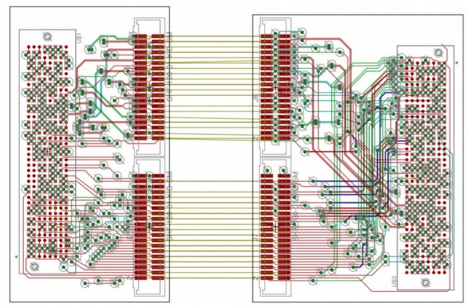
TheRutherford Cancer Centres

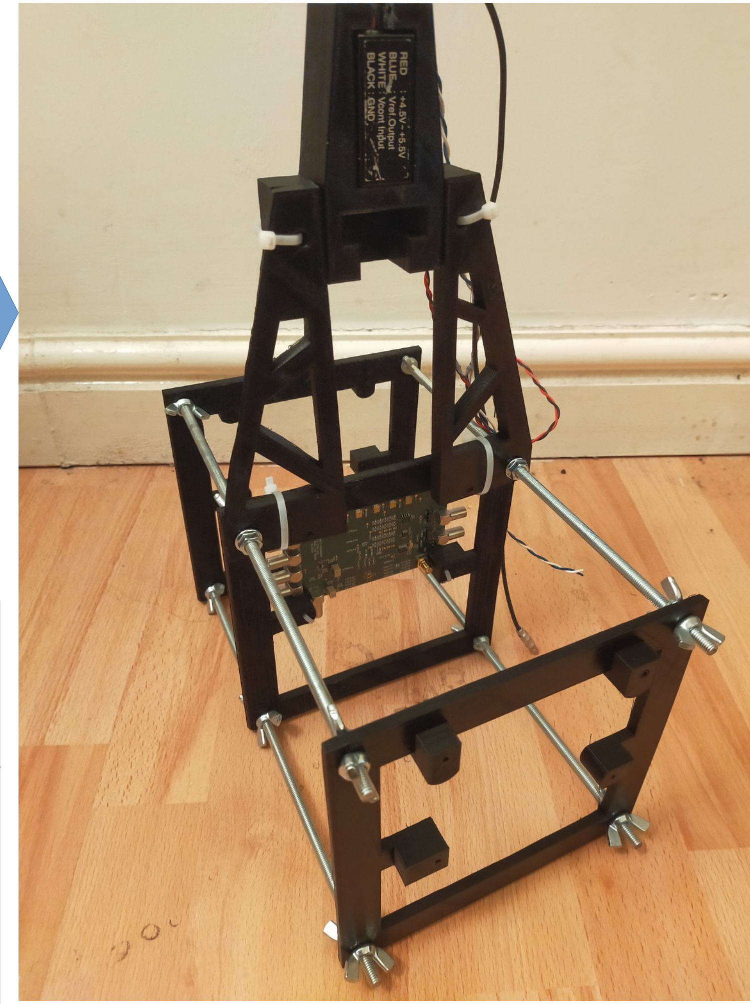
RD50-MPW2 TESTBEAM



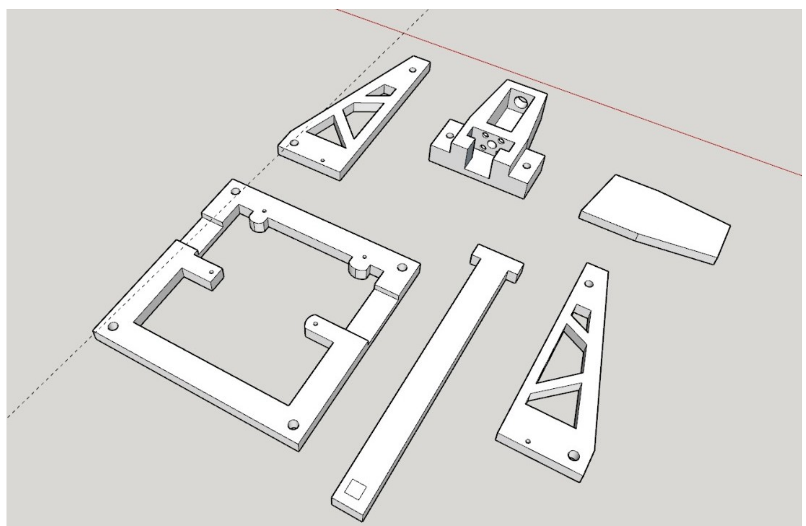
RD50-MPW2 BEAM TELESCOPE



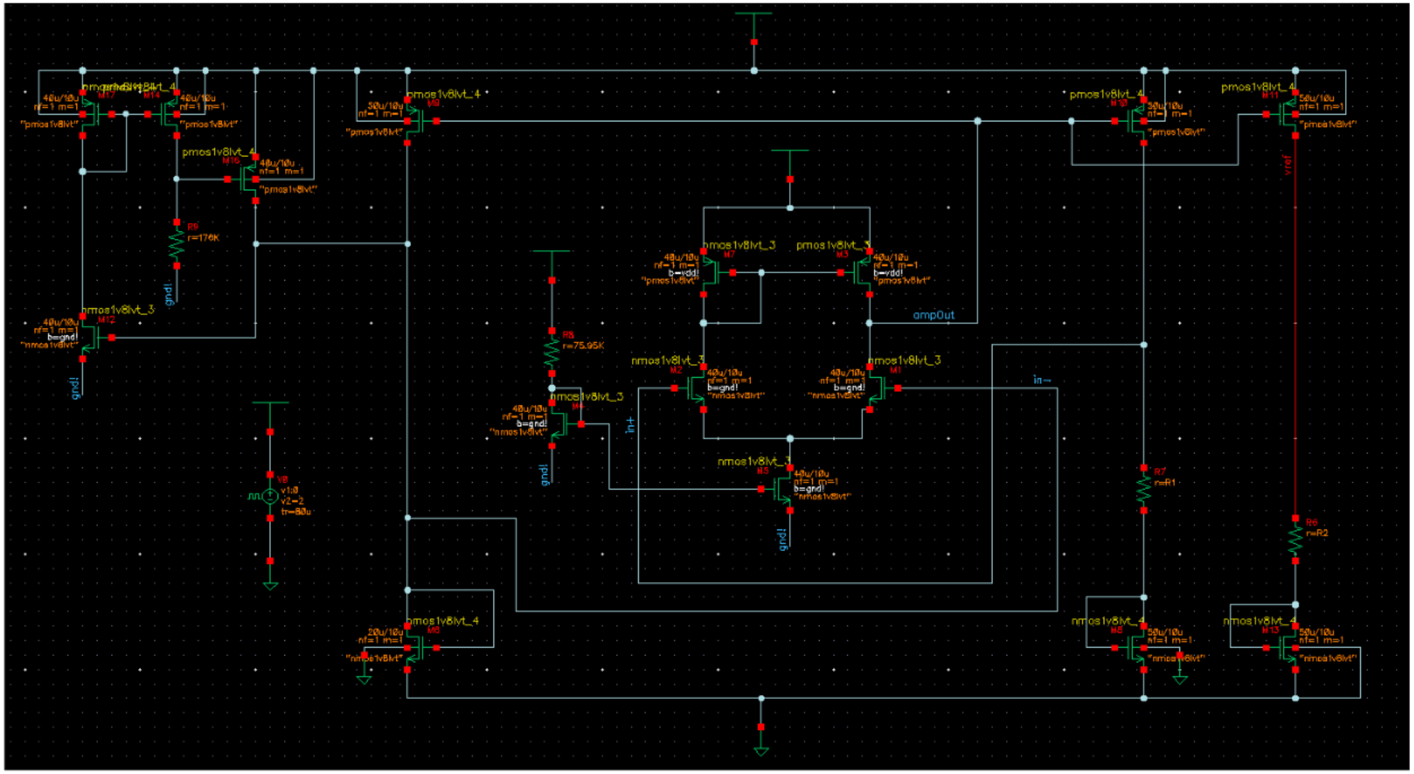




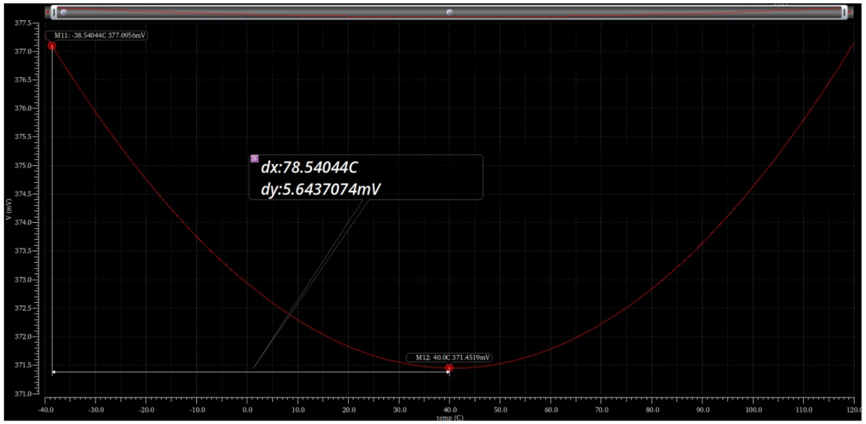
- The testbeam telescope has been designed to be 3d printed to allow the design to be modified easily

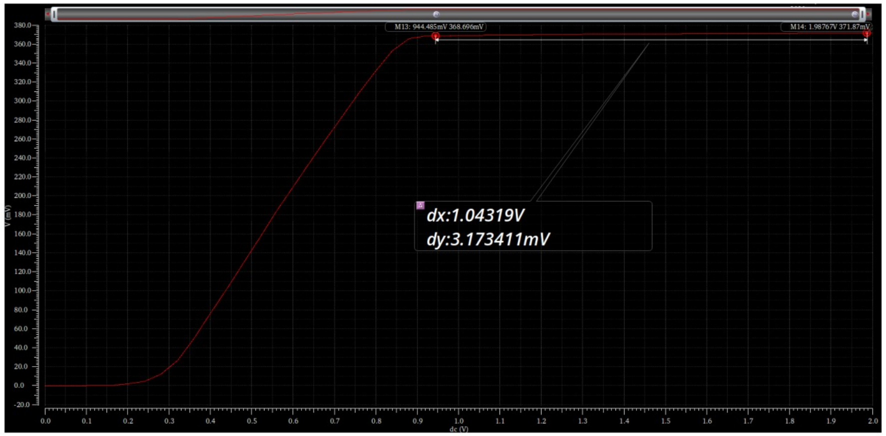


FULLY CMOS BASED BANDGAP UKRI-MPW0

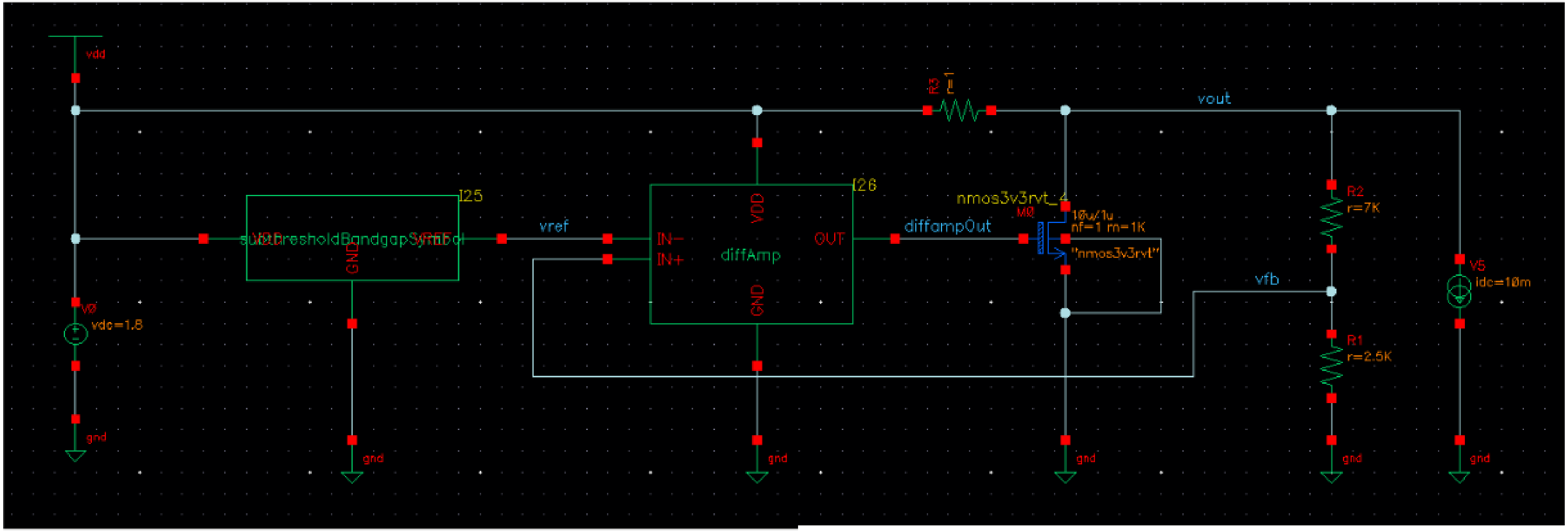


- Simulations of fully CMOS based bandgap for UKRI-MPW0 show
  - Output voltage changes by 3.17mV over the entire operating range (0.8-1.8V)
  - Output voltage changes by 5.6mV for a change in ambient temperature from -40 to +120 degrees Celcius





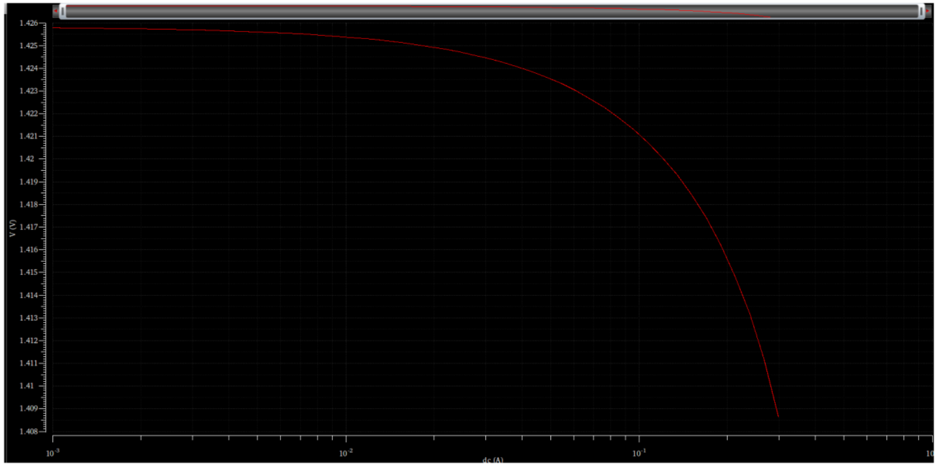
SHUNT REGULATOR UKRI-MPW0



- A Shunt regulator has also been designed
- for UKRI-MPW0 building on the success of the bandgap in RD50-MPW2

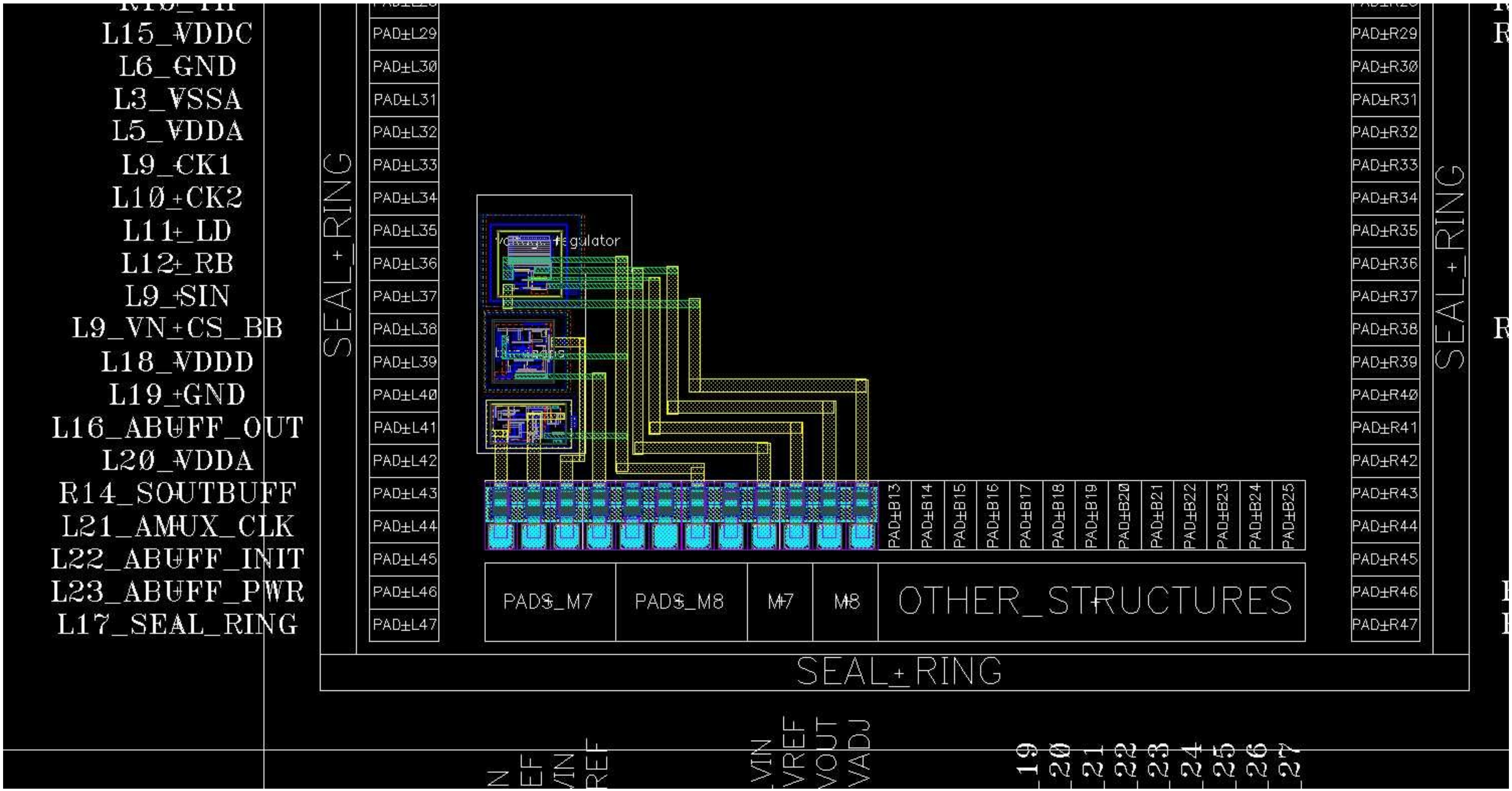
- A regulator provides not only a stable voltage, but the capability to provide significant current

- This allows power supplies to be generted on chip reducing the need for external compenents and PCB area – **reducing the material budget**



- Fully mosfet regulator set for arbitrary 1.4V ouput
- Ouput voltage changes by less than 5mV for a current draw from 0 to 100mA

PLACED AND ROUTED BLOCKS UKRI-MPW0



SUMMARY

- CHIPS SUBMITTED
  - RD50-MPW1
  - RD50-MPW2 (Designed - BJT bandgap reference)
  - UKRI-MPW0 (Designed - BJT bandgap reference , Fully CMOS bandgap reference and Shunt regulator)

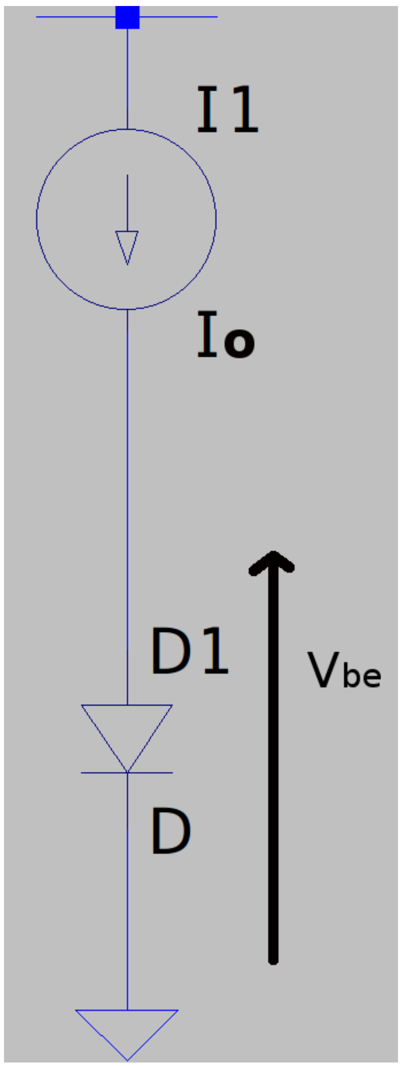
- Chips characterised
  - RD50-MPW1 – gain, noise, thresholds
  - RD50-MPW2 – gain, noise, thresholds (Testbeam planned for 10th May)

- Awaiting Delivery
  - UKRI-MPW0

- Further work –
  - Submit design for readout PCB for UKRI-MPW0
  - Write FPGA firmware for UKRI-MPW0 DAQ in VHDL and C
  - Write FPGA firmware for decode addresses for UKRI-MPW0 DAQ in VHDL
  - Write GUI to configure UKRI-MPW0 in C++
  - Confirm measurements of RD50-MPW2 with testbeam
  - Characterise UKRI-MPW0

BACKUP SLIDES FOLLOW

Design Principles

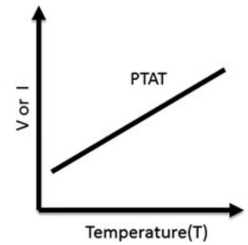


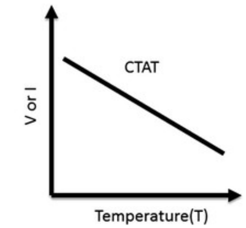
$$Io = Is \cdot [e^{Vbe/Vt} - 1]$$

$$\text{for } Ic \gg Is$$

$$Io = Is \cdot e^{Vbe/Vt}$$

$$Vbe = Vt \cdot \ln\left(\frac{Io}{Is}\right)$$





PTAT CTAT

- **CTAT (Complementary To Absolute Temperature) term in this equation dominates giving an overall CTAT nature for Vbe**

$$Io = \text{Diode Current}$$

$$Is = \text{Saturation Current}$$

$$Vt = {kT}/{q} = 25.3\,mV \text{ @ Room Temp}$$ PTAT

- **PTAT (Proportional To Absolute Temperature)**

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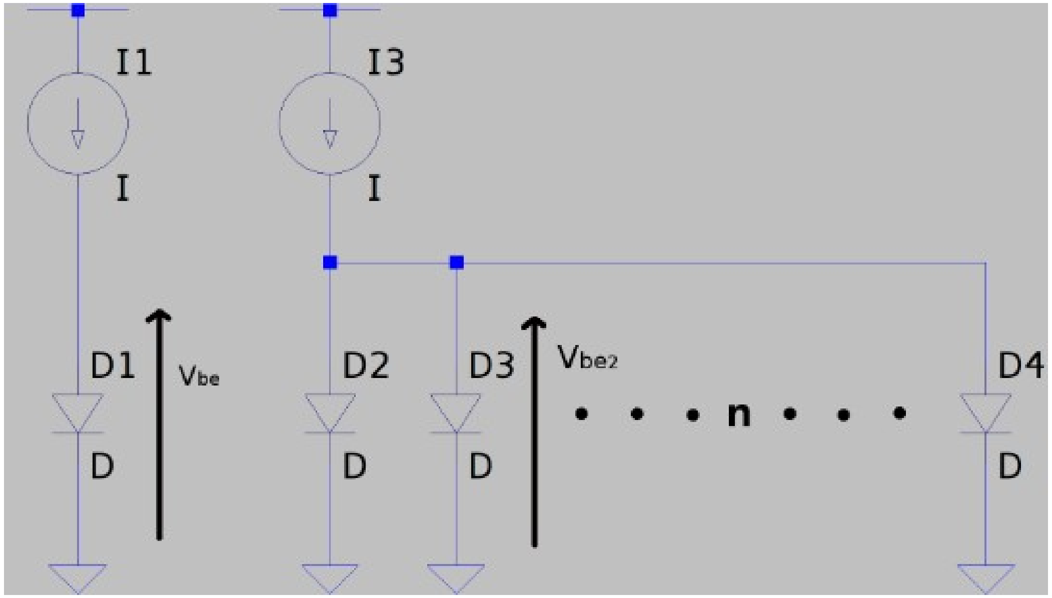
How to generate a PTAT

$$Vbe = Vt \cdot \ln\left(\frac{Io}{Is}\right)$$

- If we can cancel out this term we generate a pure PTAT



$$Vbe = Vt \cdot \ln\left(\frac{Io}{Is}\right) \qquad Vbe_2 = Vt \cdot \ln\left(\frac{Io}{Is}\right)$$

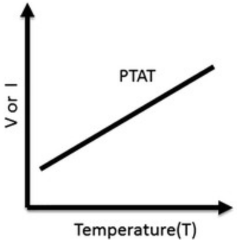
$$Vbe - Vbe_2 = Vt\left[\ln\left(\frac{Io}{Is}\right) - \ln\left(\frac{Io}{n \cdot Is}\right)\right]$$

$$\ln(a) - \ln(b) = \ln\left(\frac{a}{b}\right)$$

$$Vbe - Vbe_2 = Vt \cdot \ln\left[\left(\frac{Io \cdot n \cdot Is}{Io \cdot Is}\right)\right]$$

- Note. These equations rely on both current sources being equal. To achieve this a current mirror circuit is required

$$Vbe - Vbe_2 = Vt \cdot \ln(n) \qquad PTAT$$



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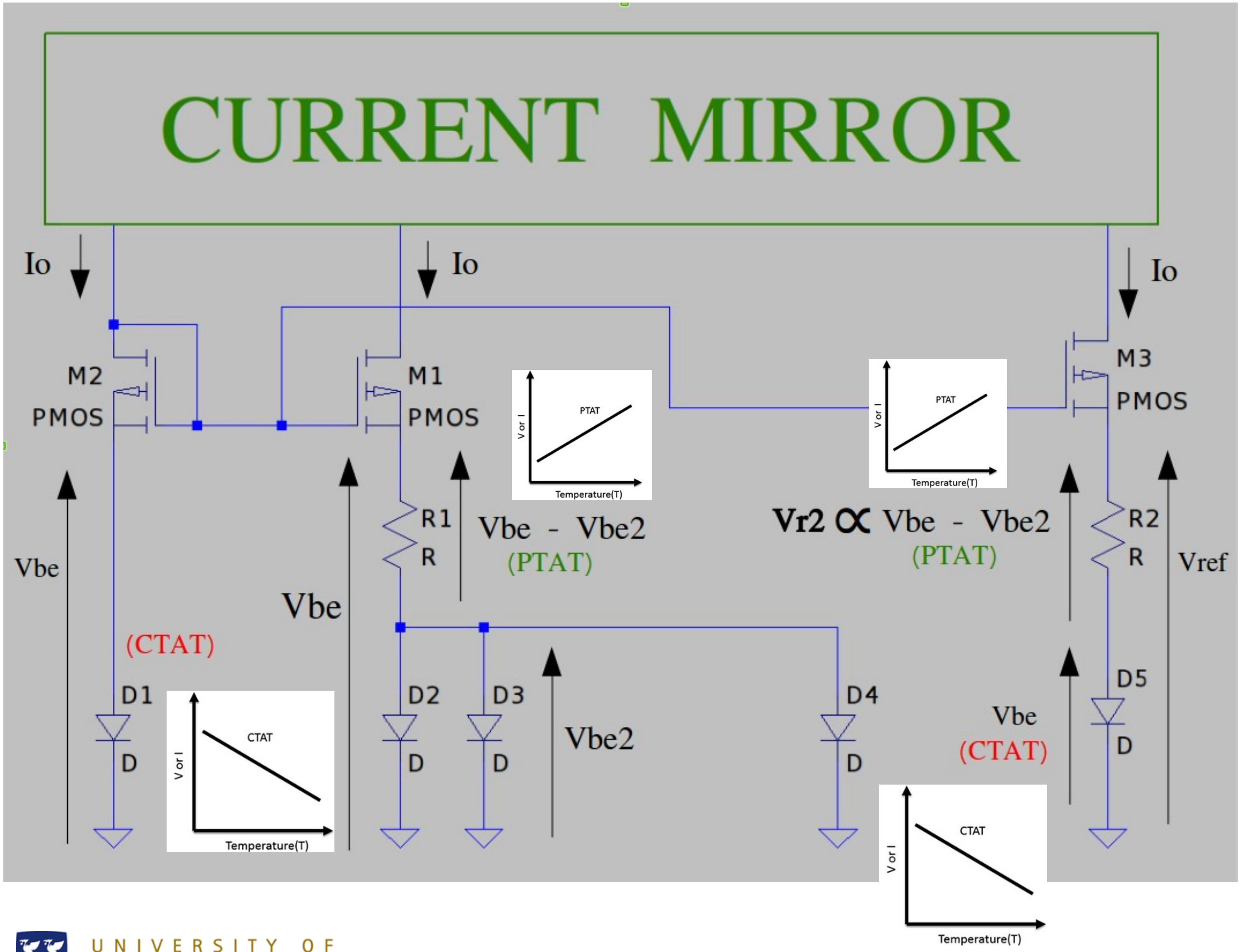
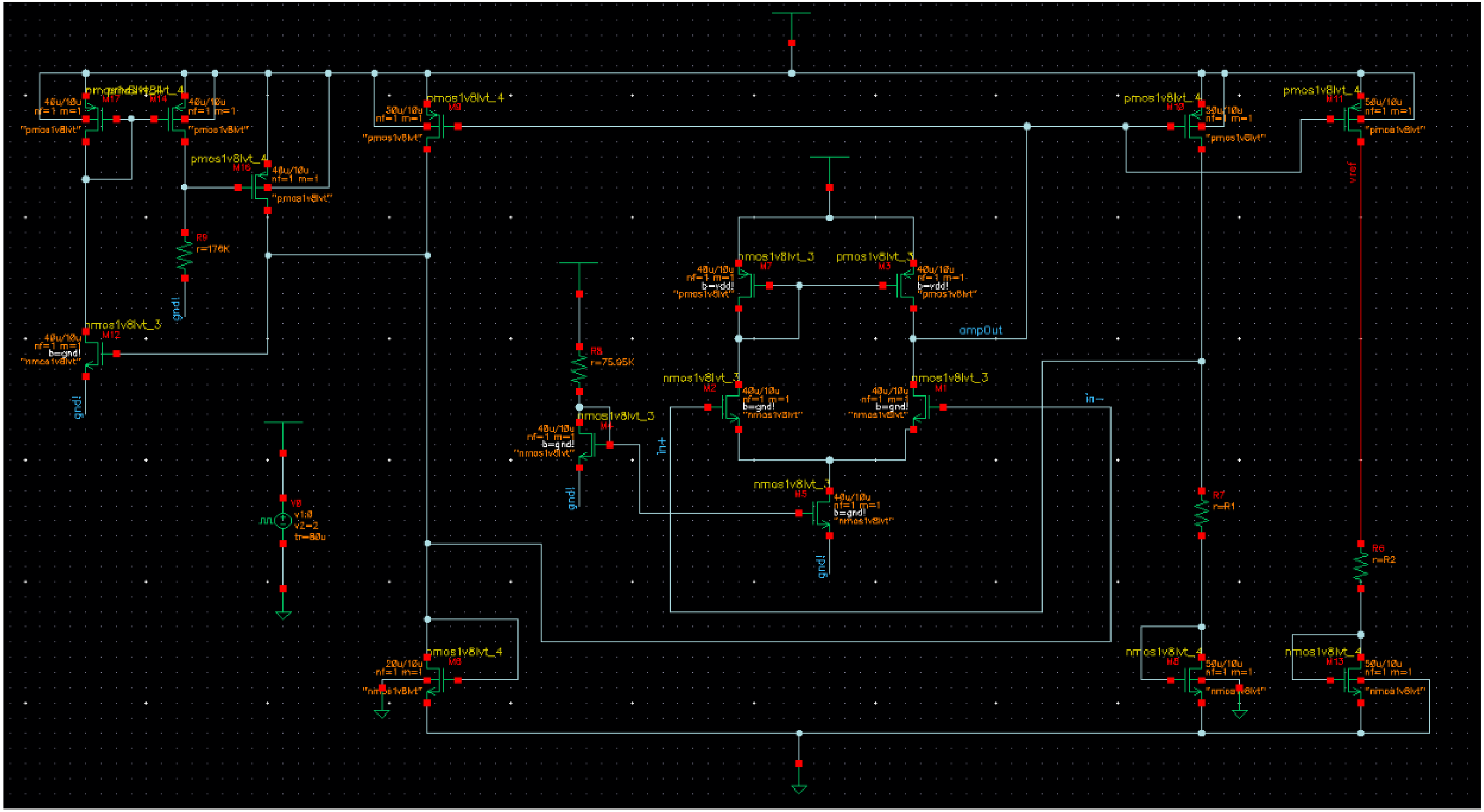
RD50

Bandgap Design Principles

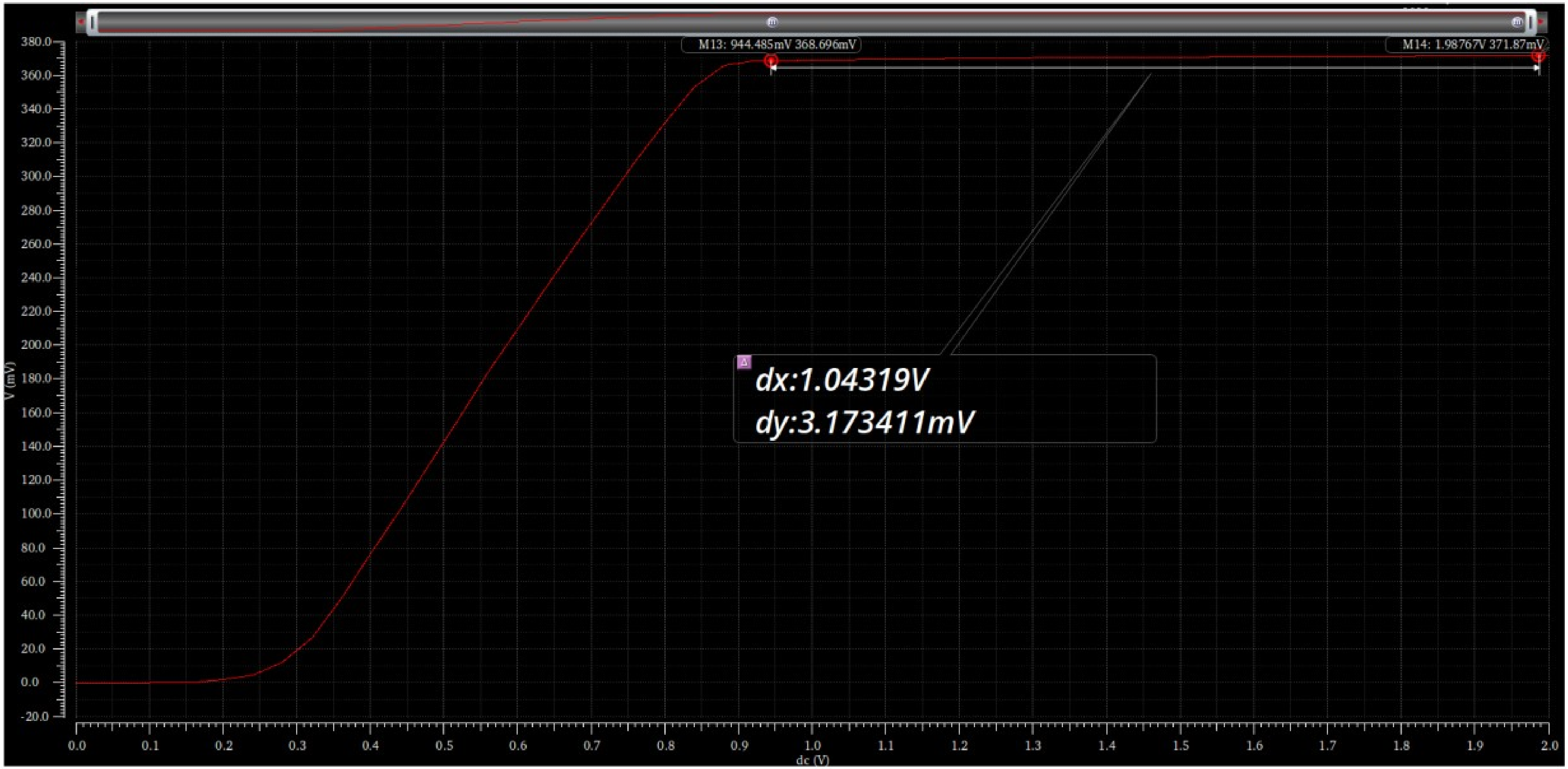


- Vref is a combination of both a PTAT and a CTAT term
- By controlling the ratio of resistor values R1/R2 and the number of diodes n we can cancel out the PTAT and CTAT terms giving an output that is independent of Temperature

FULLY CMOS BASED BANDGAP UKRI-MPW0



FULLY CMOS BASED BANDGAP UKRI-MPW0



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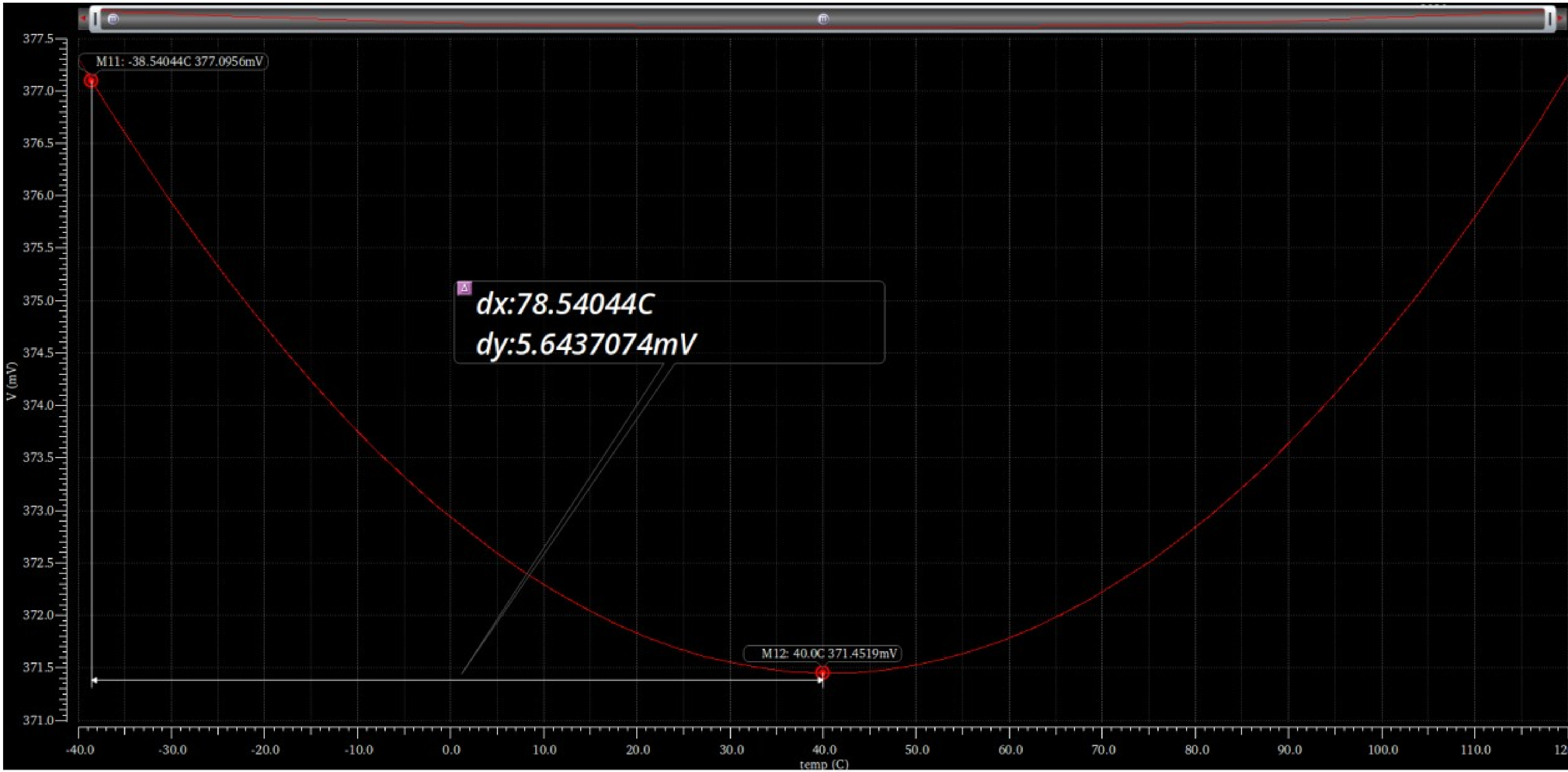
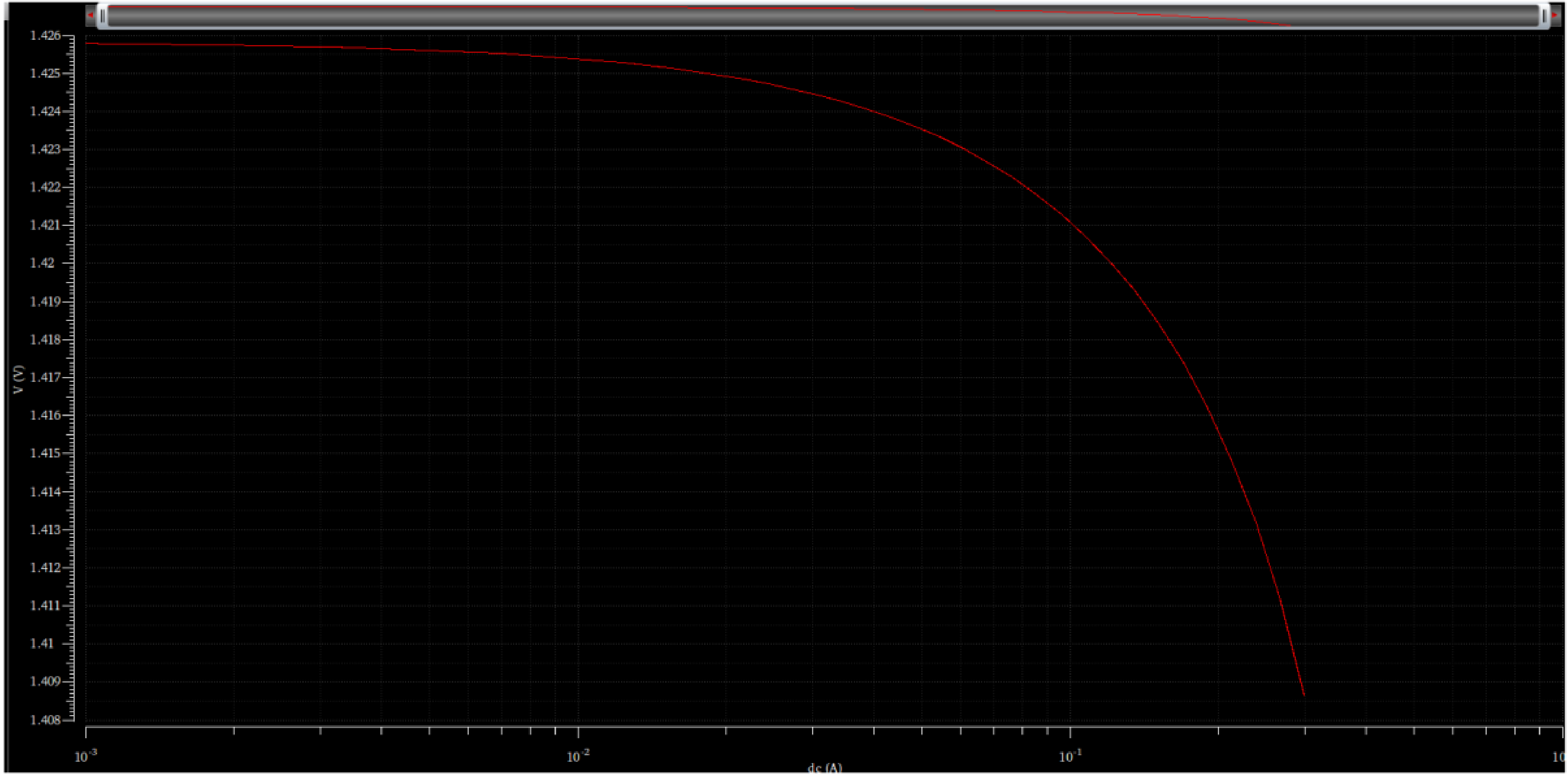
FULLY CMOS BASED BANDGAP UKRI-MPW0



SHUNT REGULATOR PERFORMANCE



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- Ouput voltage changes by less than 5mV for a current draw from 0 to 100mA