R&D of HV-CMOS detectors

2020 HEP Annual Meeting Part II

UNIVERSITY OF LIVERPOOL

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on behalf of the HV-CMOS group

Liverpool HV-CMOS Group

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- **Who we are:**

- **What we do:** Development of HV-CMOS pixel detectors for HEP experiments.

HV-CMOS: Monolithic Pixel Detectors

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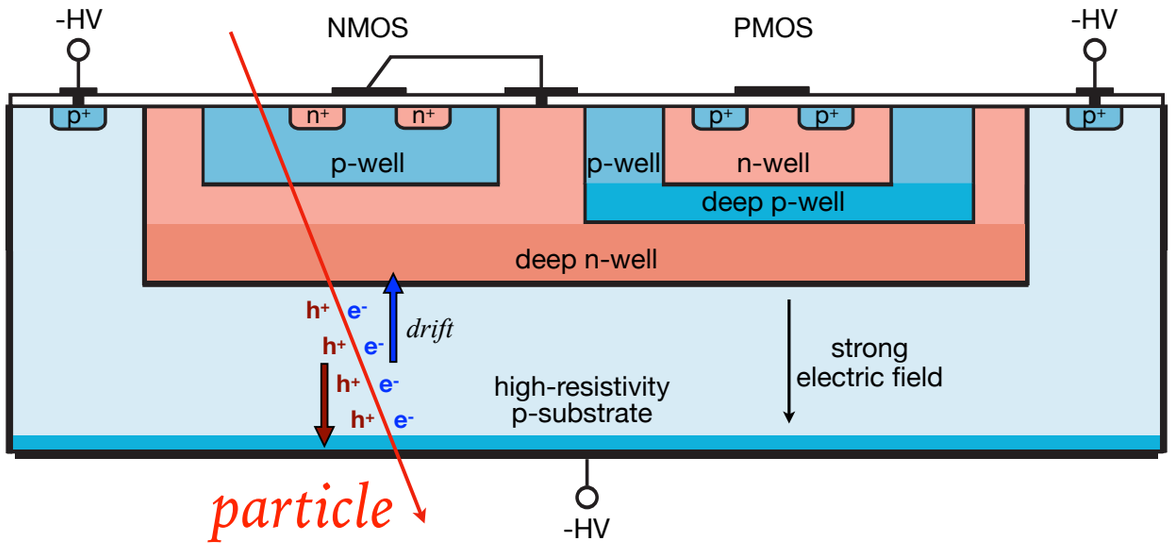
- Sensor and readout electronics are embedded in a single silicon wafer.
- Use commercial HV-CMOS processes.
- Advantages:
  - ➤ Single layer structure: low material thickness (50 μm)
  - ➤ No bump-bonding: Small pixel size (< 50 μm × 50 μm); reduced production cost (~ £100k/m^2)
  - ➤ High bias voltage: fast charge collection by drift (~ 200 ps) and high radiation tolerance (5×10^{15} 1 MeV n_{eq}/cm^2)
- The Mu3e experiment has chosen HV-CMOS pixel detectors and many others are considering them: LHCb, proton EDM, PANDA. And applications fields other than HEP experiments.



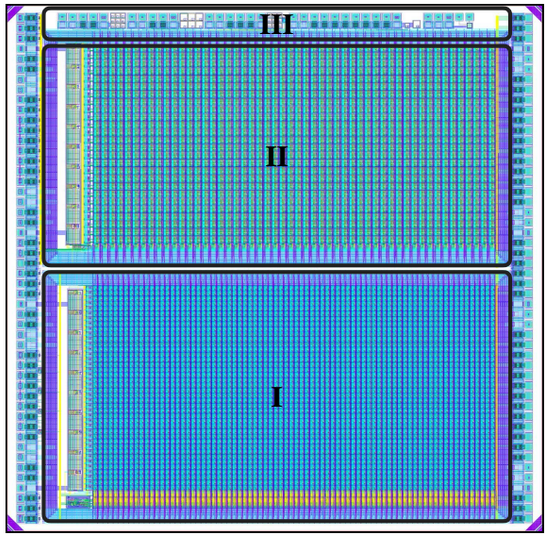
CERN-RD50 CMOS Working Group

- **CERN-RD50** collaboration focuses on developing radiation-tolerant detectors.
- Liverpool has the leadership of its CMOS Working Group which does:
  - ASIC design
  - TCAD simulations
  - DAQ development
  - Chip performance evaluation
- Currently involves about 40 researchers from 14 institutes across Europe:

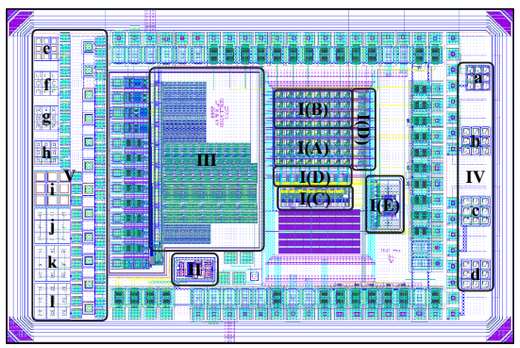
Liverpool HV-CMOS Prototypes

- Development goals:
  - ➤ High radiation tolerance (low leakage and high breakdown)
  - ➤ excellent time resolution and pixel granularity
- Recent prototypes designed by Liverpool in LFoundry 150 nm HV-CMOS process:

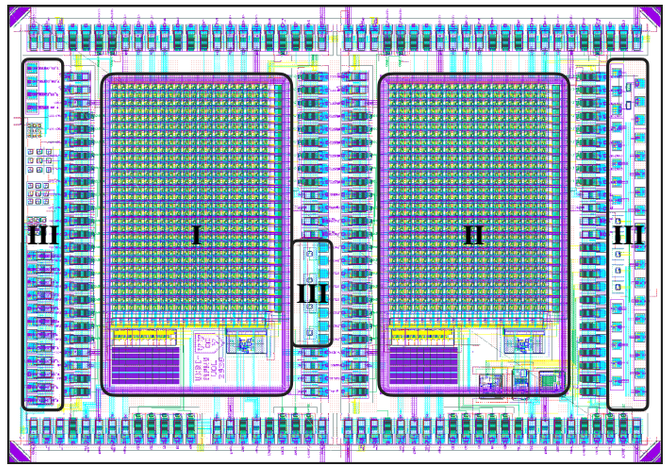
RD50-MPW1 received in Apr. 2018



RD50-MPW2 received in Feb. 2020



UKRI-MPW0 submitted in Nov. 2020



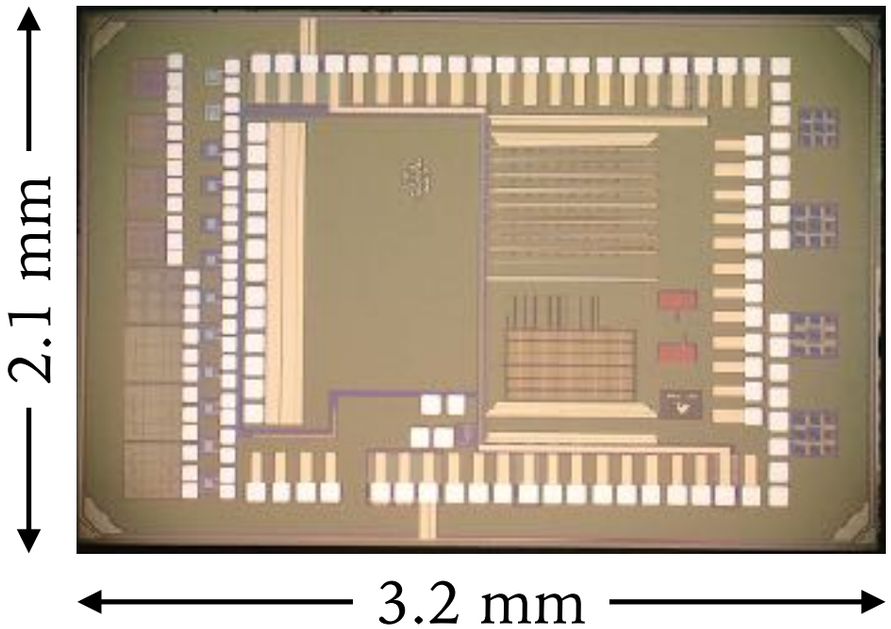
RD50-MPW3 to be submitted in Oct. 2021

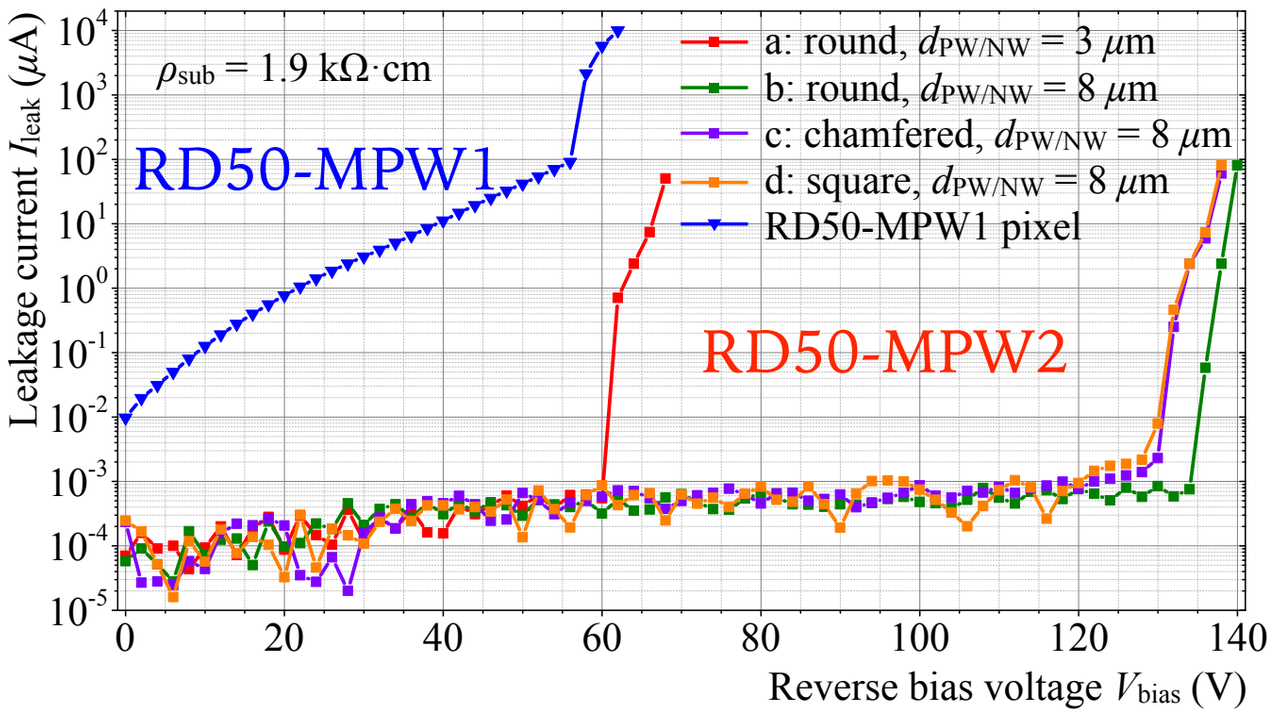
- **RD50-MPW1** - test the LF150 process; works well, but has high I_{Leak} and low V_{BD}.
- **RD50-MPW2** - fixes the issues in RD50-MPW1 and improves pixel performance.
- **UKRI-MPW0** - (Liverpool internal project) tests backside biasing.
- **RD50-MPW3** - implements large pixel matrices with advanced readout electronics.

RD50-MPW2 Measured Results

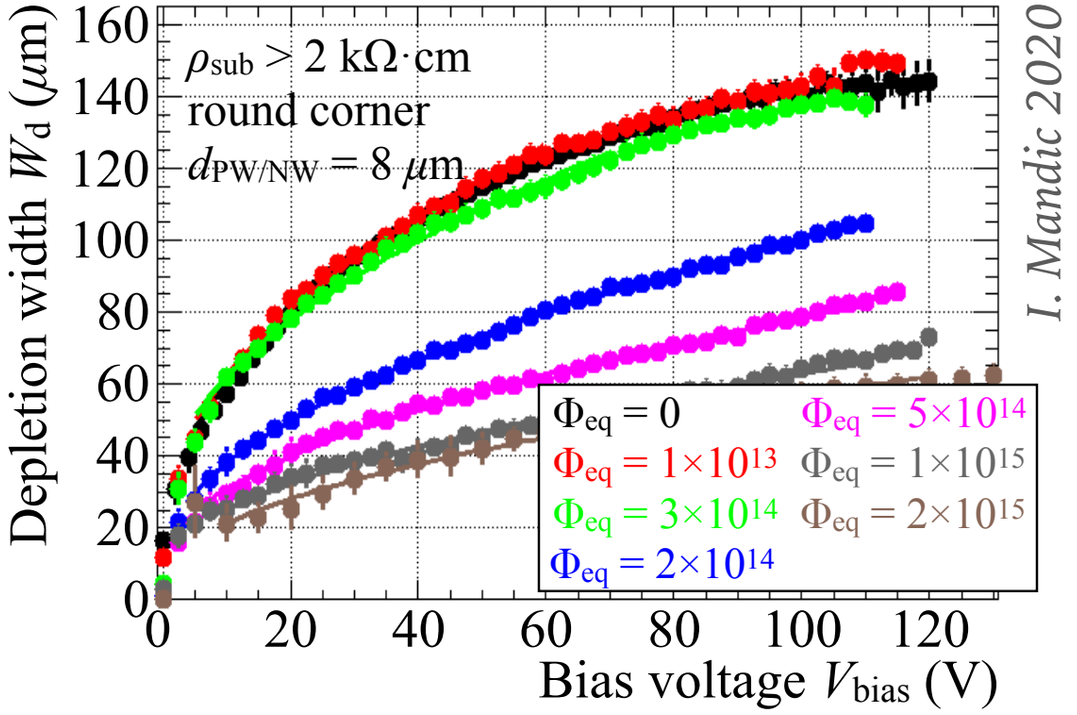
- contains test structures and an 8 × 8 pixel matrix.
- Improvements:
  - Low leakage current
  - High breakdown voltage
  - Fast analog readout electronics
- Despite the difficulties caused by the pandemic, RD50-MPW2 has been well characterised in Liverpool and other RD50 institutes.

received in Feb. 2020





I-V of RD50-MPW1 and RD50-MPW2



Depletion width after irradiation

RD50-MPW2 Measured Results

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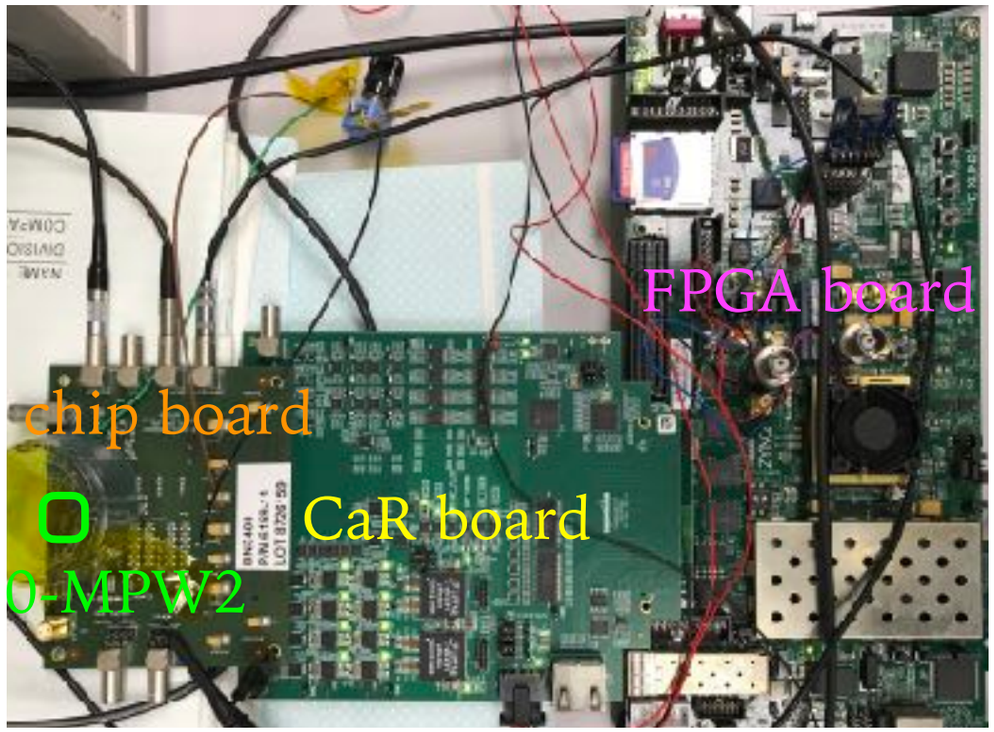
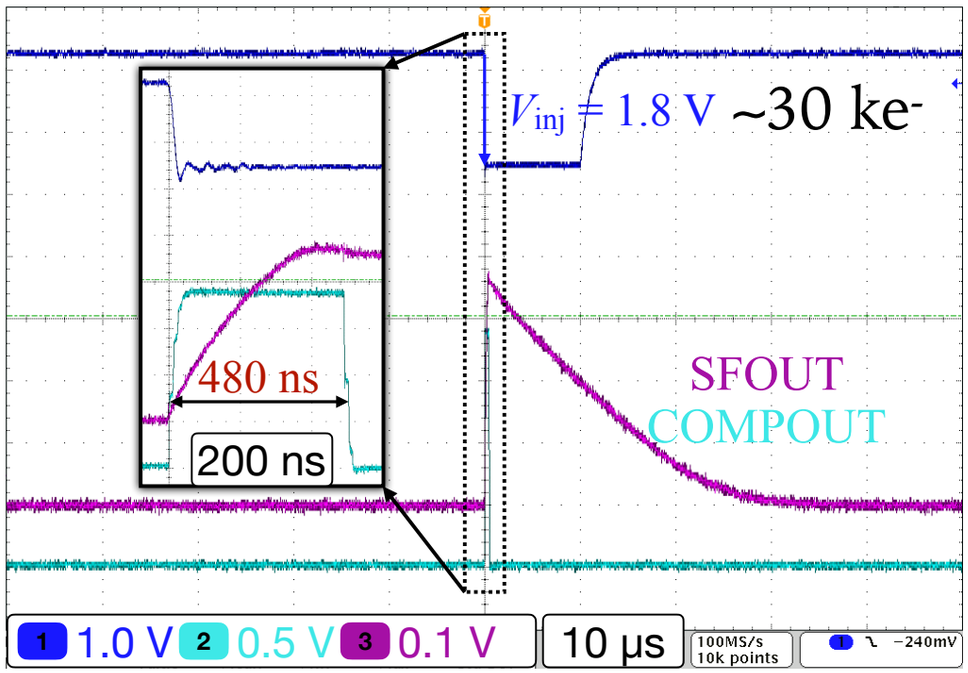
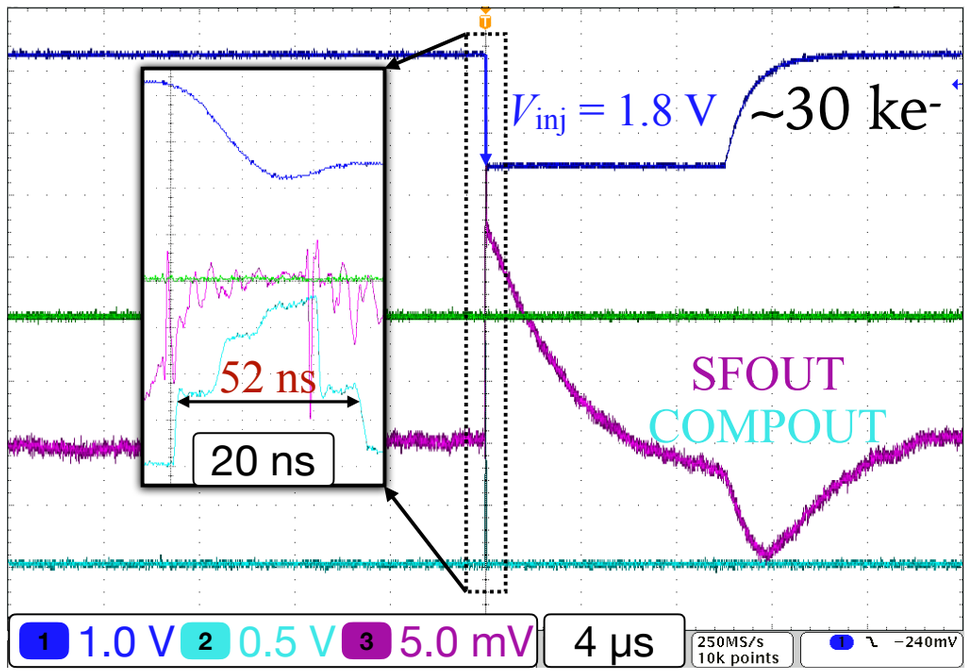
- DAQ system to evaluate performance of readout electronics.
  - ➤ developed within CERN-RD50
- Two pixel flavours with high processing speed:
  - ➤ Continuous-reset (~ 500 ns for 30 ke-)
  - ➤ Switched-reset (~ 50 ns, but not ToT compatible)





Continuous-reset pixel



Switched-reset pixel

RD50-MPW2 Measured Results

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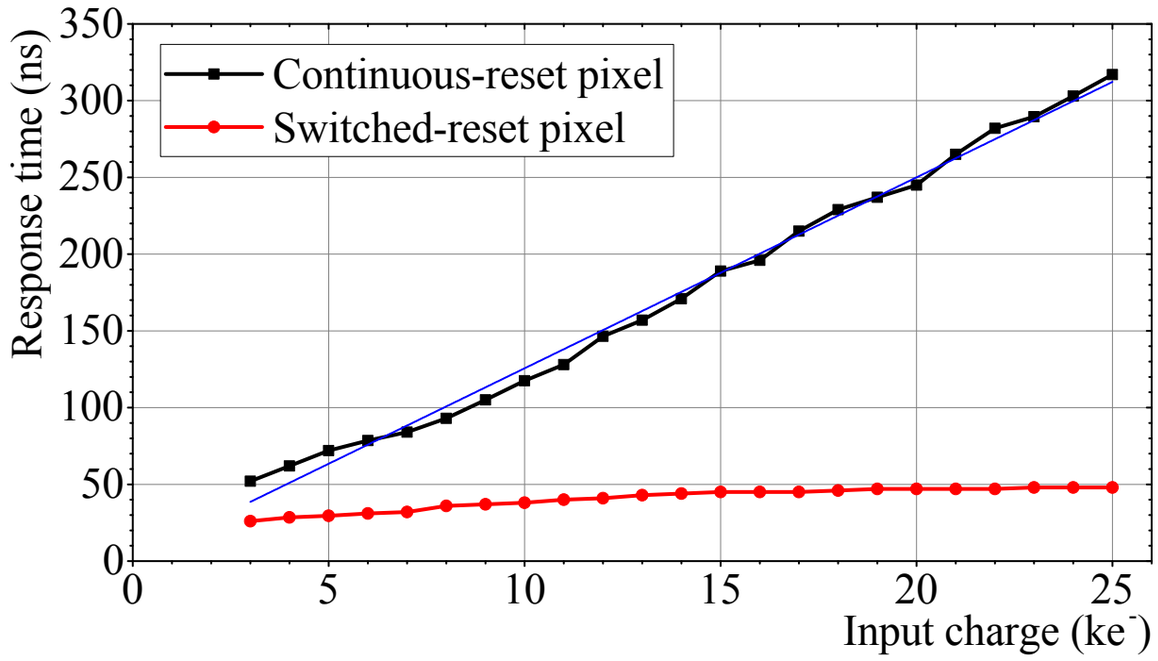
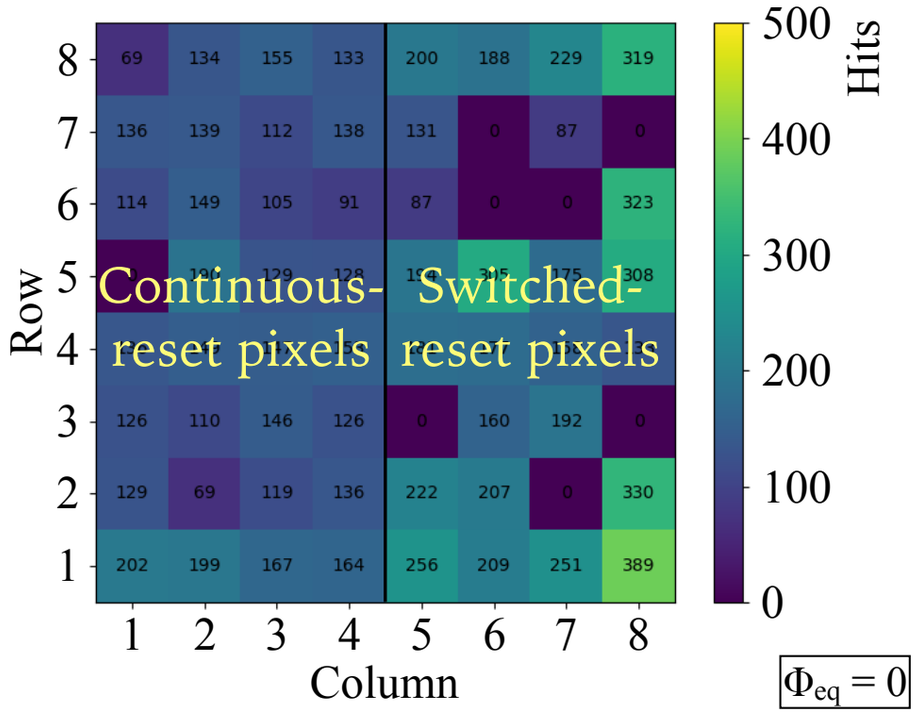
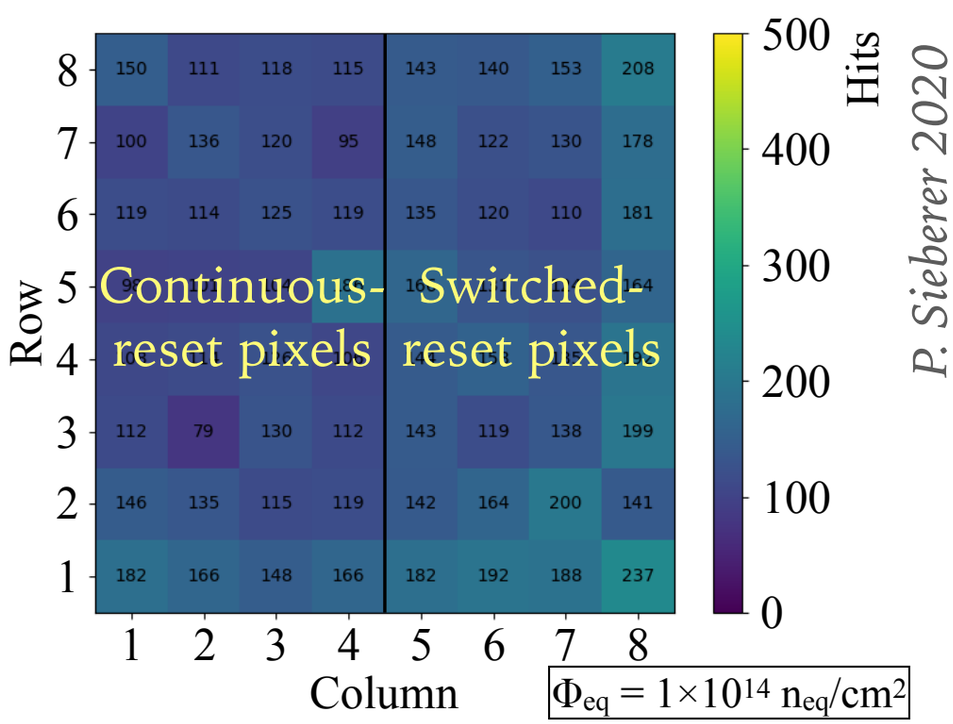
- Dead time for different input charge.



- Hit maps of pixel matrix exposed to radioactive source.





P. Sieberer 2020

RD50-MPW2 beam test

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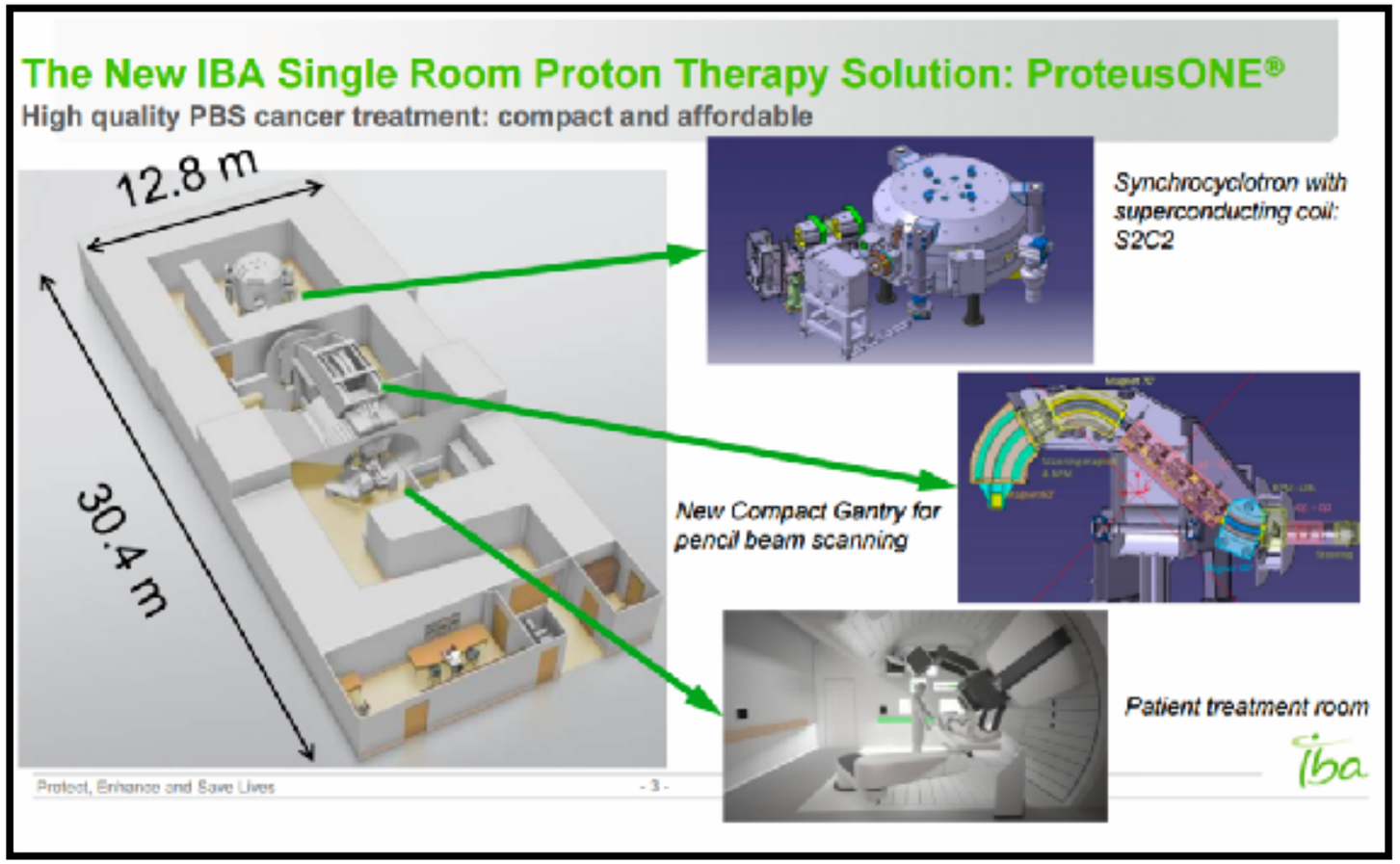
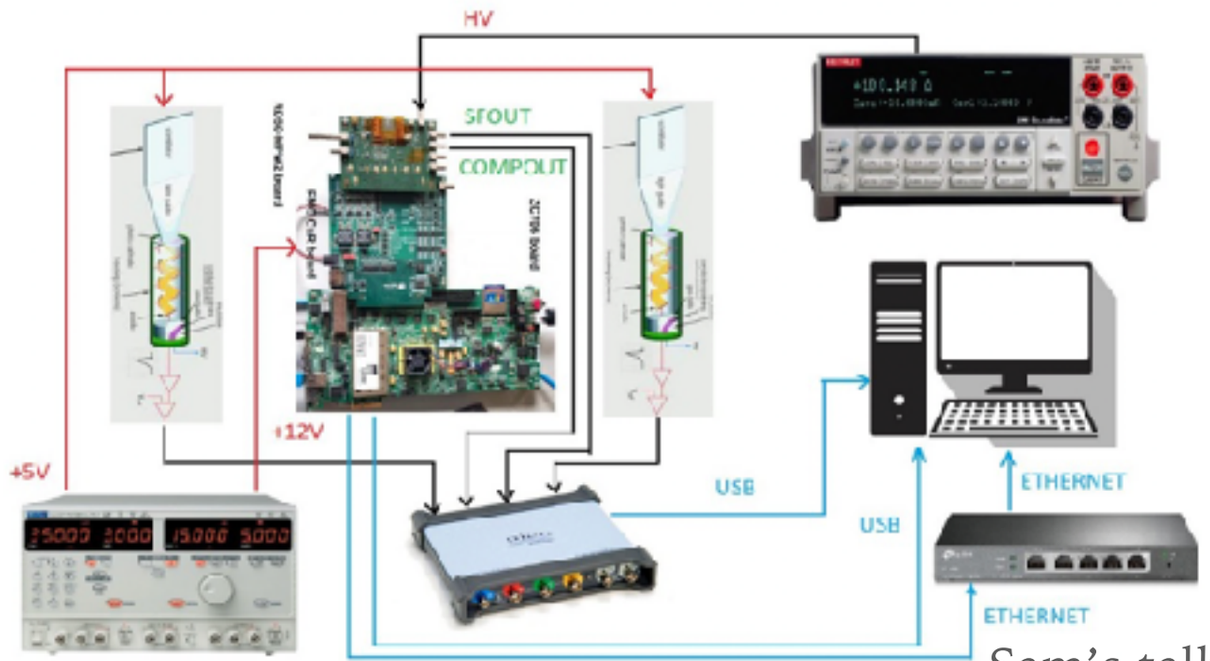
- Beam test at Rutherford Cancer Centre in Northumberland on 10th May.
- Protons delivered in bunches with a 1 kHz rate
  - ➤ Beam energy: 70 -229 MeV
  - ➤ Min beam spot size: 3.5 mm



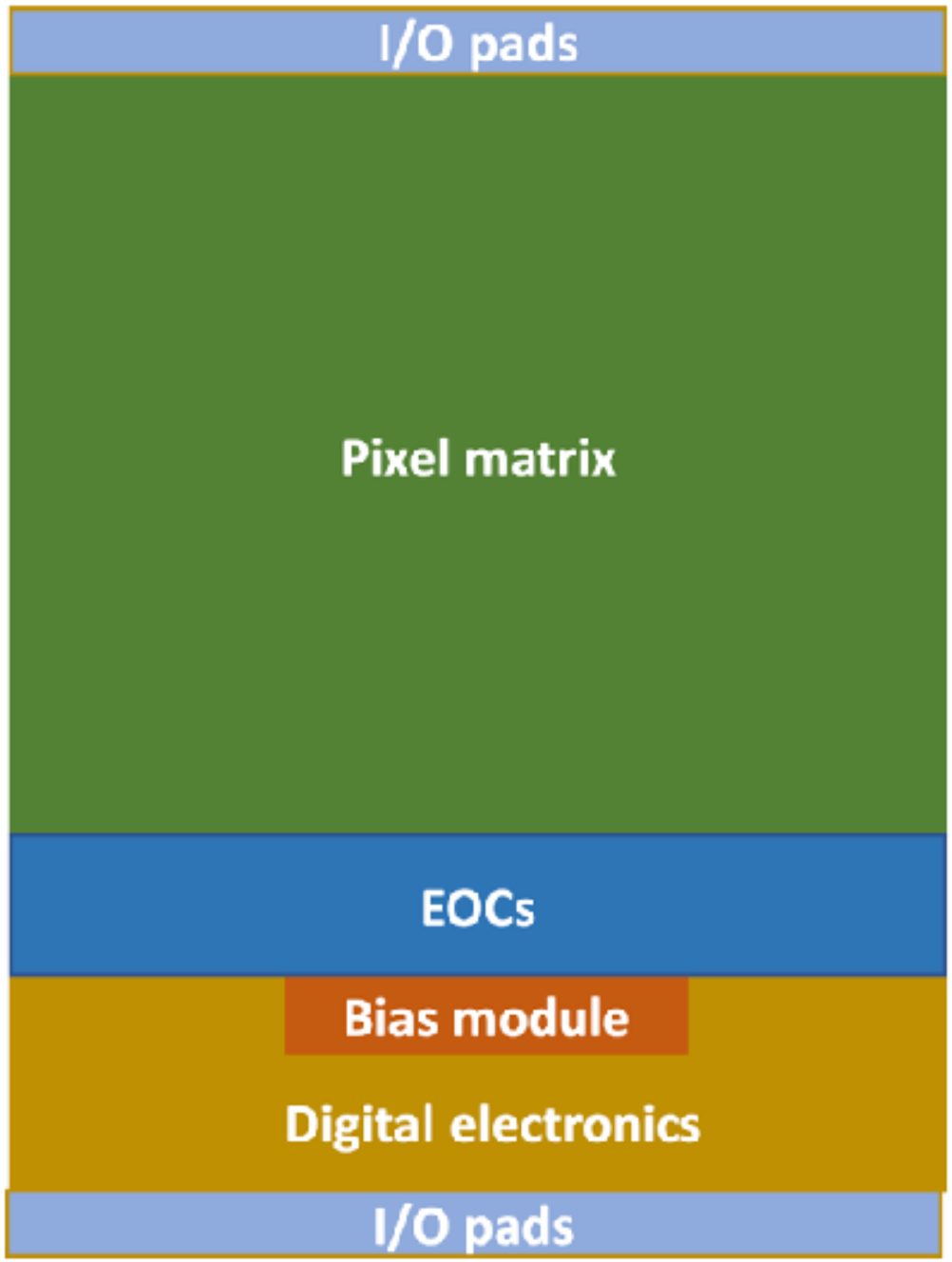
- First beam test by HV-CMOS group.
- DAQ setup prepared.



Sam's talk yesterday

RD50-MPW3

- **RD50-MPW3** is being designed within RD50.
- Incorporates the knowledge from RD50-MPW1 and RD50-MPW2.
- Contains large pixel matrix with full analog and digital readout electronics.
- Optimise peripheral readout circuitry to allow high-rate data transmission.
- Explore new amplifier flavours for improvements in timing and power.

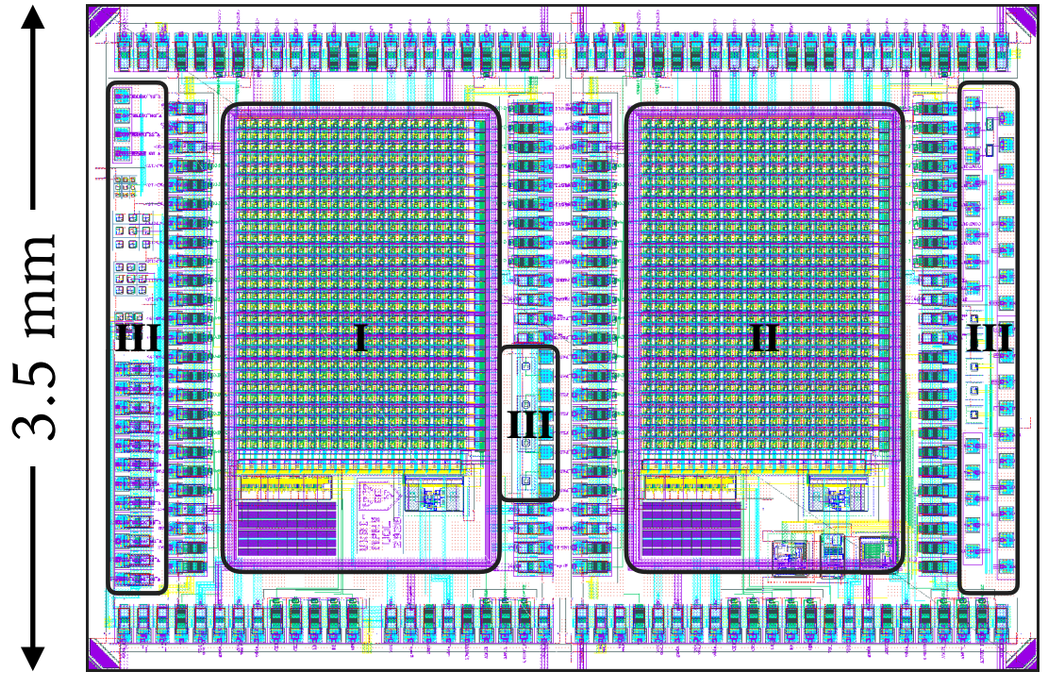


RD50-MPW3 Floorplan
to be submitted in Oct. 2021

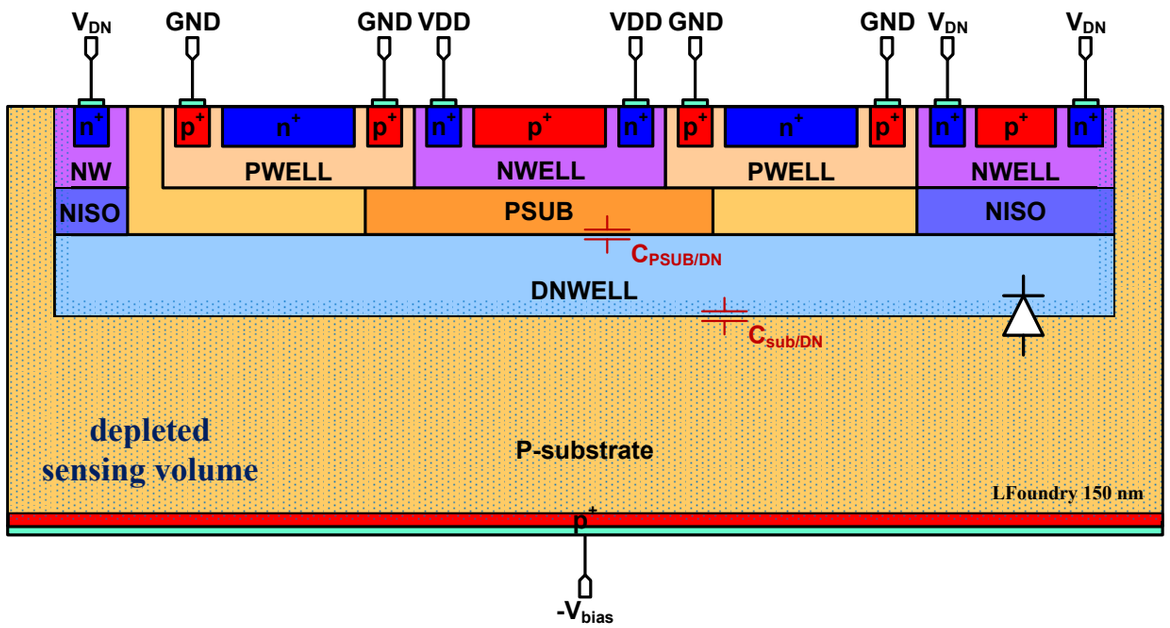
UKRI-MPW0 Overview

- **UKRI-MPW0** a Liverpool internal project.
- Design by Liverpool HV-CMOS group (WFH) during the lockdown.
- Backside biased with no topside contact
  - ➤ Higher breakdown
  - ➤ Better radiation tolerance
- 2 large pixel matrices for more statistics.

submitted in Nov. 2020



5.0 mm



Backside biased only

UKRI-MPW0 High Breakdown

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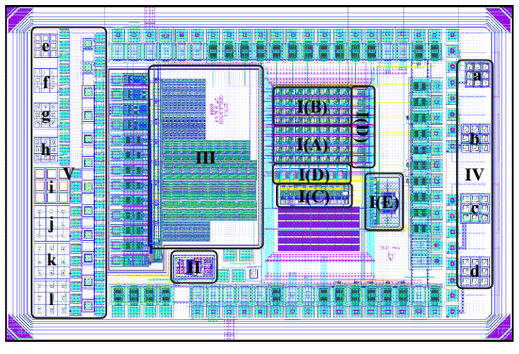
- High breakdown voltage (~ 1000 V).
- Test Enclosed Layout Transistors (ELT) for better radiation tolerance.
- DAQ development in progress.
- Wafer production completed.
- Backside processing in progress now in IBS.
- Will be delivered in the following weeks.

Summary and Next step

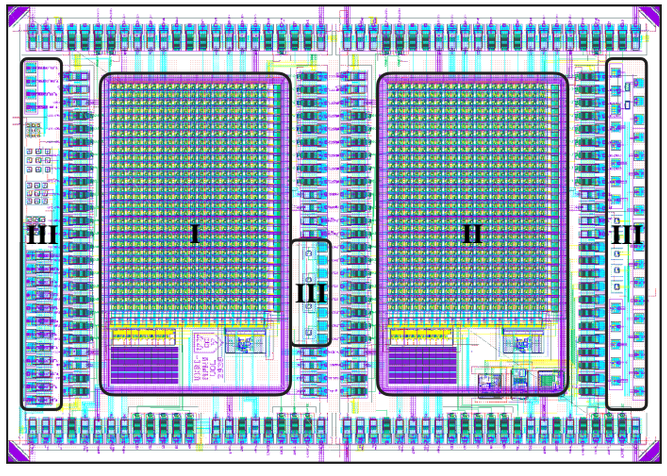
- RD50-MPW2 works well in accordance with design.
- RD50-MPW2 beam test next month.
- Receive and test UKRI-MPW0 in the near weeks.
- Submit RD50-MPW3 in October.

received in Feb. 2020



RD50-MPW2

submitted in Nov. 2020



UKRI-MPW0

to be submitted in Oct. 2021

RD50-MPW3