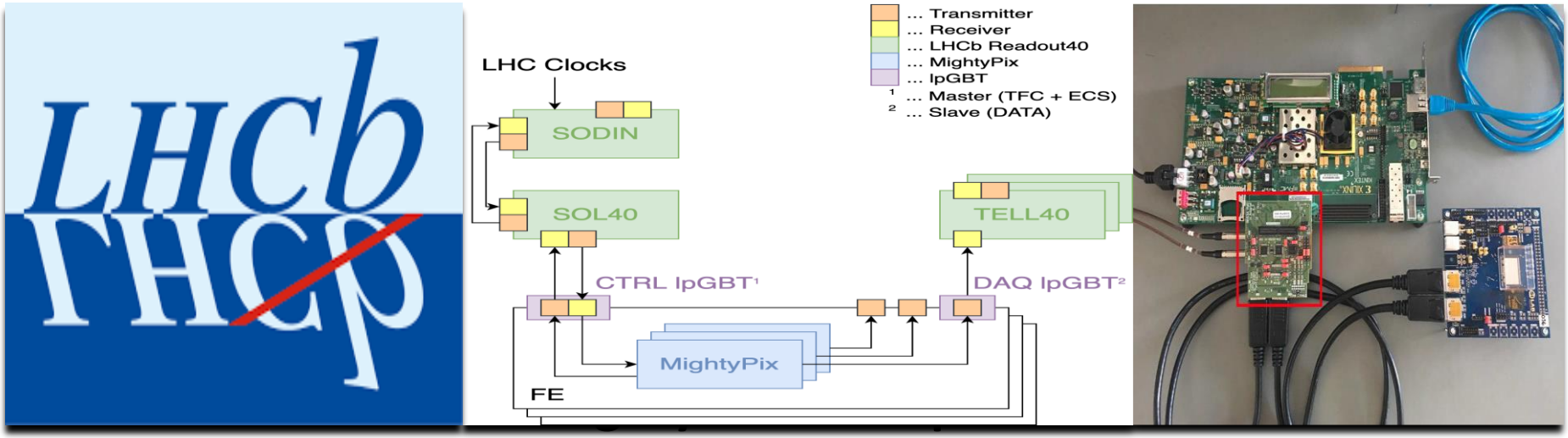

Mighty Tracker Update

Ayushi Khatri

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Contents

- Myself
- Mighty Tracker
- MightyPix Design
- Verification Framework
- Electronics Beyond Chip
- Measurement
- Conclusion

Myself

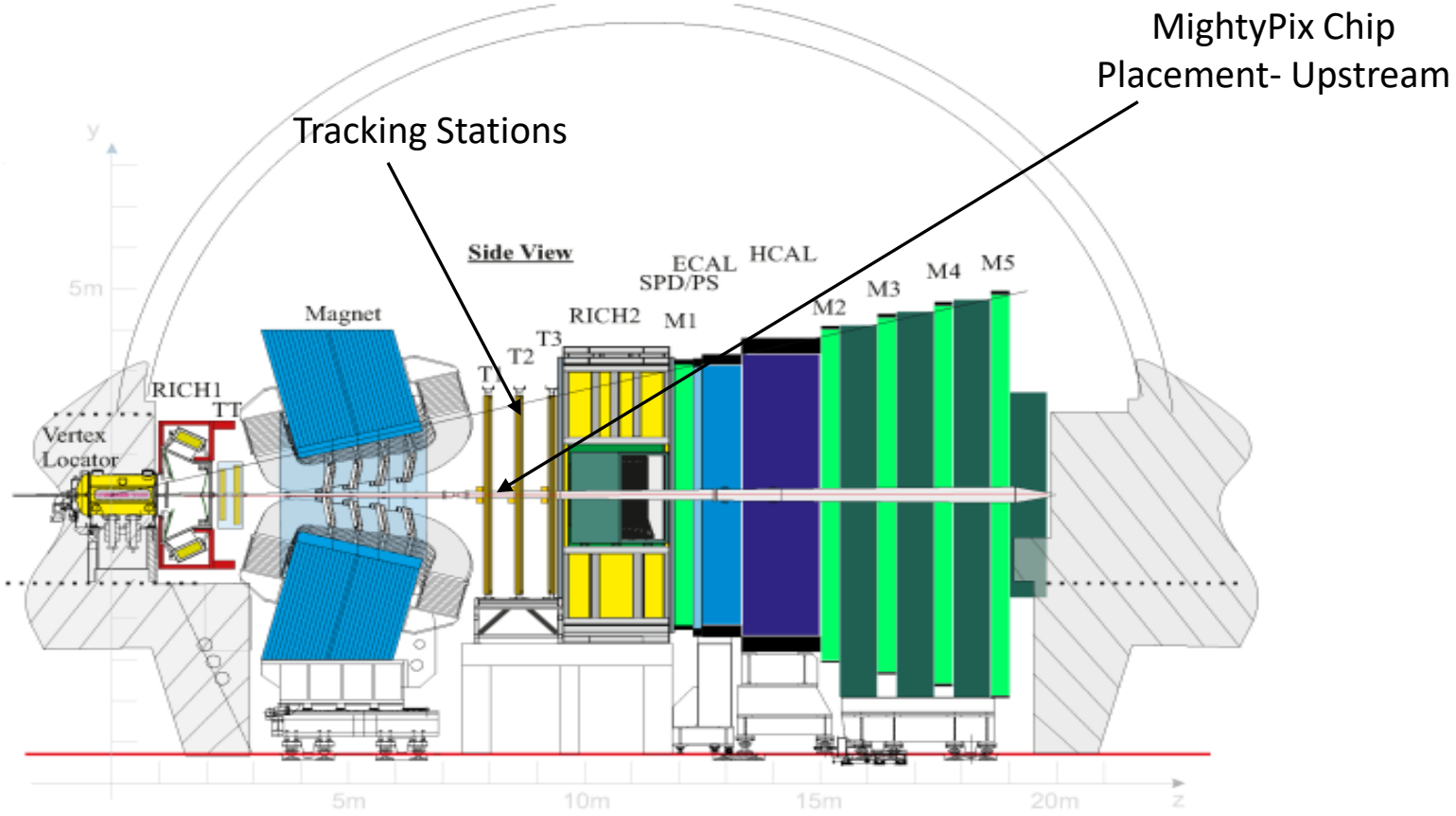
- **University of Liverpool-**
  - Digital ASIC Design Engineer.
  - October, last year.

- **ST Microelectronics-**
  - Standard cell department for 1 year.
  - Worked on Design validations and Layout.

- **Education -**
  - Master’s in VLSI design, 2020.
  - Bachelor's in Electronics and Communication.

Mighty Tracker

- **LHCb detector layout-**



Schematic Sideview of Upgrade II Detector, LHCb framework TDR, Feb 2022

Timeline-

- Why new Mighty Tracker-
  - The radiation damage with time would increase, which SciFi could not sustain.
  - So Silicon detectors that have **high radiation tolerance**, **excellent resolution and granularity**, are planned to introduce to the design. Its two step process.

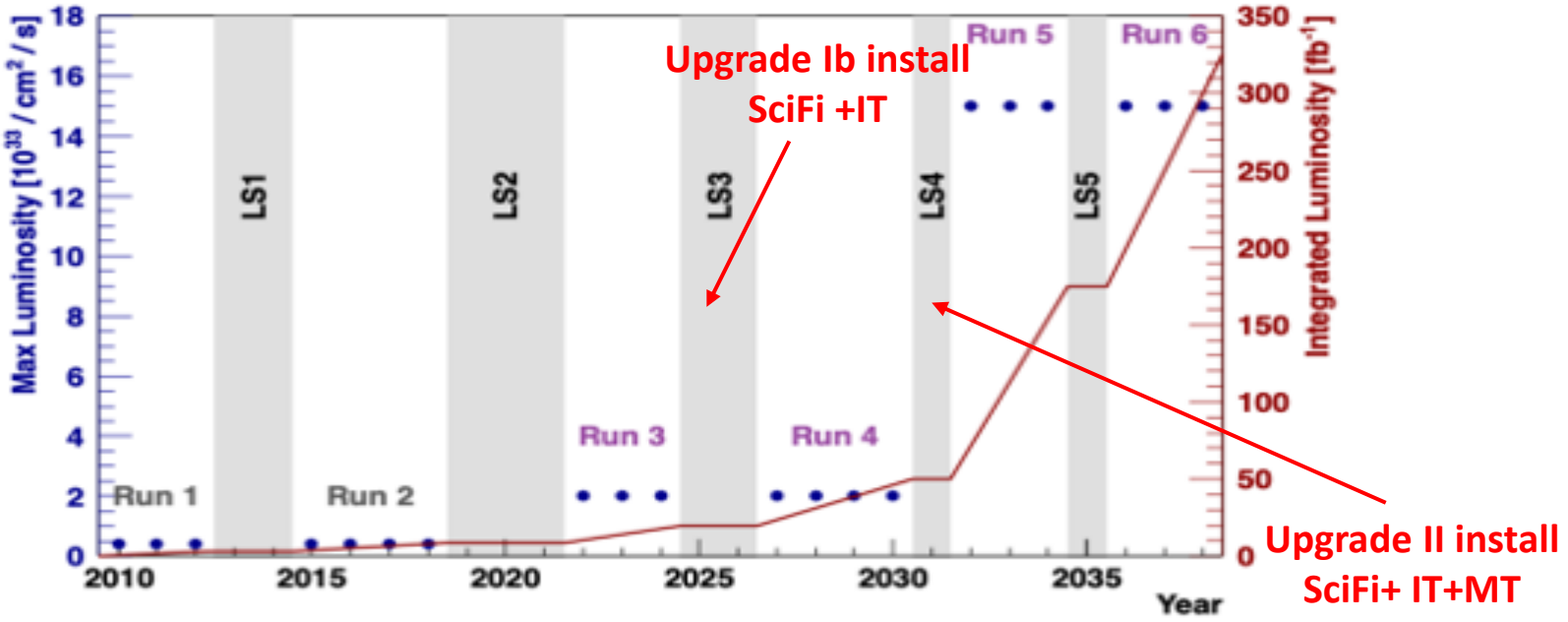


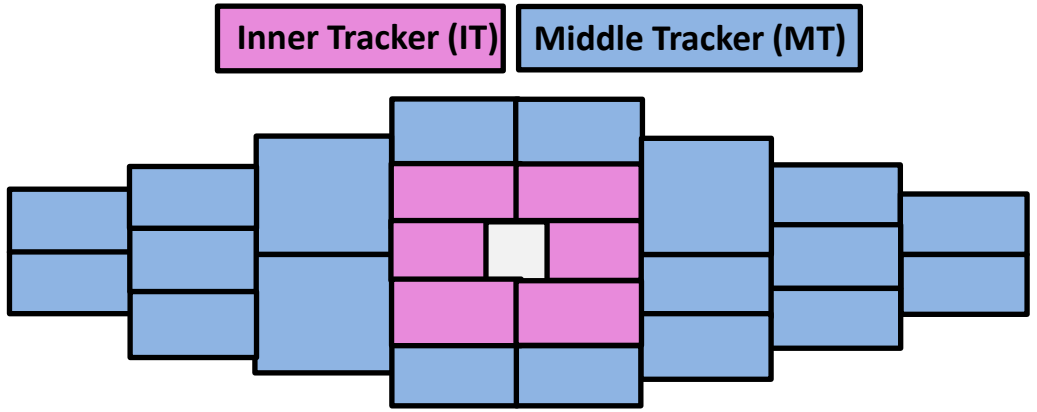
Figure- Timeline of Upgrade Ib and II with Mighty Tracker installation dates, LHCb TDR, Feb. 2022

Mighty Tracker

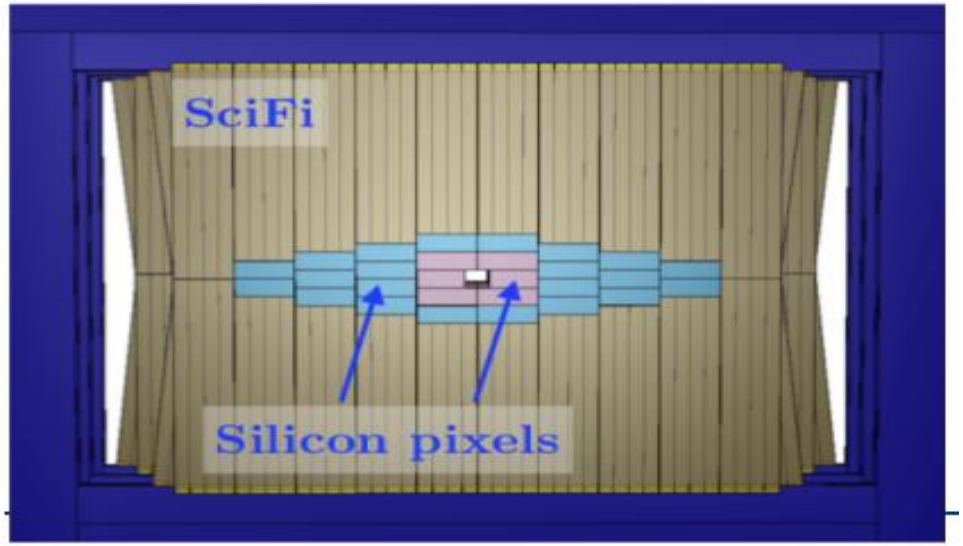
Structure-

- For Upgrade Ib in LS3, the center part of SciFi is replaced with **Silicon inner tracker (IT)**

- For the Upgrade II in, LS4, hybrid technology of Scifi and both the **middle tracker (MT)** as well as the inner tracker (IT) will be constructed.



Inner + Middle + SciFi Tracker = New Mighty Tracker

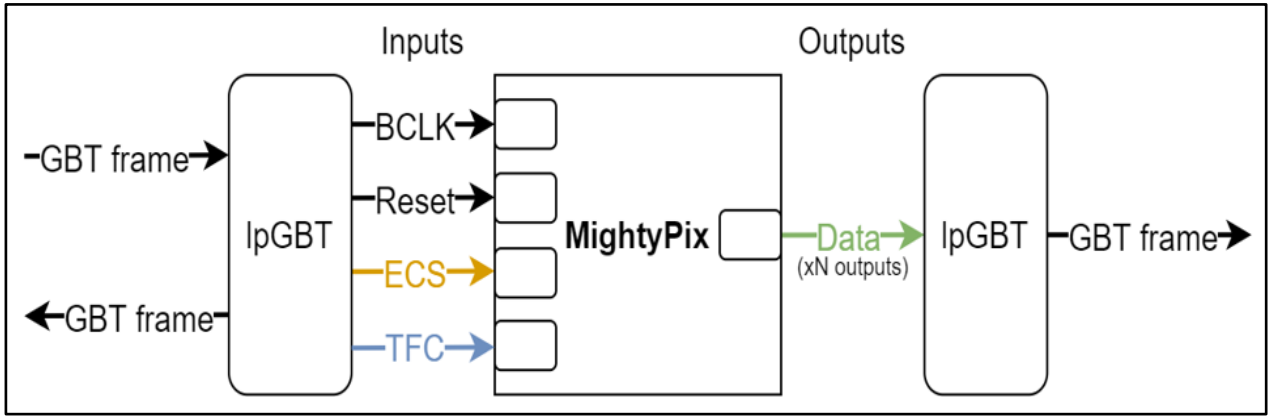


LHCb framework TDR, Feb 2022

MightyPix Design

Design Features-

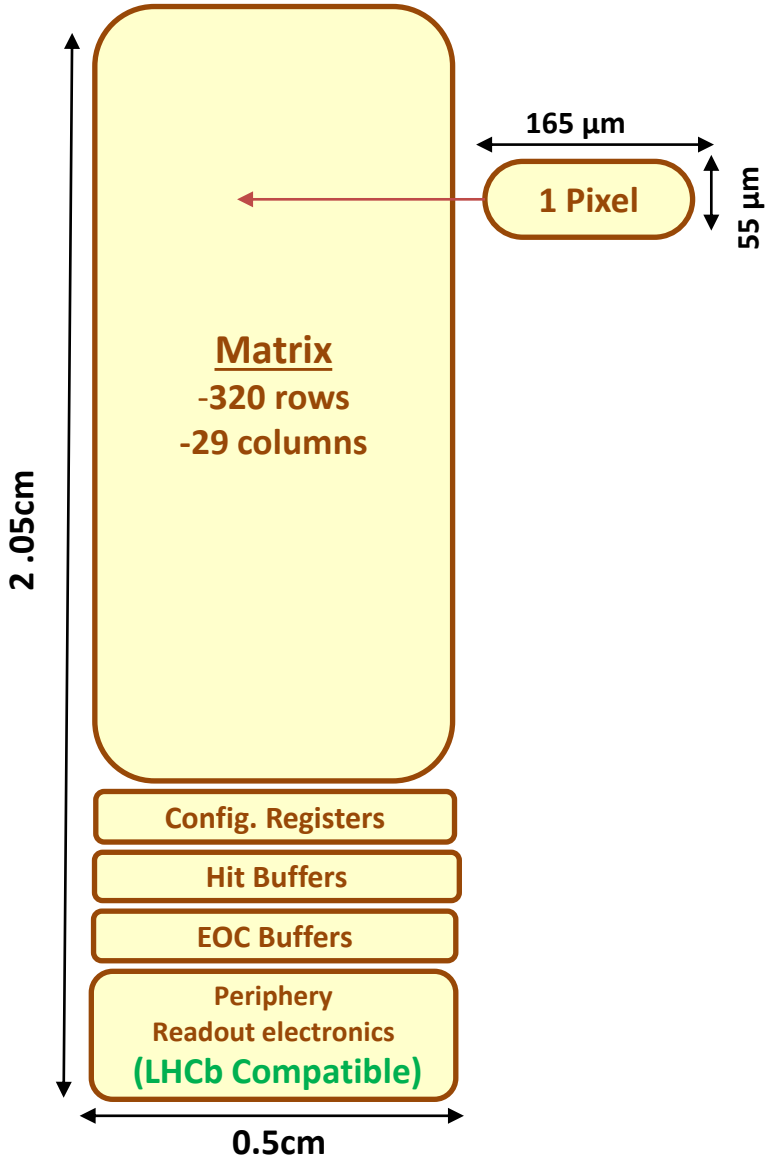
- MightyPix chip's digital periphery is almost **compatible with LHCb** DAQ, developed with HV-CMOS sensors compatible to radiations.
  - LHC clock – 40MHz
  - lpGBT protocol is used
  - TFC (Timing and Fast Control) and ECS (Experiment Control System) commands with DAQ



Sigrid Scherl

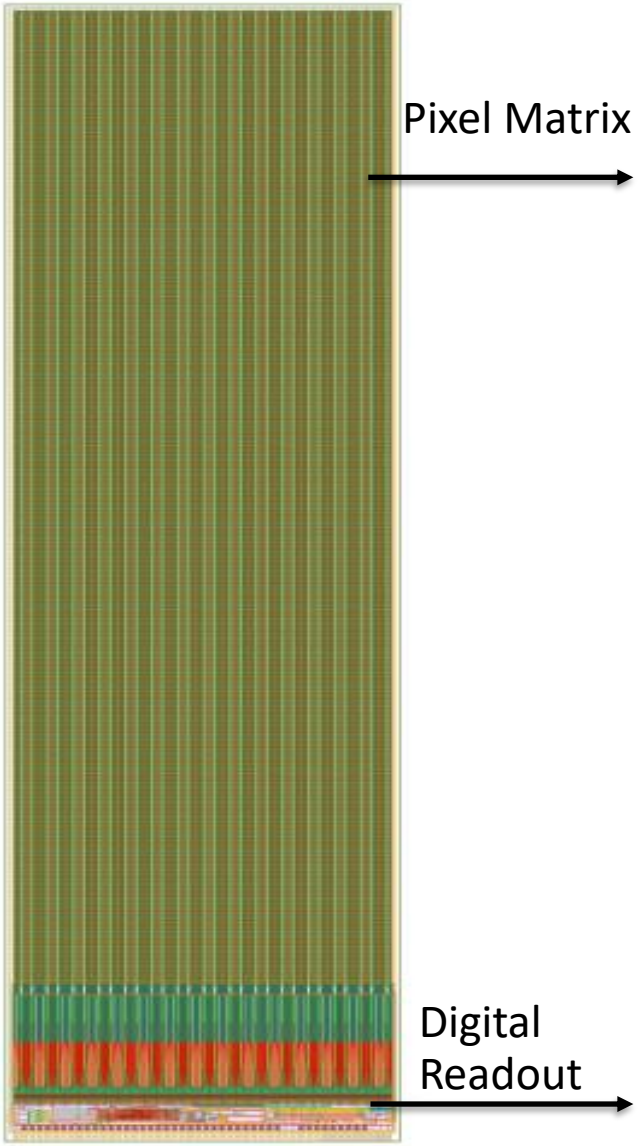
MightyPix Design

- **Chip Specification of MightyPix 1**
  - Chip size 2.05 cm x 0.5 cm (LxW)
  - Escalate full column length
  - Pixel size- 165 µm x 55 µm
  - This design grows on the well established design of µpix and ATLASpix HV-CMOS chip.
  - Digital DAQ readout (LHCb compatible)



MightyPix Design

- **Layout of MightyPix Design→**
- **Review & Submission**
  - Design review held in January with LHCb and ASIC experts.
  - Chip was submitted last week to TSI foundry and is expected to be back by November.
  - This is a prototype chip & is 1/4th size of final chip.



MightyPix Design

Design Setup-

- Successfully set up and simulated design in Liverpool.

```
Path 1: VIOLATED (-1384 ps) Late External Delay Assertion at pin d_out[0]
           View: functional_slowHT
          Group: C20_functional_slowHT
     Startpoint: (R) serialiser_SerializerTree_4to2_A_Stage2_reg[0]/CP
          Clock: (R) clk_640M
       Endpoint: (R) d_out[0]
          Clock: (R) clk_640M

                    Capture       Launch
       Clock Edge:+    1562            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)     -300 (I)
           Arrival:=   1562         -300

      Output Delay:-     781
       Uncertainty:-     156
     Required Time:=     625
      Launch Clock:-    -300
         Data Path:-    2310
             Slack:=   -1384

Exceptions/Constraints:
  output_delay             781           constraints_function_line_148_58_1

#-------------------------------------------------------------------------------------------------------------------------------------
#                  Timing Point                    Flags   Arc   Edge   Cell      Fanout  Load Trans Delay Arrival      Instance
#                                                                                          (fF)  (ps)  (ps)   (ps)       Location
#-------------------------------------------------------------------------------------------------------------------------------------
  serialiser_SerializerTree_4to2_A_Stage2_reg[0]/CP -       -     R     (arrival)     25     -     0     -    -300             (-,-)
  serialiser_SerializerTree_4to2_A_Stage2_reg[0]/Q  -       CP->Q R     DFSX4_HV       1 525.2  2941  2266    1966  (445.200,131.040)
  d_out[0]                                          <<<     -     R     (port)         -     -     -    43    2010             (-,-)
#-------------------------------------------------------------------------------------------------------------------------------------
```

Timing report for the design

Synthesis result of design setup in Liverpool

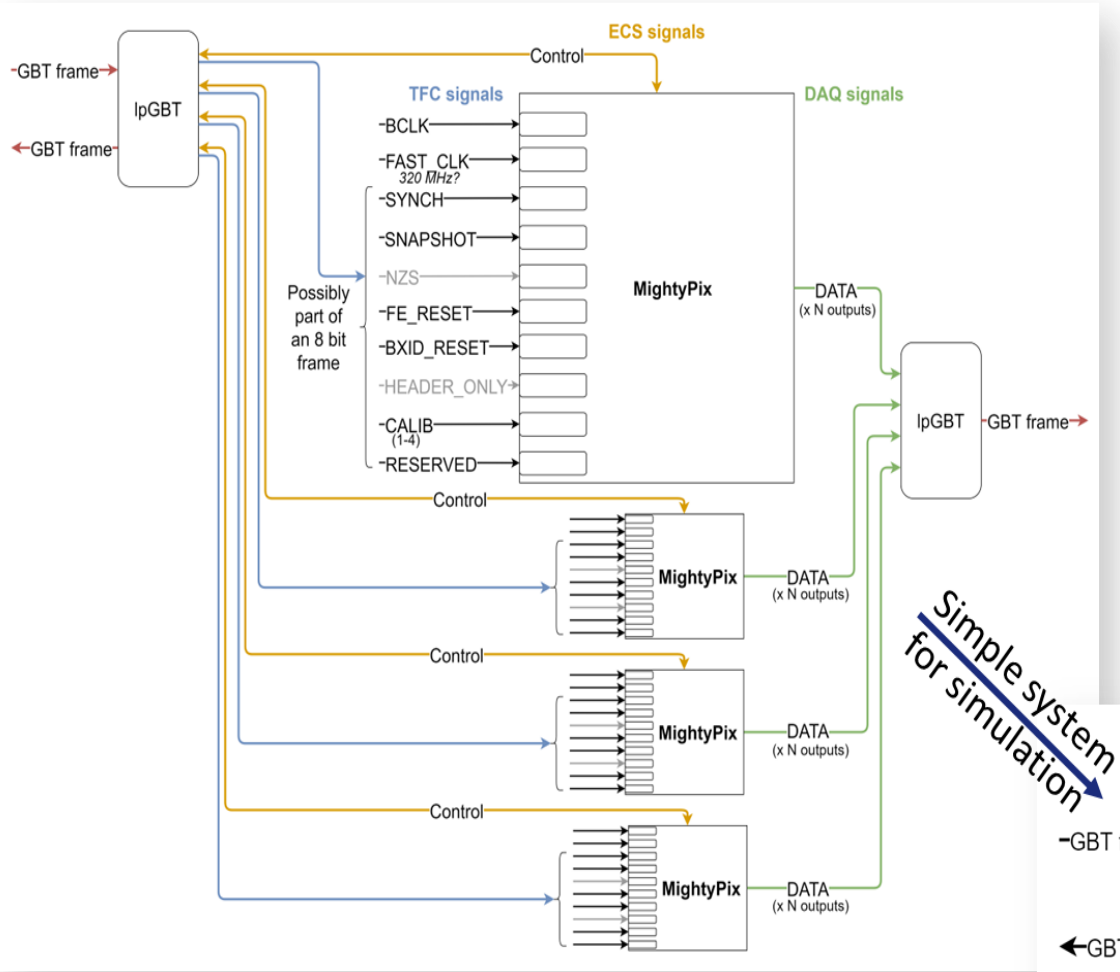
MightyPix Design

- **Design Run-**
  - Simulation
  - Synthesis
  - Place and Route

- **FPGA Prototyping of MightyPix1 Chip-**
  - Emulating the chip on FPGA to anticipate the behaviour of the chip. This would be useful for future experiments in labs.
  - Imported Design on Xilinx Vivado and use Model Sim for Simulations
  - Simulate to analyse I2C timing constraints, data signals and debug clocks for timing resolutions and power consumption.

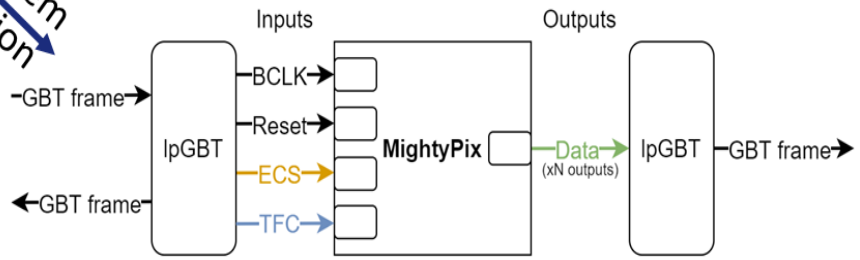
Verification Framework

- **LHCb MightyPix Interface:-**



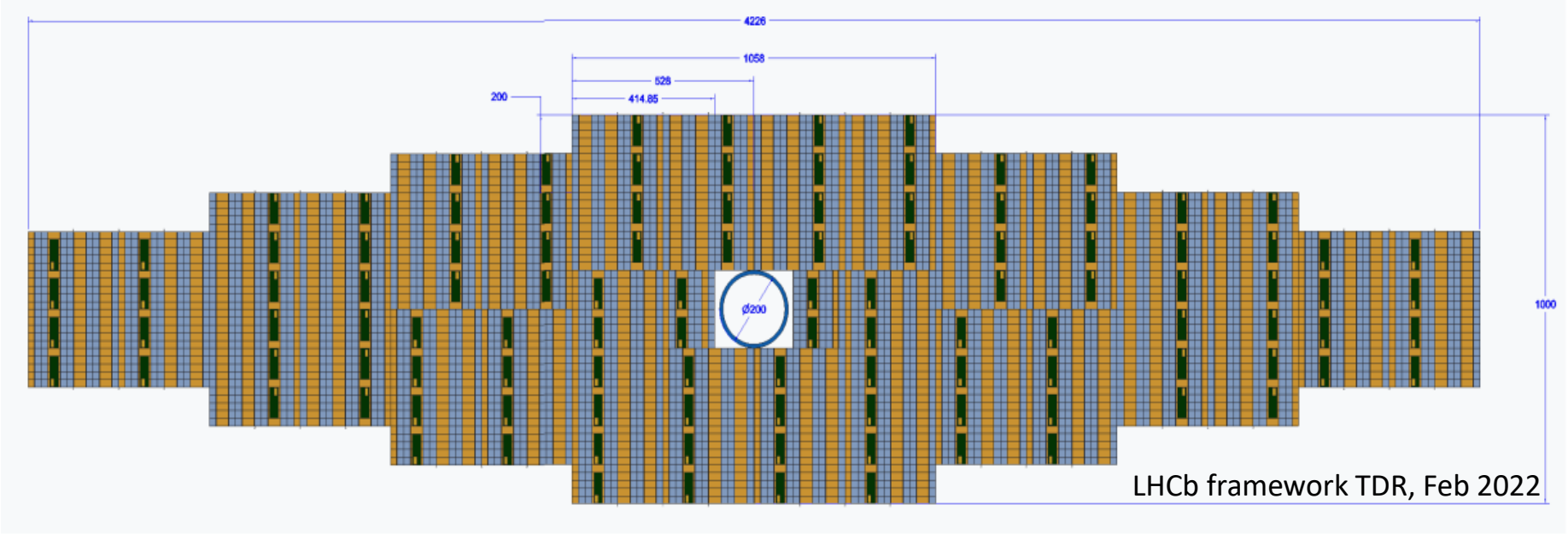
- Experiment Control System (ECS)
  - Bidirectional links from and to the lpGBT readout board
- Timing and Fast Control (TFC)
  - Links from lpGBT readout board to the MightyPix chips
  - Signals possibly part of 8-bit frame
- Data Acquisition (DAQ)
  - (N) Links to lpGBT per chip

Simple system for simulation



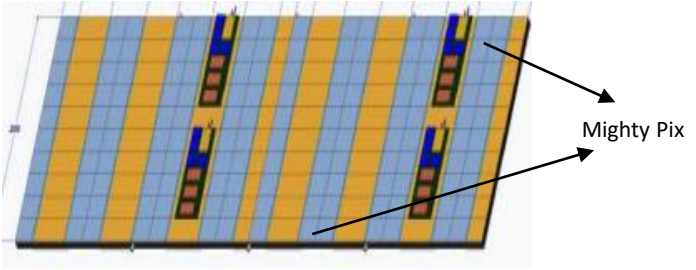
Sigrid Scherl

The Mechanical Outline of the Tracker-



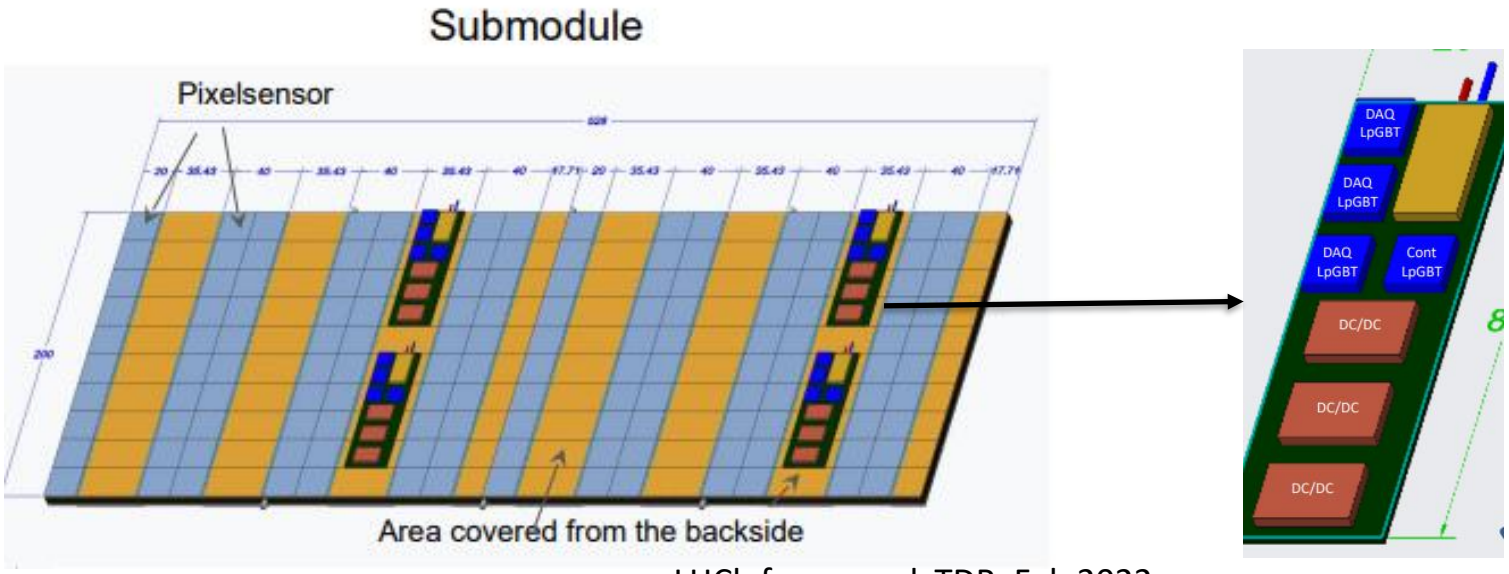
LHCb framework TDR, Feb 2022

- 6 layers of two sided pixel areas
- 28 sub-modules per layer
- <35 MightyPix per sub-module
- 3 m^2 silicon per layer
- 18 m^2 pixel area



Module

Current Proposal for Mighty Tracker Module

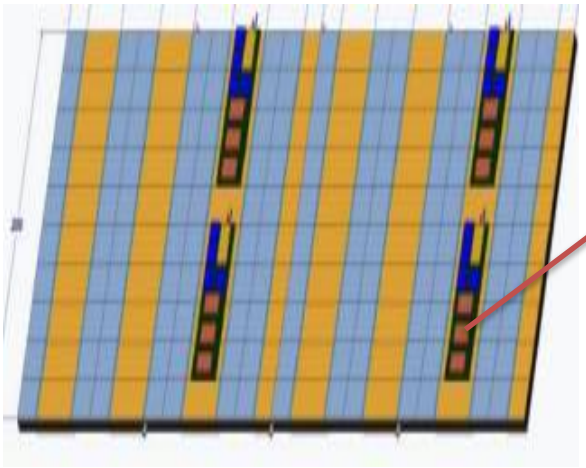


LHCb framework TDR, Feb 2022

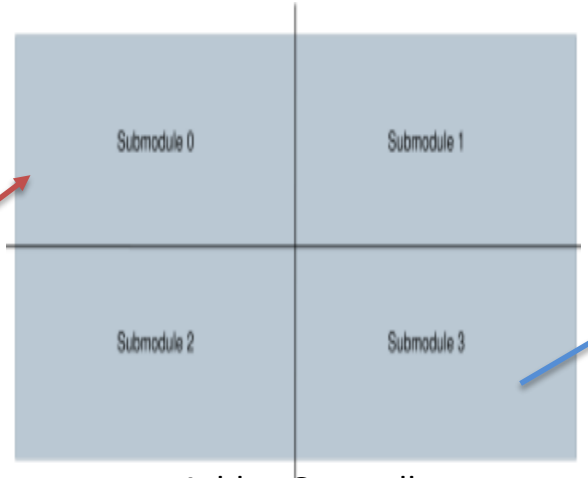
- The proposed design is- flex tape is glued on the carbon plates. Over the flex tape, HV-CMOS sensor is glued.
- Electric connection between flex tape by wire bonding.
- Each readout hybrid- 3lpGBT, 1 control lpGBT, 3 DC/DC converters.

Current Proposal for Mighty Tracker Module

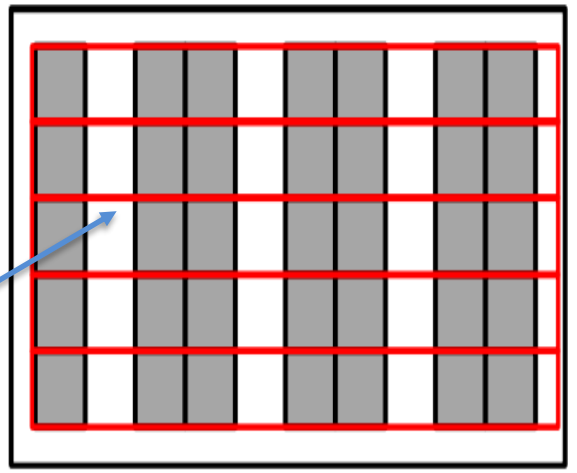
- Each submodule have- 20/35 (short/long) mighty pix devices.
- In the current proposal, there would the **horizontal flex**, consider as horizontal ladder or **horizontal topology**.



Module to sub-module division

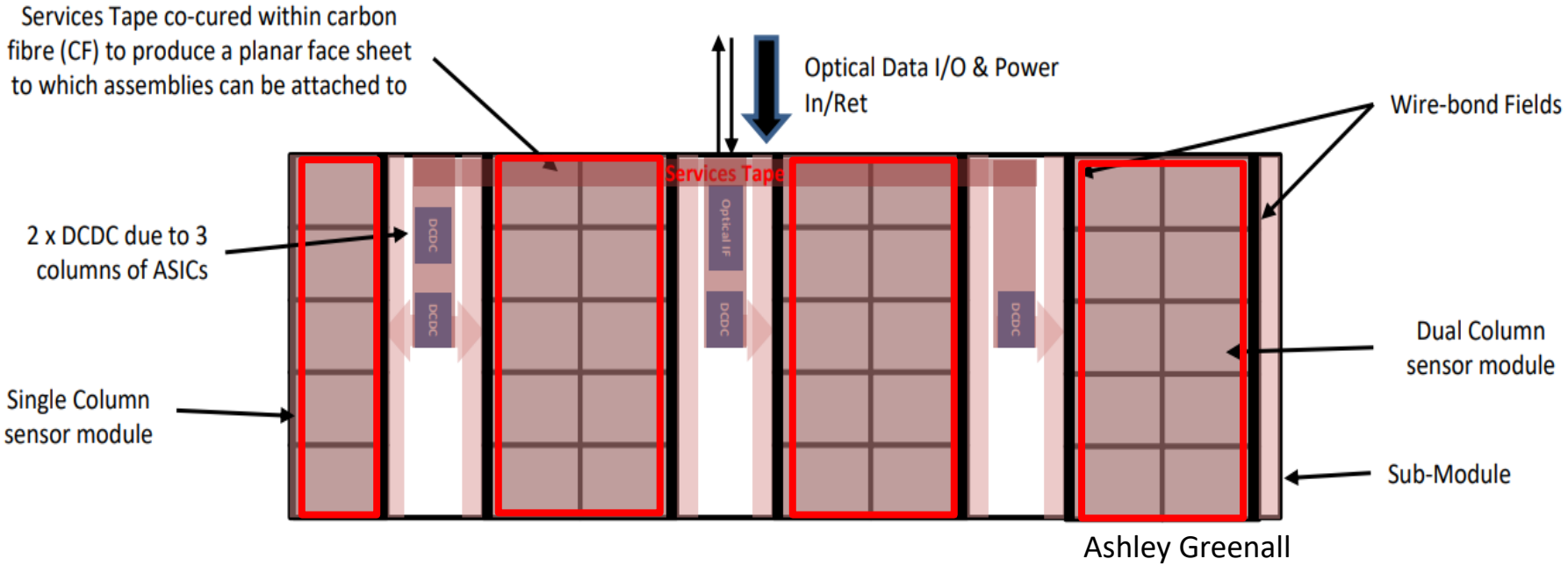


Ashley Greenall



Each of the red horizontal box represents a ladder – Horizontal Flex ladder over a long sub-module

Liverpool's Proposal for Mighty Tracker Module

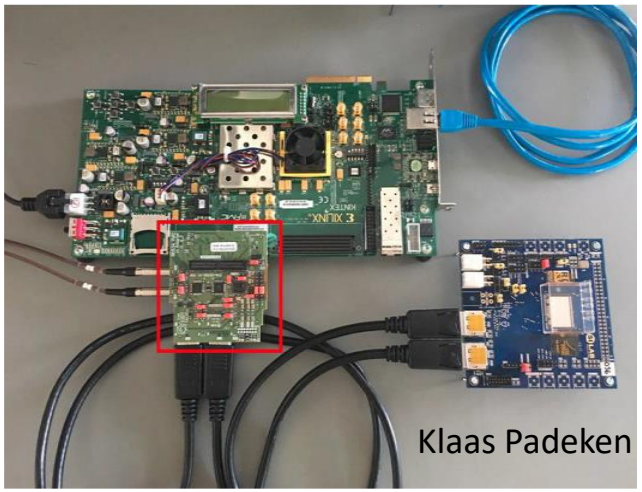


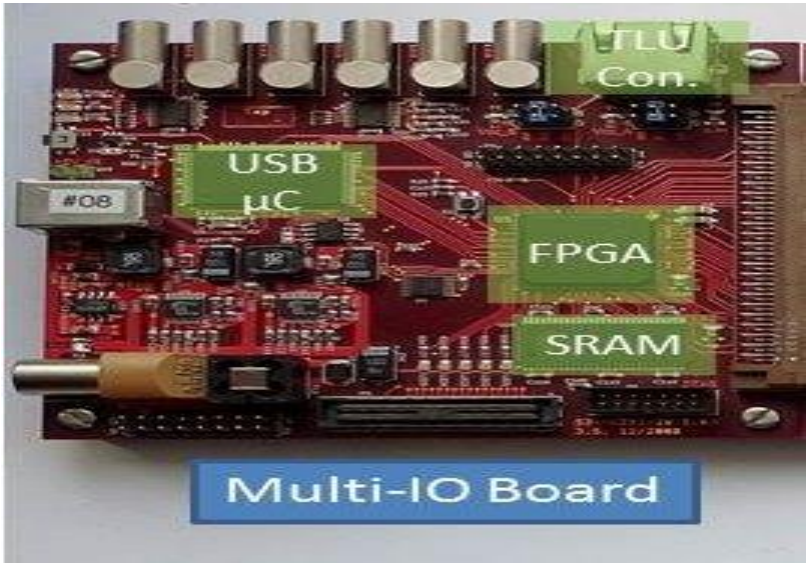
- **Modular Column Topology** is made up of -- .
  - Sensor Module Assembly
  - Services Types
  - DC/DC converter & lpGBT chipset

Measurements

Basil DAQ-

- We would use BASIL DAQ in our lab to test our chips for measurements, (established by University of Bonn)
- Easy for measurement and is LHCb compatible, tested widely.





HARDWARE-

- Mother/system board.
- Chip board where the chips are bonded.

FIRMWARE-

- FPGA firmware modules.
- Programmable based on different HDL's.

SOFTWARE-

- Python is used.
- Cocotb library.

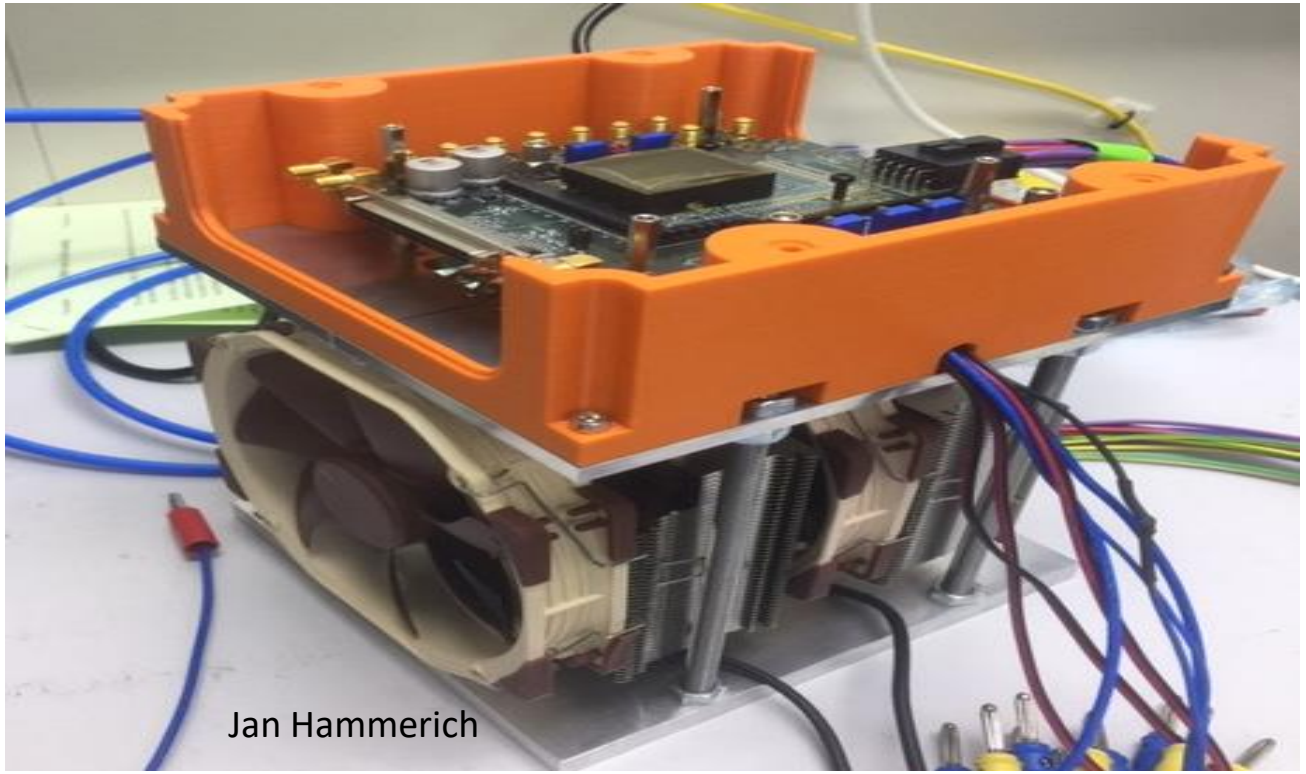
Measurements

- **What do we expect to check through BASIL DAQ-**
  - Electronics Compatibility of the chip
  - Periphery works with electronics LHCb environment or not
  - Chips have full column length, check no loss in signal
  - Effect of radiation on the chip
  - Speed and Robustness

- **Measurements in Lab-**
  - I have recently started working in Lab with the measurements for ATLASPix3.1 irradiated chip.

Measurements

- **Cooling Setup-**

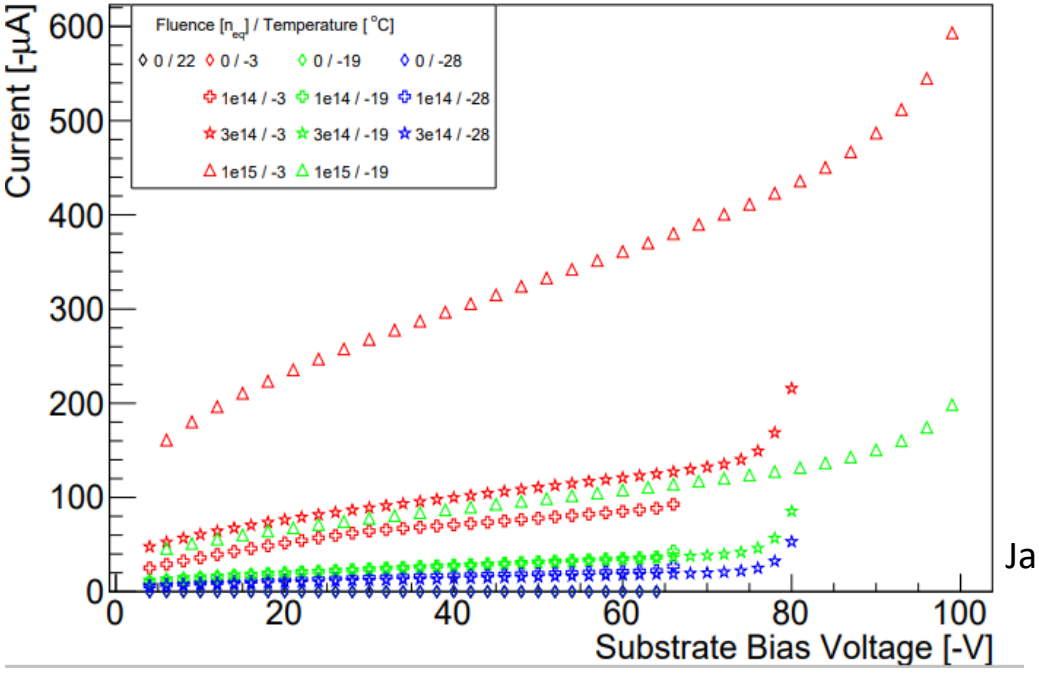


- This setup has been completely build in Liverpool lab. It is a in house developed setup.
- The cooling setup used for ATLASPix3.1 in the lab.

Measurements

Irradiated ATLASPix3.1 -

- Since ATLAS is also an HV-CMOS chip so its results would provide us a good reference for MightyPix chip.
- The study would include the specifications of temperature after high radiations and their time resolutions and power consumptions calculations.



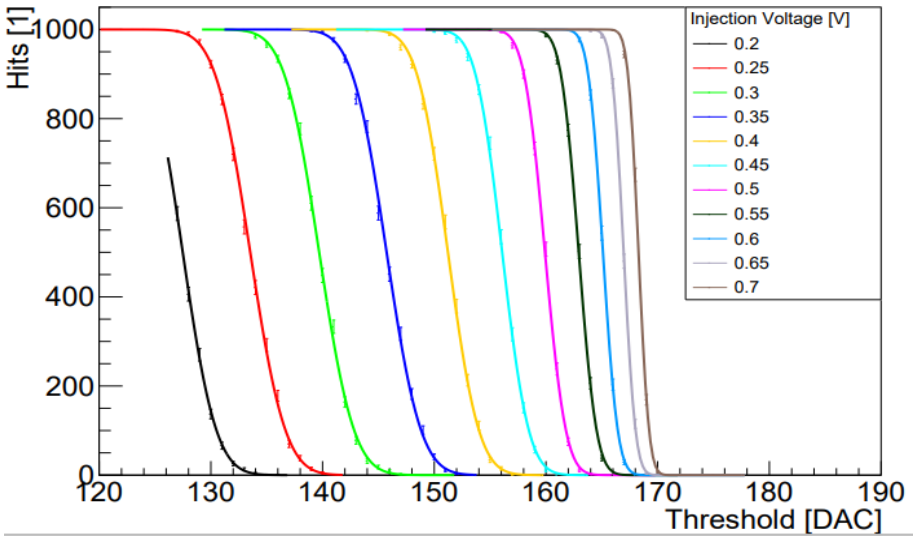
Jan Hammerich for ATLASPix3.1

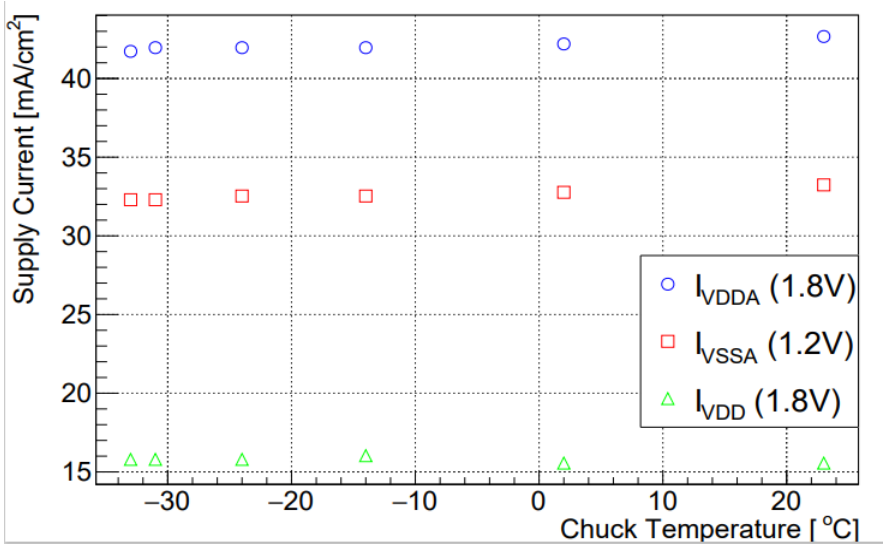
Measurements

Irradiated ATLASPix3.1-

- These information would be helpful to check MightyPix chip in future and will provide us a base for future measurements in lab as well as at testbeam.

- Few results for ATLASPix3.1 are shown below-





Jan Hammerich for ATLASPix3.1

Conclusion

- The **MightyPix 1 design has been submitted** last week to the TSI foundry and is expected to be with us by **November** for the lab measurements.

- The **DESY test-beam** from 5th June to 12th June has been booked for **ATLASPix3.1** irradiated chip. Since ATLAS is also an HV-CMOS chip it results would provide us a good reference for MightyPix in future.

- The **Flex electronics design** for the chip is under discussion and we have weekly meeting with the chip mechanics group.

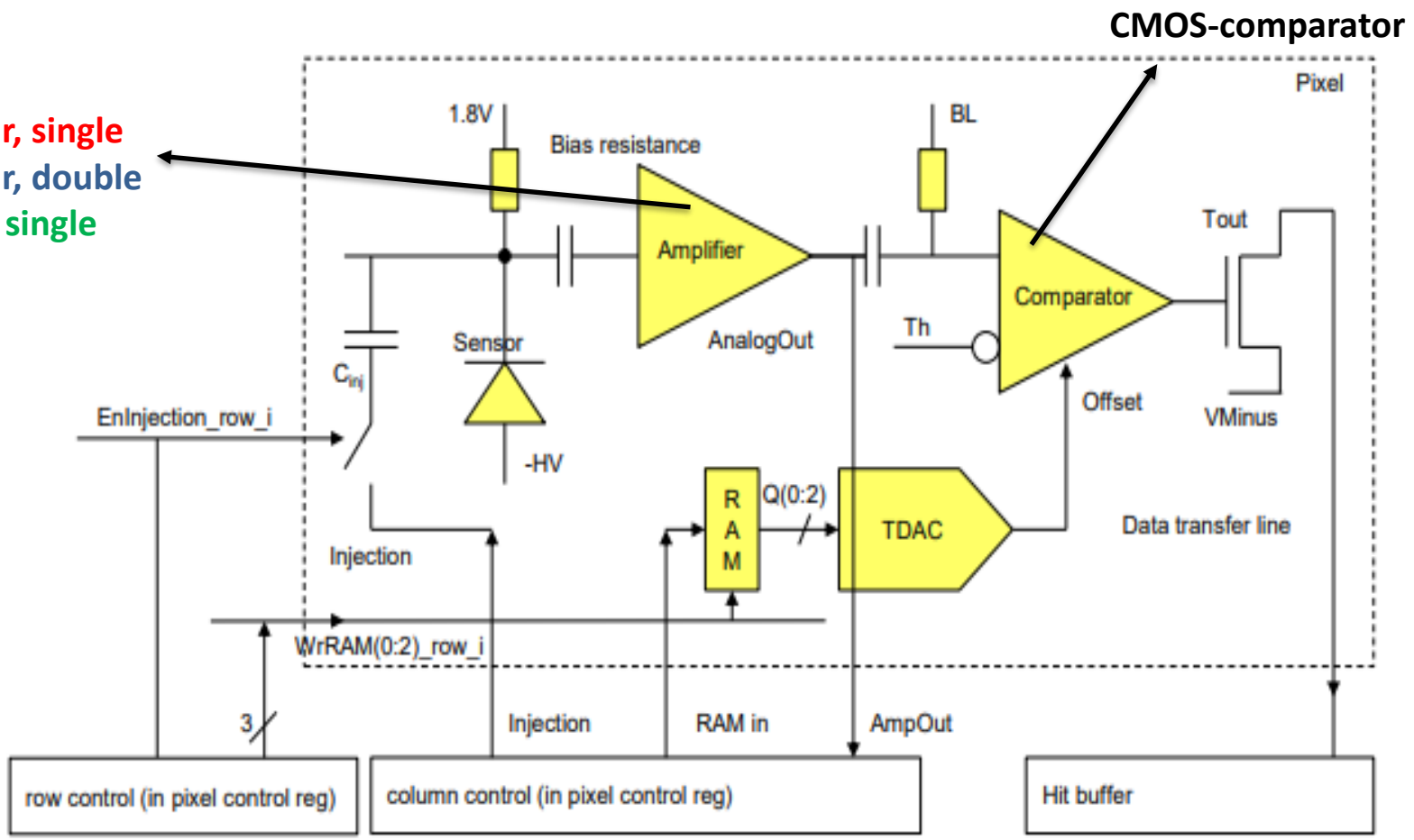
- The simulation results from **FPGA prototyping** of the chip, would help us to gain knowledge for the next iteration of the chip.

Conclusion

Thank you

Circuitry inside each Pixel

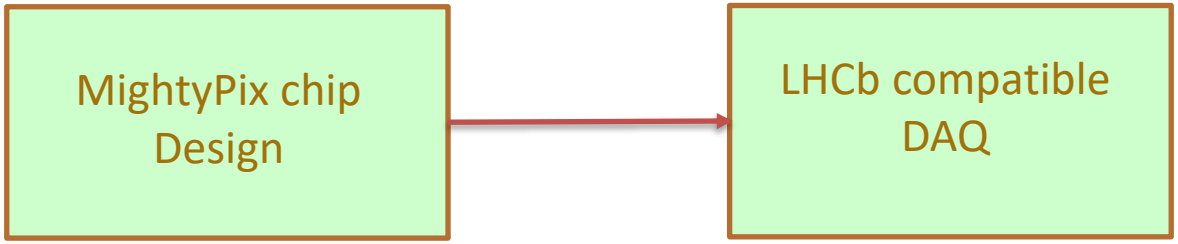
- 8µm, circular, single
- 4µm, circular, double
- 8µm, linear, single



TSI Engineering run v2-KIT

Simulations Structure:-

It's a complex combination of various files of different languages and different tools.



- **Used Programs for-**
  - Test HDL code- Questa Sim
  - Test Design- python
  - Bring two together (cocotb Library)

- **Verilog Testbenches for DUT-**
  - Drive clocks, instantiate HDL modules (e.g. MightyPix)
  - Read in simulated data (e.g. TFC signals, injection data)and feed it into MightyPix

Backup slides

- **Recommended-**
  - BASIL over GECCO
  - GECCO not completely compatible for LHCb readout environment.
  - More efficient and precise validations use BASIL.
  - KIT use GECCO and BASIL in Bonn.
  - Data exact to proof them-
    - Gigabit Ethernet, support (10Gb/s)

Backup slides

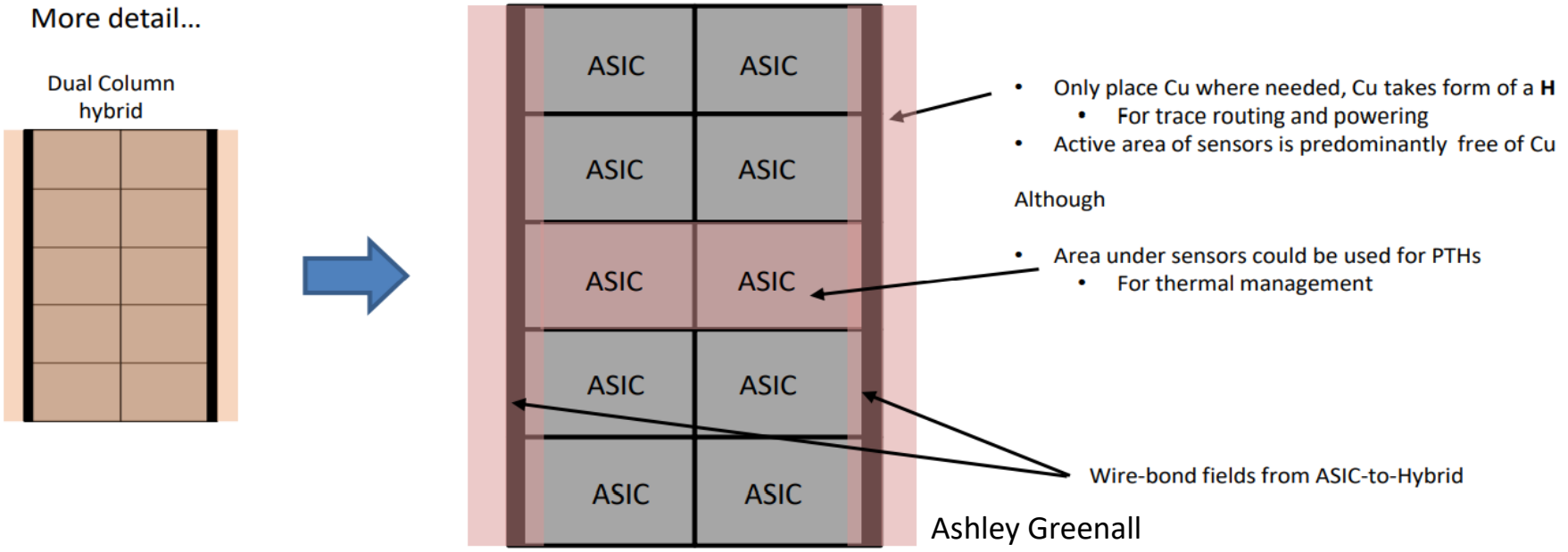
Connection	Purpose	Voltage	Single ASIC Current	Current per column of 5 sensors
VDDD	Digital	1.8V	61mA	305mA
VDDA	Analogue	1.8V	195mA	975mA
VSSA	Analogue	1.2V	140mA	700mA
Total Current			396mA	1980mA

bPOL12V DCDC Converter (4A max load) could power up to 10 MightyPix – provides a hint to powering topology:

n

1 converter per ladder or 1 per double column

Sensor Modular Assembly-



- ASICs are wire bonded to flex to pick up signalling and power.
- H topology of this Cu provides easy thermal management of ASICs.