R&D of HV-CMOS detectors

2021 HEP Annual Meeting, 19-20 May 2022

UNIVERSITY OF LIVERPOOL

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on behalf of the HV-CMOS group

HV-CMOS: Monolithic Pixel Detectors

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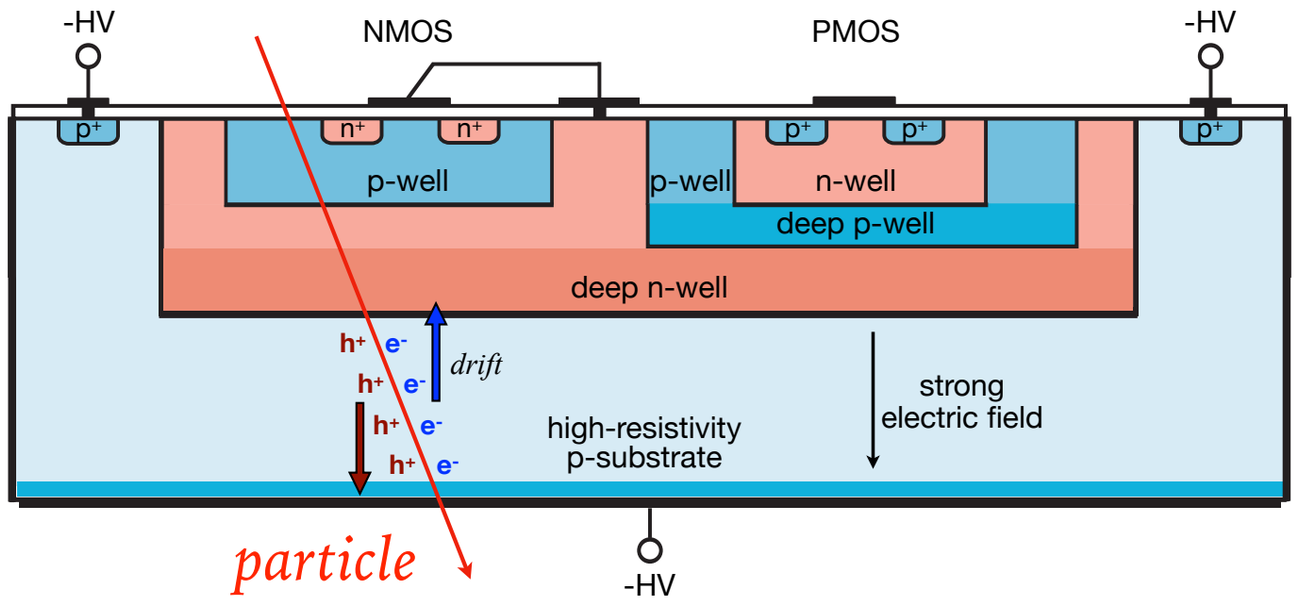
- Monolithic: Sensor and readout electronics in a single silicon wafer.
  - ➤ Single layer structure: **low material thickness** (50 μm);
  - ➤ No bump-bonding: **Small pixel size** ($< 50\ \mu\text{m} \times 50\ \mu\text{m}$); **reduced production cost** (~ £100k/m^2);
  - ➤ High bias voltage: **fast charge collection** by drift (~ 200 ps) and **high radiation tolerance** (5×10^{15} 1 MeV n_{eq}/cm^2).



- The Mu3e experiment has chosen HV-CMOS pixel detectors and many others are considering them: LHCb, proton EDM, PANDA. And applications fields other than HEP experiments.

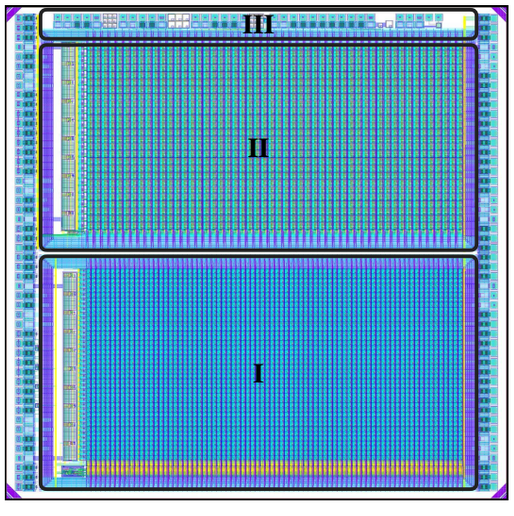
Our Collaborations

- **CERN-RD50** collaboration focuses on developing radiation-tolerant detectors.
- Liverpool has the leadership of its **CMOS Working Group**, we do:
  - ASIC design
  - TCAD simulations
  - DAQ development
  - Chip performance evaluation
- Currently involves 17 institutes across the world:

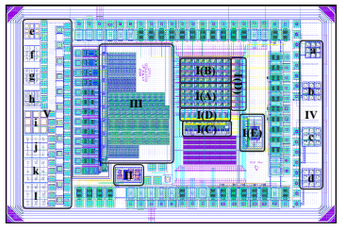
Liverpool HV-CMOS development

- Development goals:
  - ➤ High radiation tolerance (low leakage and high breakdown)
  - ➤ excellent time resolution and pixel granularity

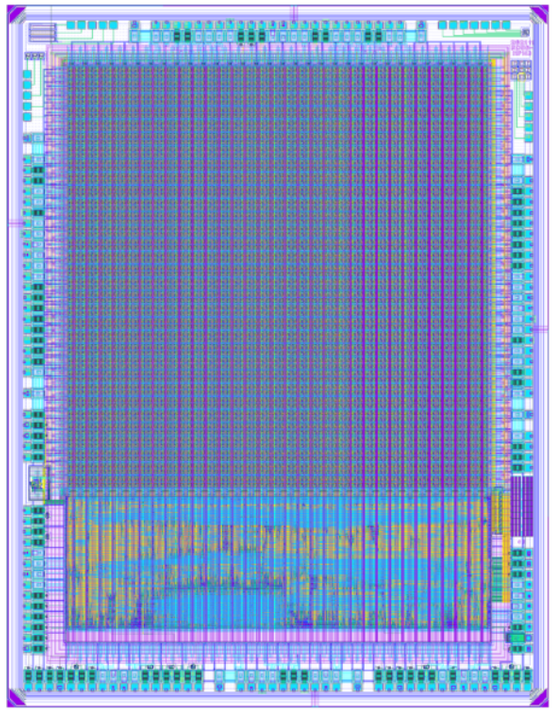
RD50-MPW1
received in Apr. 2018



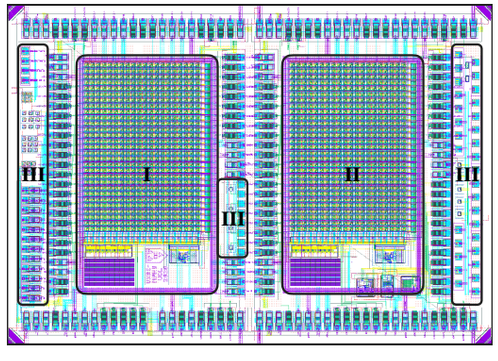
RD50-MPW2
received in Feb. 2020



RD50-MPW3
submitted in Dec. 2021



UKRI-MPW0
received in Jun. 2021



- **RD50-MPW1**: test the LF150 process, low V_{BD} (55 V) and high I_{Leak} (~ μA).
- **RD50-MPW2**: high V_{BD} (130 V), low I_{Leak} (~ nA) and fast analog pixel.
- **RD50-MPW3**: implements large pixel matrices with advanced digital readout.
- **UKRI-MPW0**: first backside-only biased, high V_{BD} (> 600 V).

Beam test of RD50-MPW2

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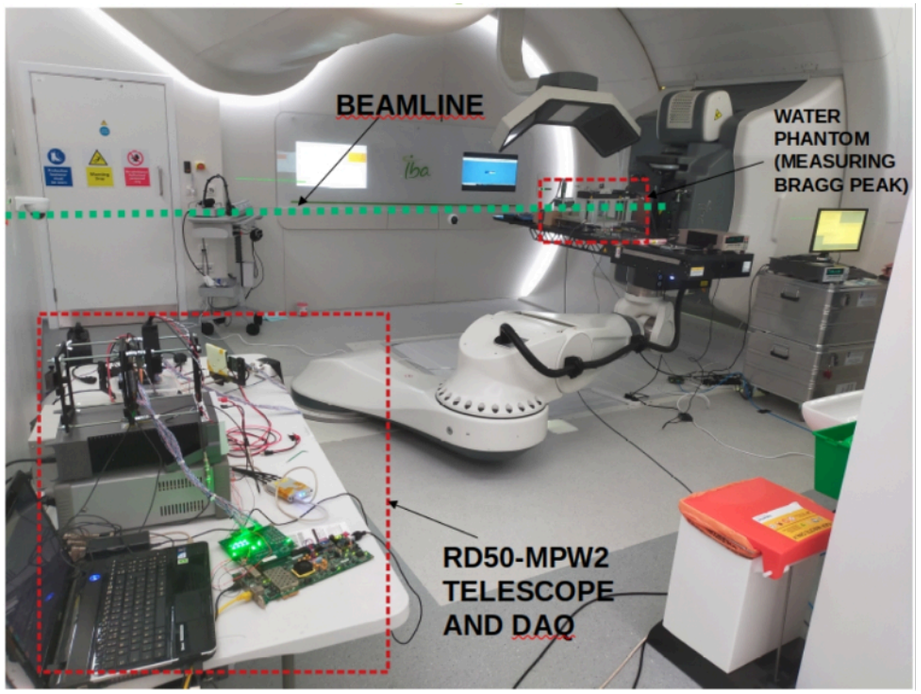
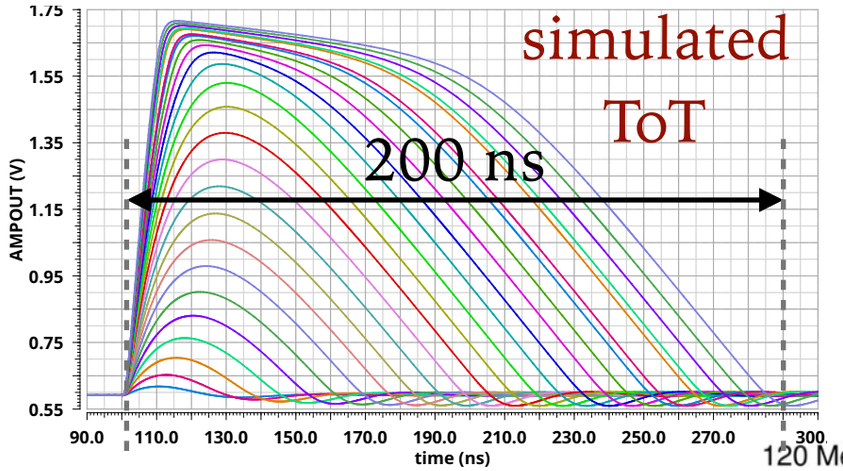
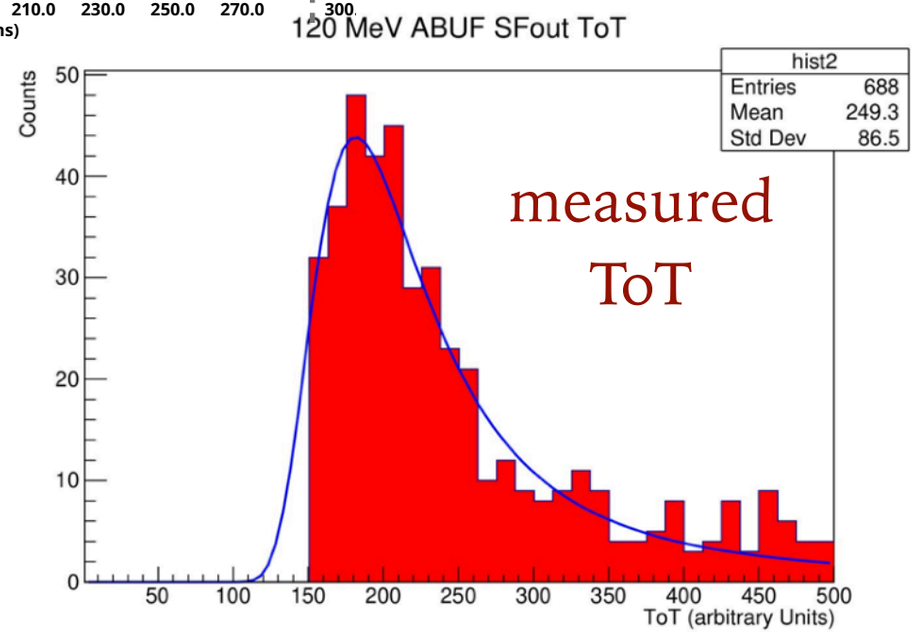
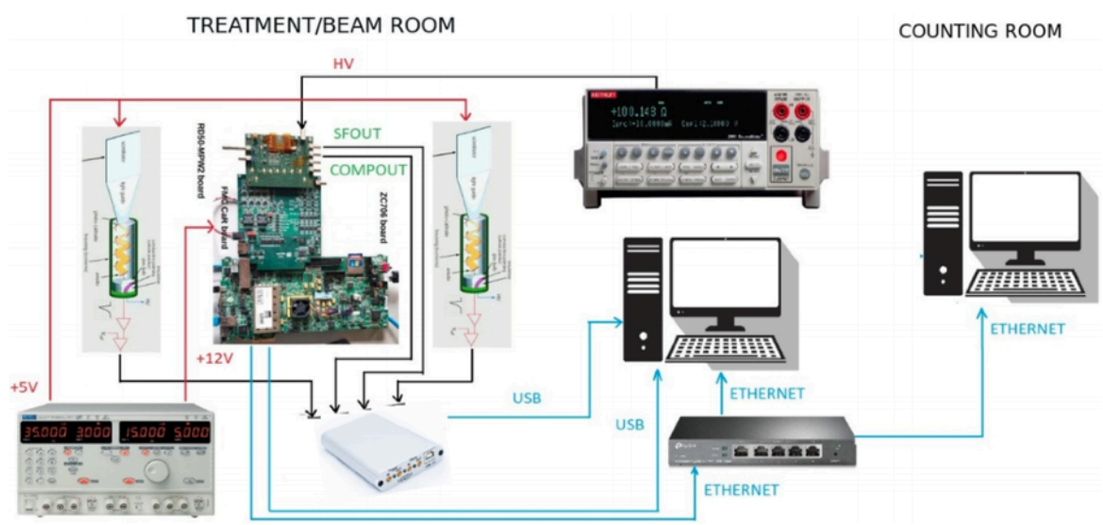
- First beam test by Liverpool HV-CMOS group.
- Characterise RD50-MPW2 at Rutherford Cancer Centre in Northumberland in May 2021.
- Protons delivered in bunches with a 1 kHz rate
  - ➤ Beam energy: 70 -229 MeV
- ToT measurement is in agreement with simulation.





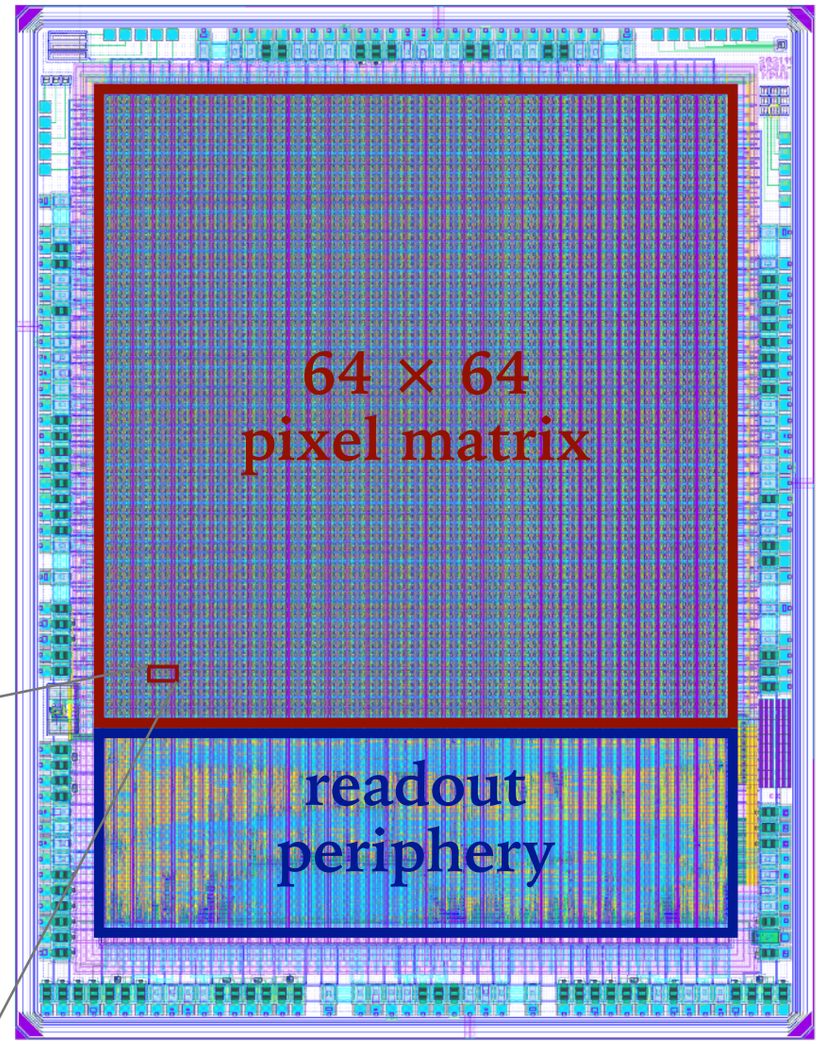


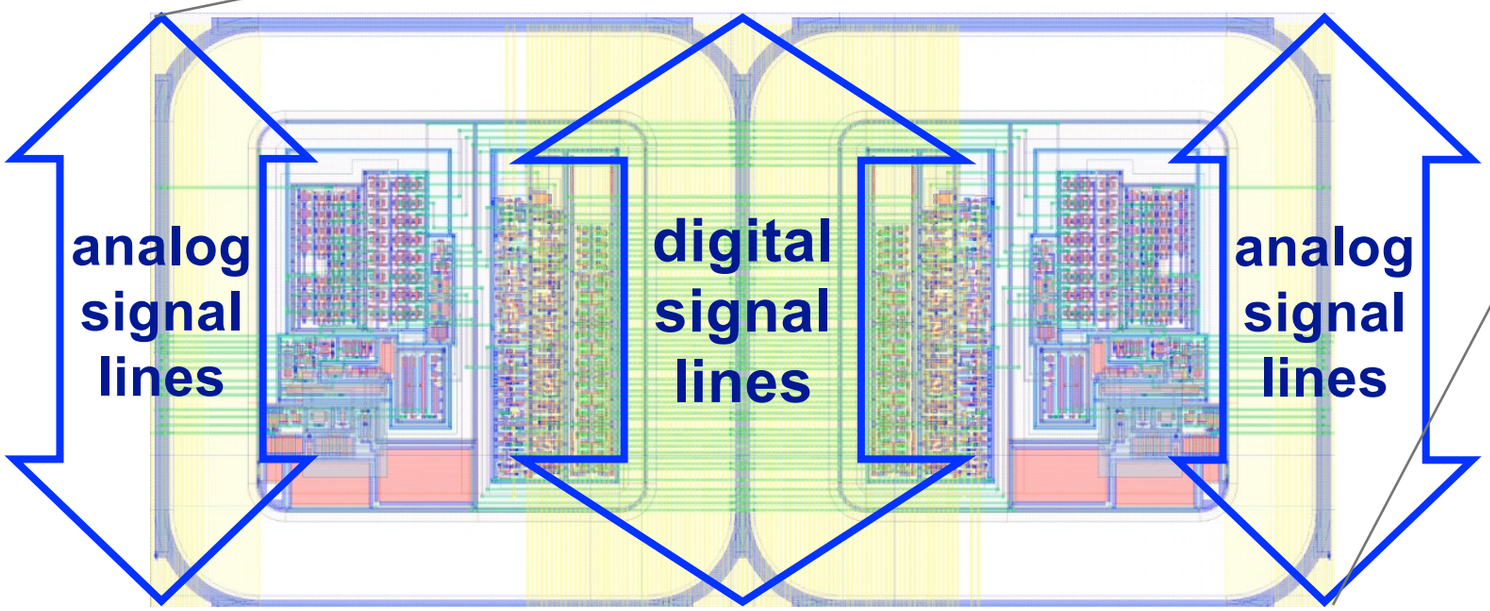


Beam test DAQ setup

Design of RD50-MPW3

- **RD50-MPW3** submitted in **Dec. 2021**, delivery expected in **Jul. 2022**.
- Composed of a 64 × 64 pixel matrix (by Liverpool) and a digital readout periphery (by HEPHY).
- Chip submission is lead by Liverpool.
- New features in RD50-MPW3 include:
  - ➤ double-column architecture;
  - ➤ advanced peripheral readout for high-rate data transmission.



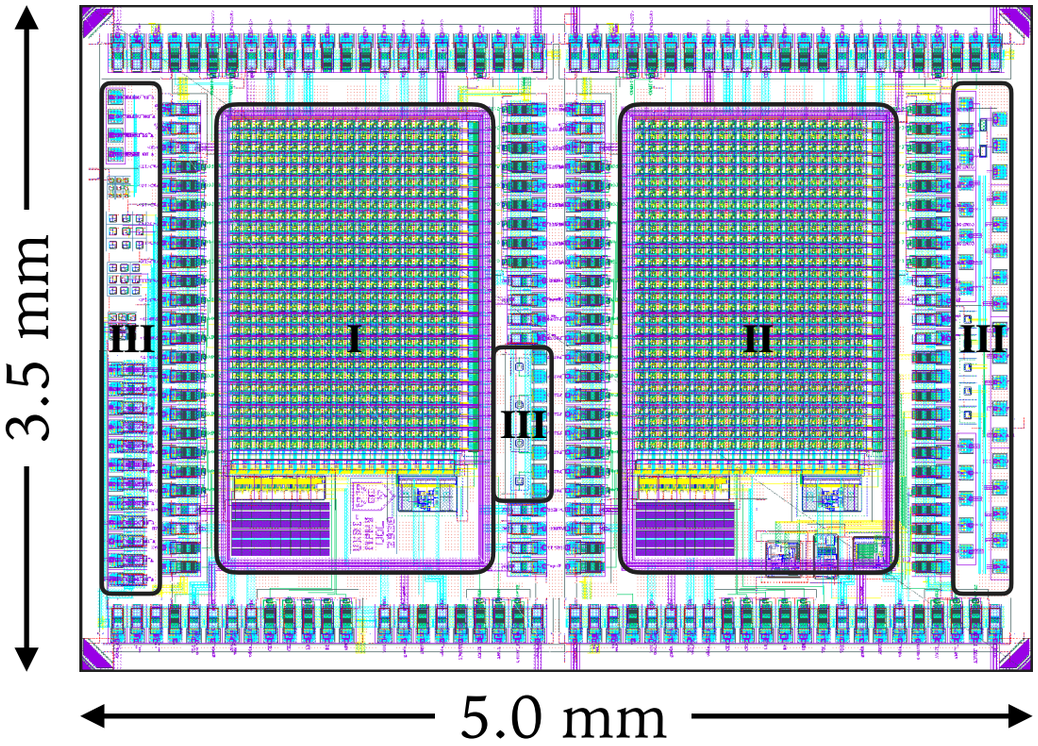


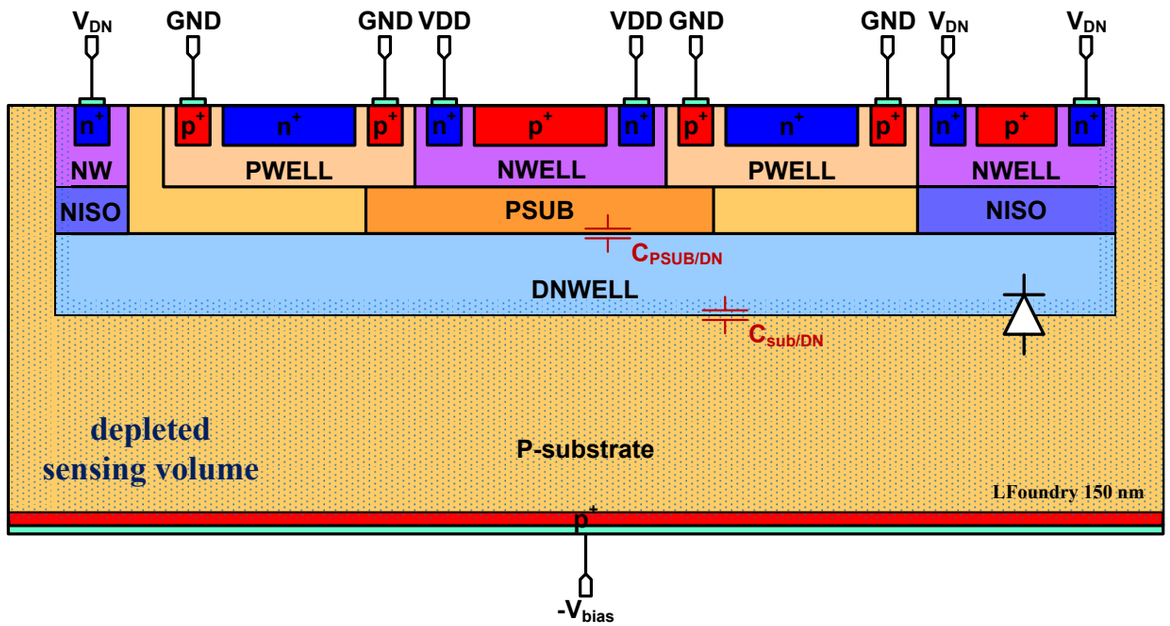
to save area and avoid crosstalk:

- ➤ Digital lines are shared within double column;
- ➤ Analog lines are shared by adjacent double columns.

UKRI-MPW0 Overview

- UKRI-MPW0: a Liverpool internal project.
- Design by Liverpool during the 2020 lockdown.
- First backside-only biased HV-CMOS for high breakdown -> better radiation tolerance.
- Two 20 × 29 pixel matrices (60 μm × 60 μm):
  I. Linear transistors
  II. Enclosed-Layout transistors (ELT)
- III. Test structures for I-V and Edge-TCT measurements, and characterise ELTs.
- Bandgap references and shunt regulator
- Two backside processing methods used:
  1. Ion Implantation (BLII) + Rapid Thermal Annealing (RTA)
  2. Plasma-Immersion Ion Implantation (PIII) + UV laser annealing

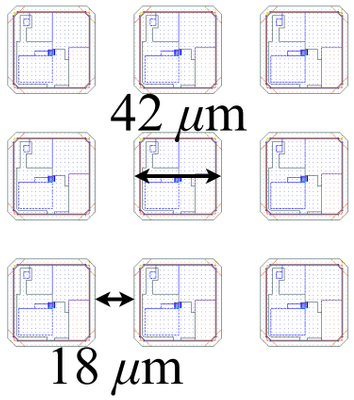


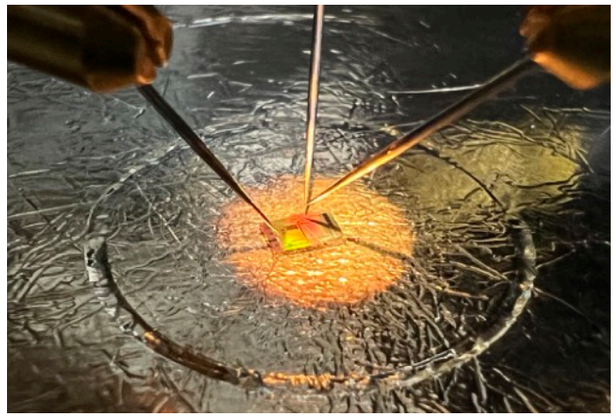


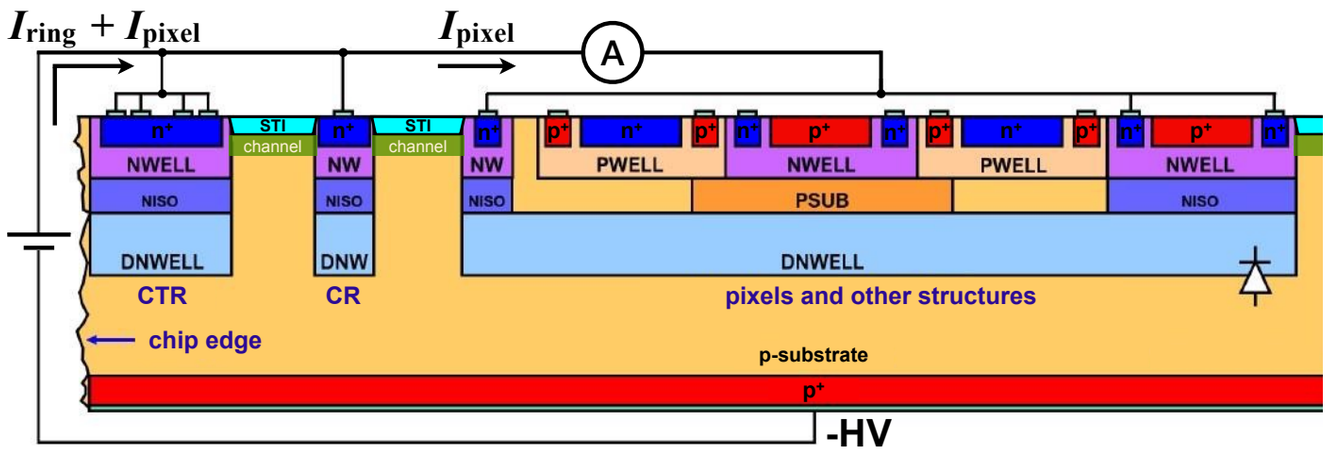
Backside-only high-voltage biasing

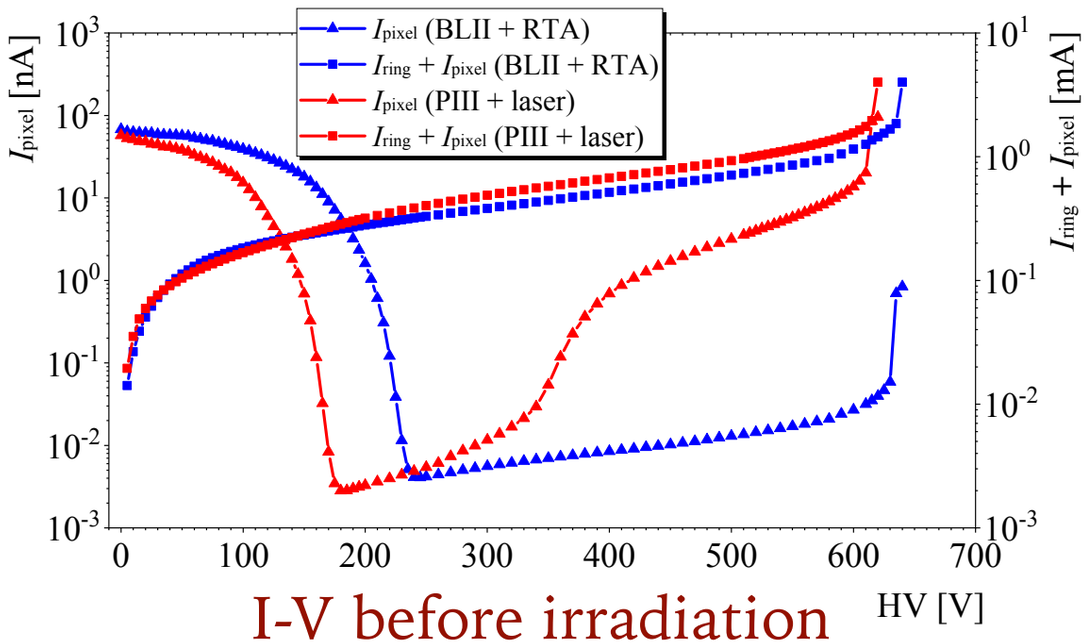
UKRI-MPW0 Initial Measurements: I-V

- I-V measurements on 3 × 3 pixel matrix.
- V_{BD} > 600 V, significant improvement over the state of the art.
- Pixel leakage current I_{pixel} is low, the unusual 'U' shape is due to the parasitic channel between ring and pixel.
- Rings current is high, since they collect most leakage currents caused by edge defects.
- V_{BD} still high after neutron irradiation.

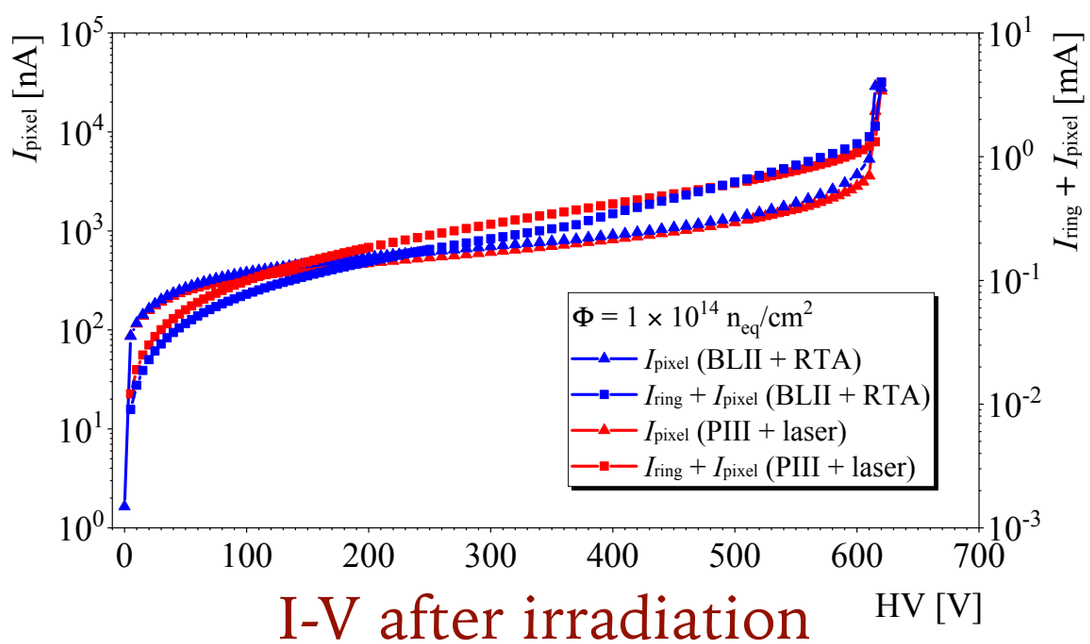








I-V before irradiation



I-V after irradiation

Edge-TCT measurement: Setup

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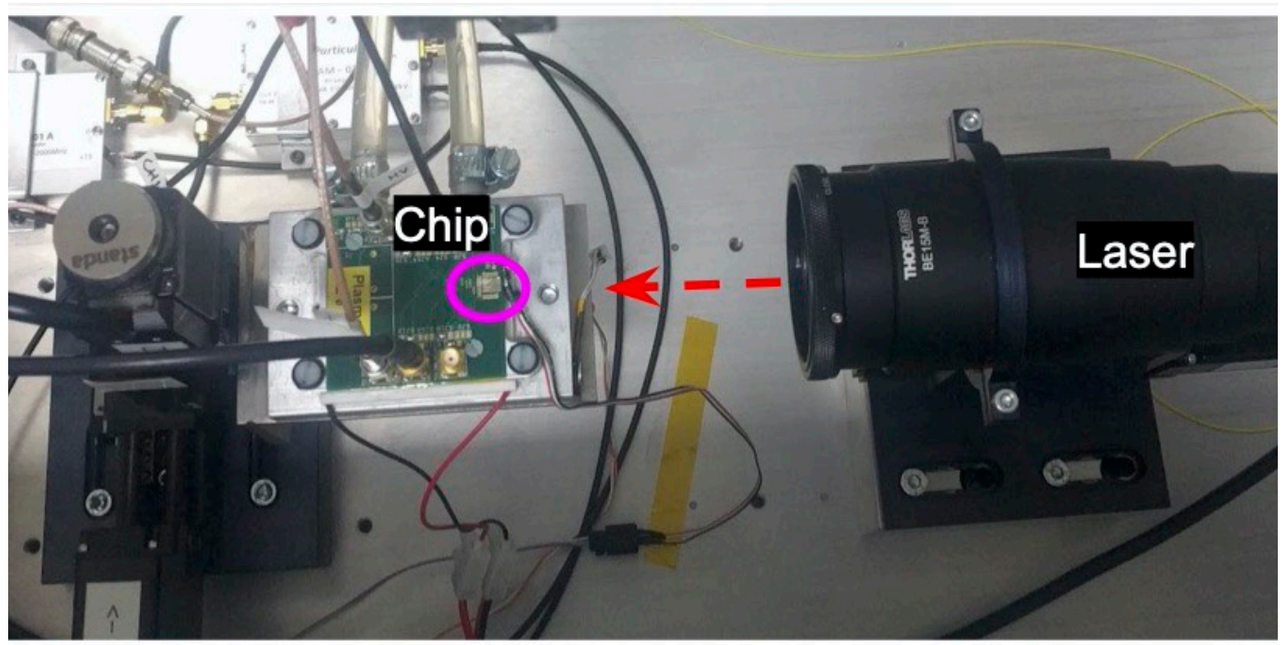
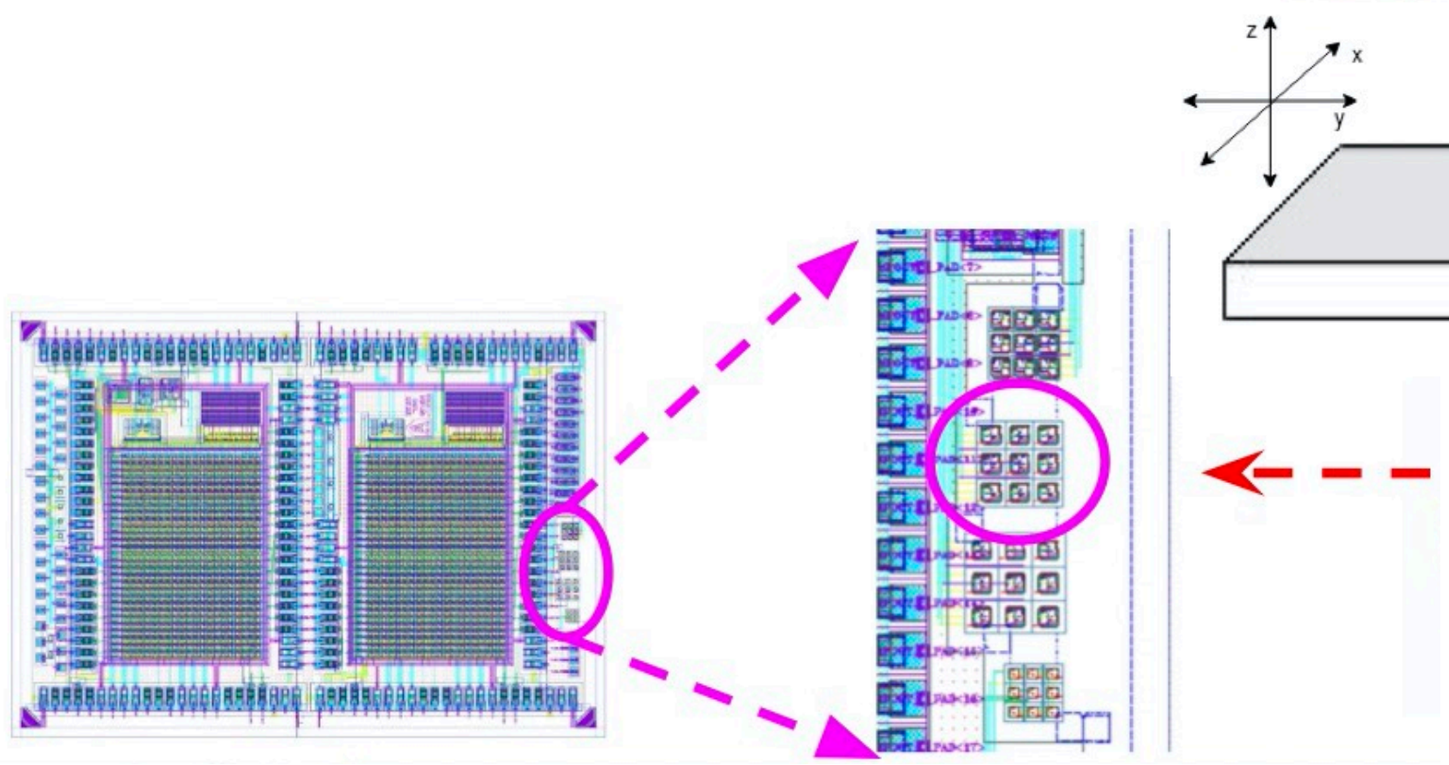
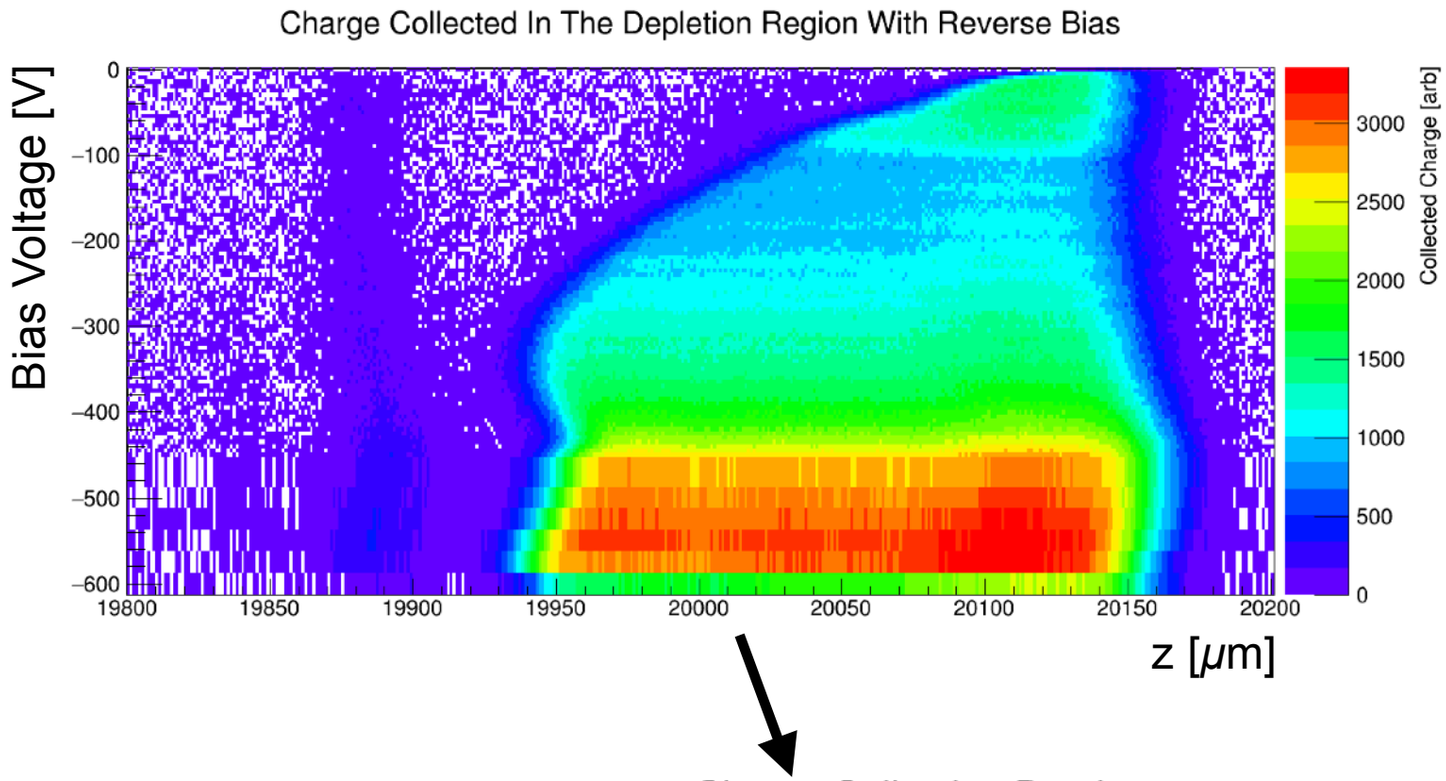
- Edge-Transient Current Technique: focus IR laser inside the chip to generate free charges.
- Measure generated charges to study depletion depths (before and after irradiation).
- focus on test structures on chip edge.

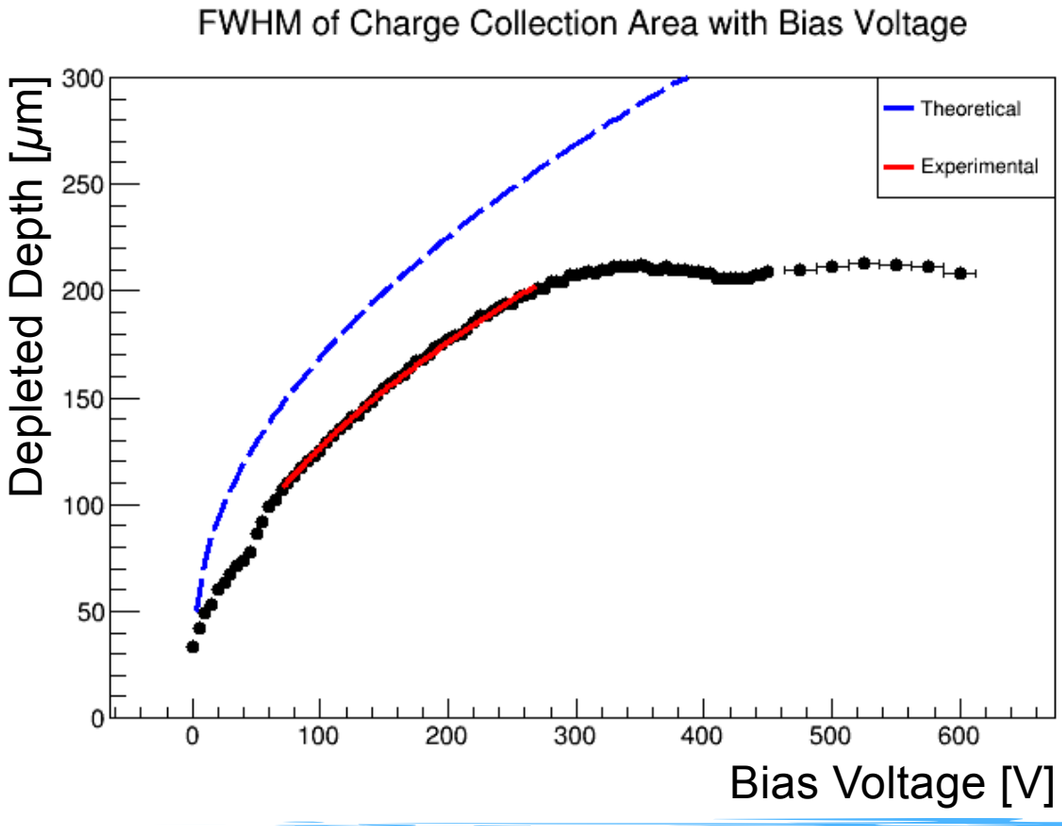


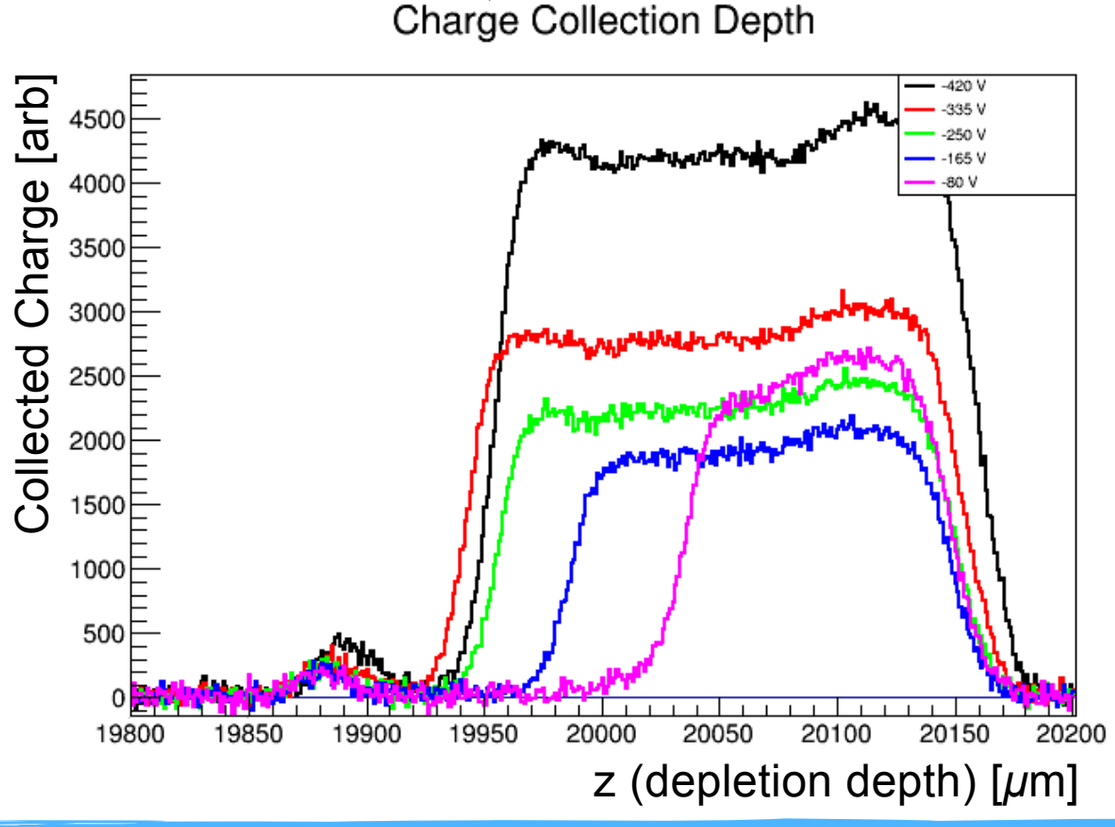


Edge-TCT measurement: Depletion Depth

- Measure depletion depth for different bias voltages.
- Chip fully depletes at the bias voltage around 350 V.
- Full depletion depth is 200 μm.
- Chip was thinned to 280 μm. Investigating the difference.

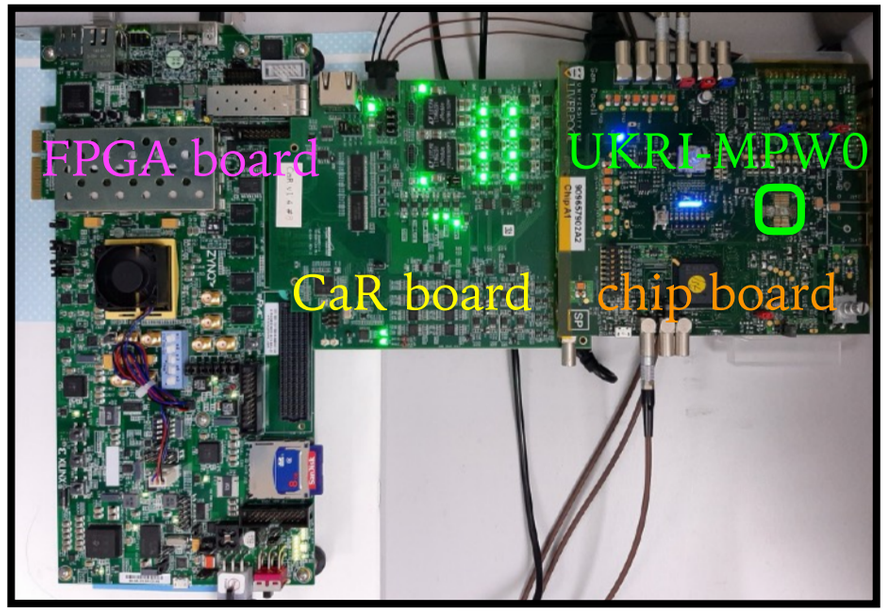




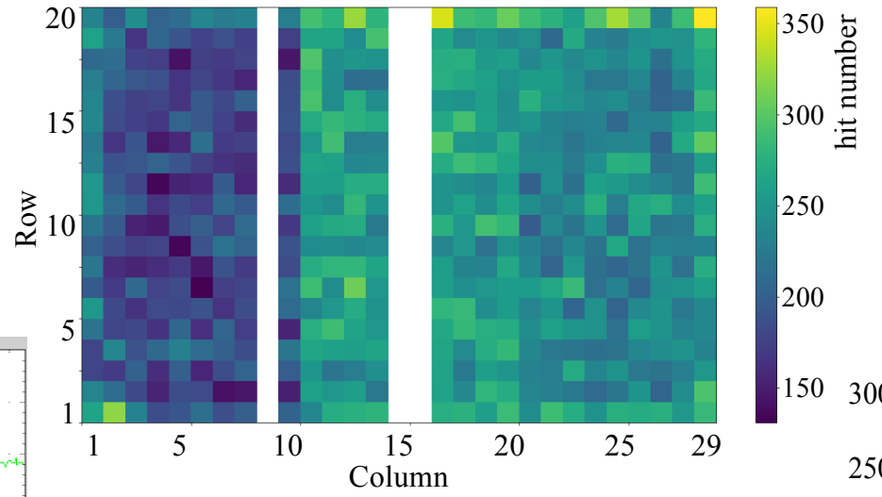


Pixel Matrix Measurements

- Measurements of the pixel matrices are going on.
- Each matrix contains 3 pixel flavours:
  1. Continuous-reset pixel (column 1-10);
  2. Switched-reset pixel (column 11-20);
  3. Modulated-reset pixel (column 21-29).
- Pixel flavours 1. and 2. have been implemented in a previous prototype (RD50-MPW2).

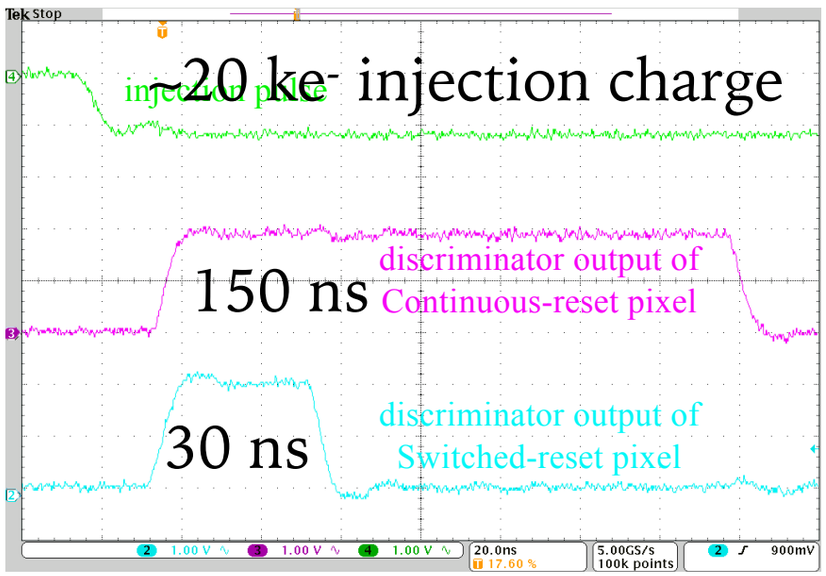


DAQ for pixel matrices

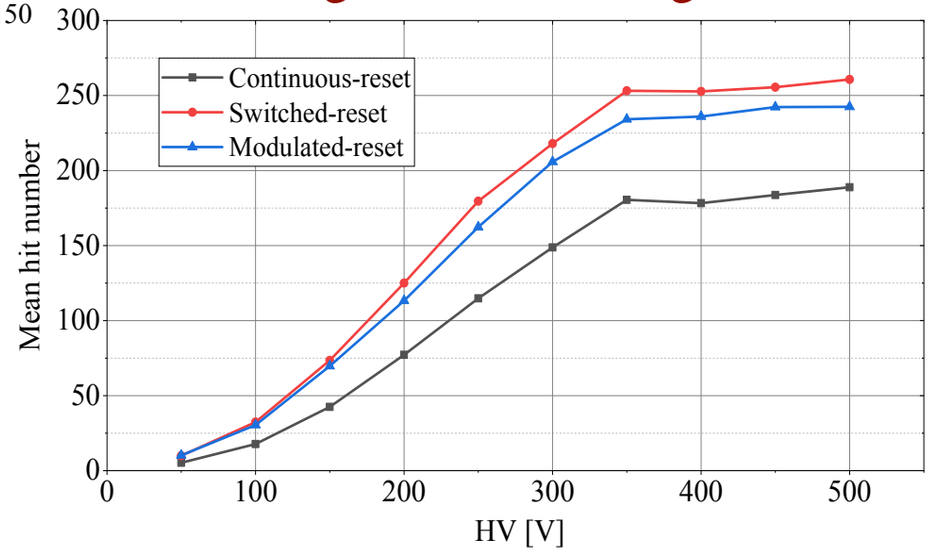


Hit map with a ^{90}Sr source (chip biased to -500 V)

Pixel responses to charge injection

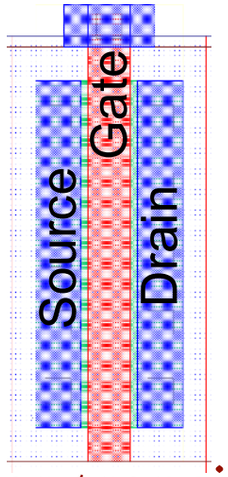


Mean hit number at different high bias voltages

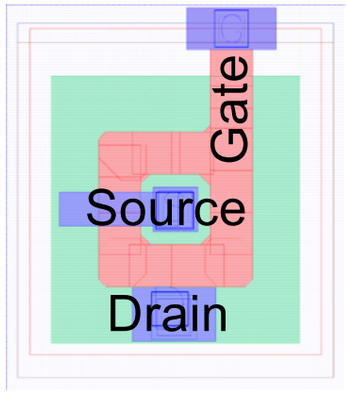


Measurement of ELT and Bandgap

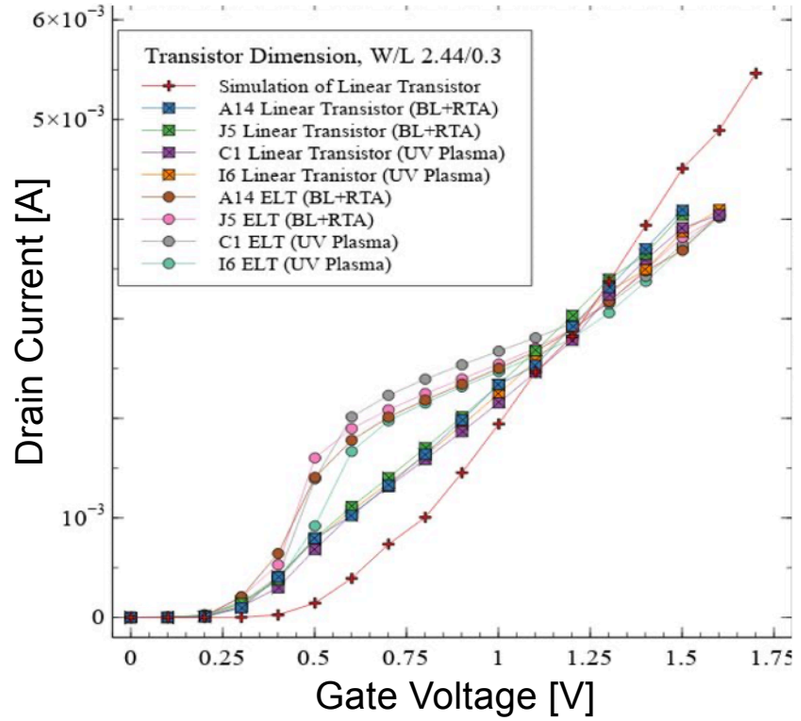
- Enclose-layout transistors are more tolerant to ionising-irradiation than traditional linear transistors.



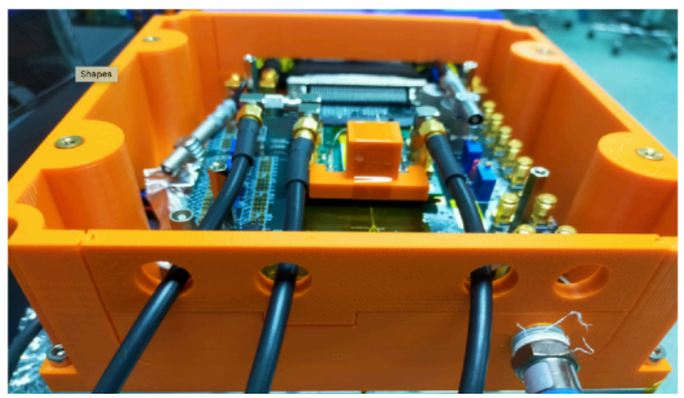
Linear transistor

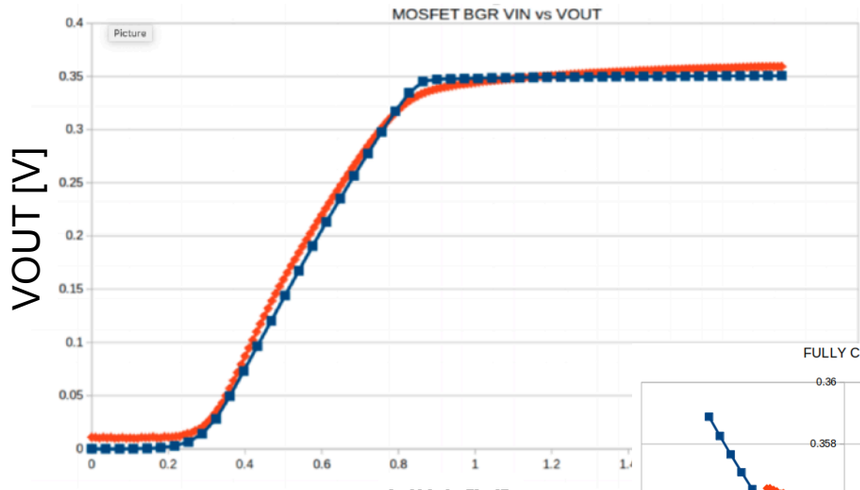


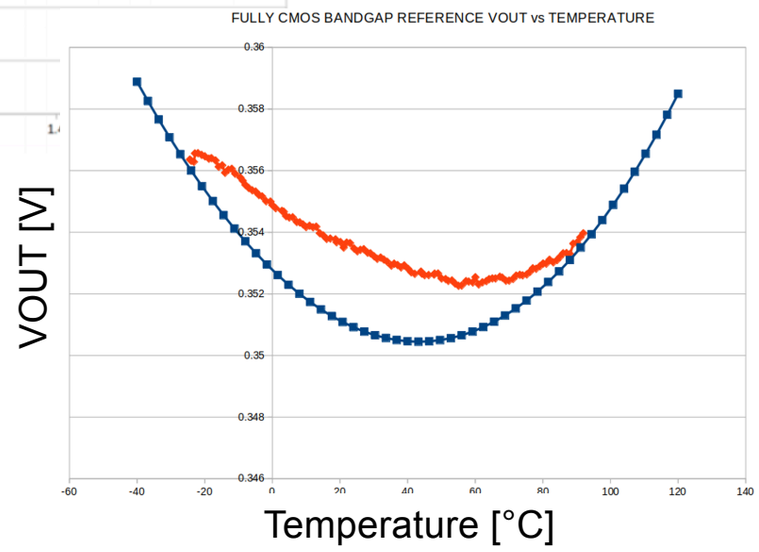
Enclosed-layout transistor



- Bandgap output voltages are measured with different input voltages and temperature (-25°C to 90°C).
- The cooling setup that was developed for the Mighty Tracker chips is used.





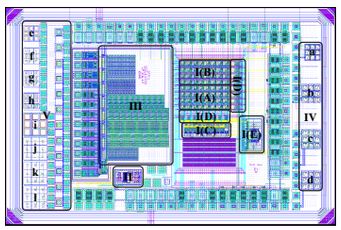


Summary and Next step

- First beam test on RD50-MPW2.
- UKRI-MPW0 has unprecedented high breakdown voltage (> 600 V).
- More measurements are going on, beam test at CERN is planned.
- RD50-MPW3 has been designed and will be delivered and tested later this year.
- Planning to design UKRI-MPW1 to fix parasitic channels and high leakage current.

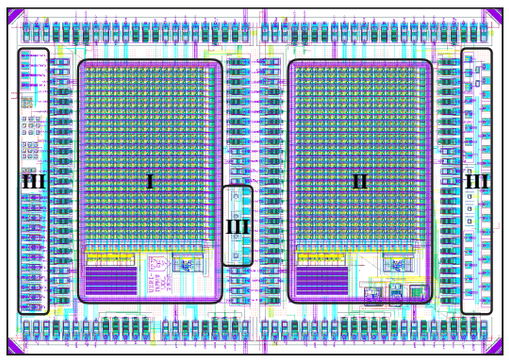
RD50-MPW2

successful beam test



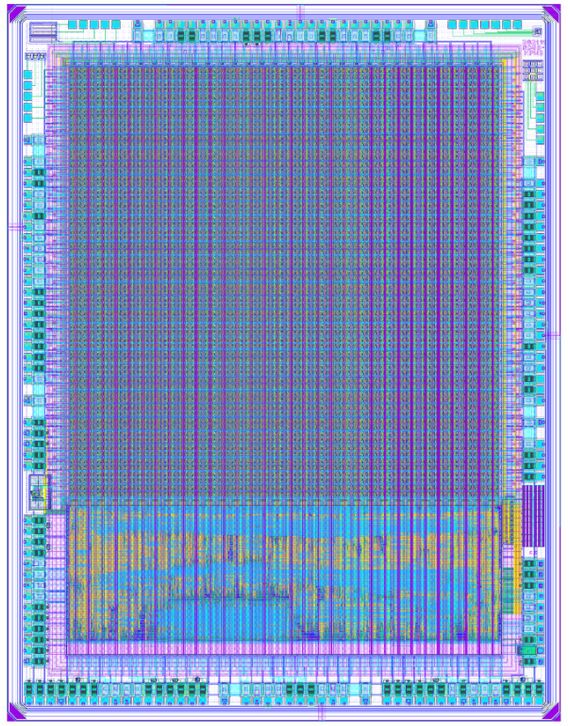
UKRI-MPW0

measurements are going on



RD50-MPW3

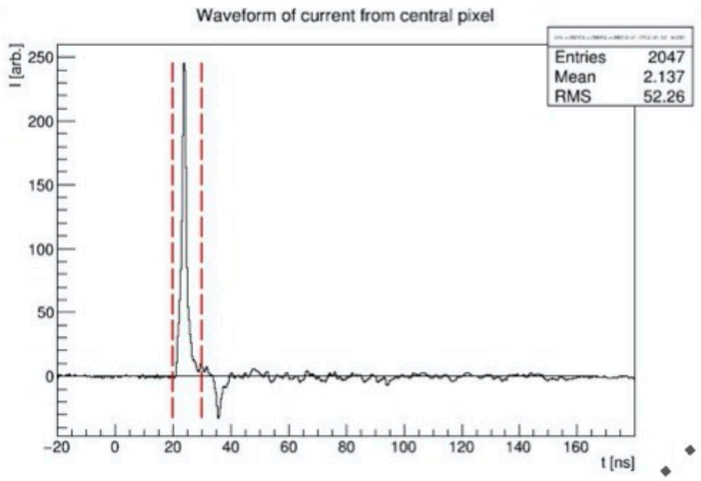
to be delivered in Jul. 2022

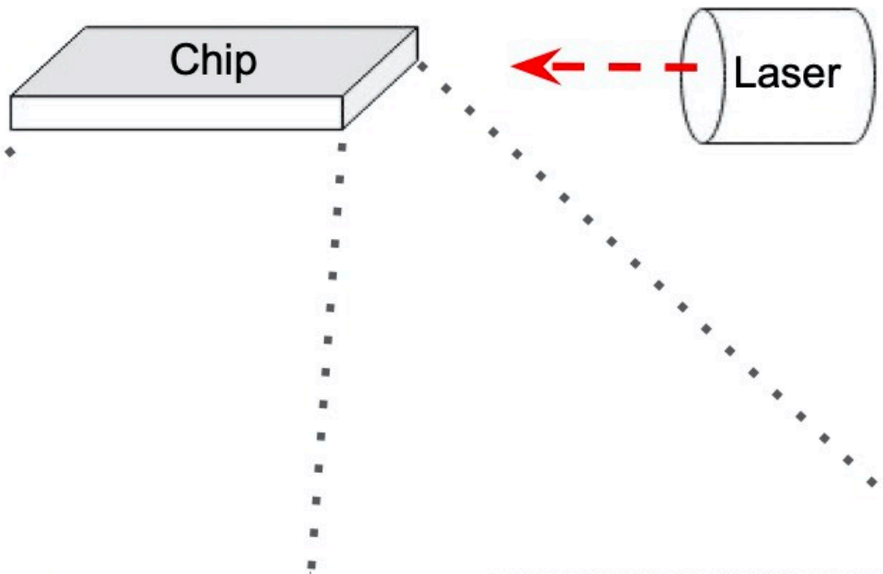


Edge-TCT measurement (backup)

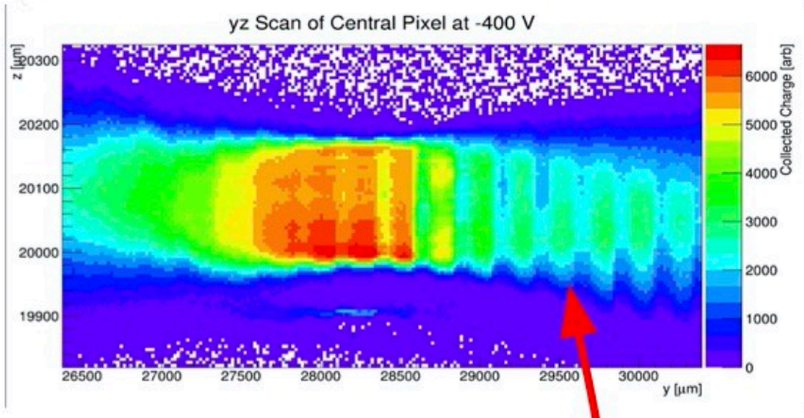
Scan Procedure

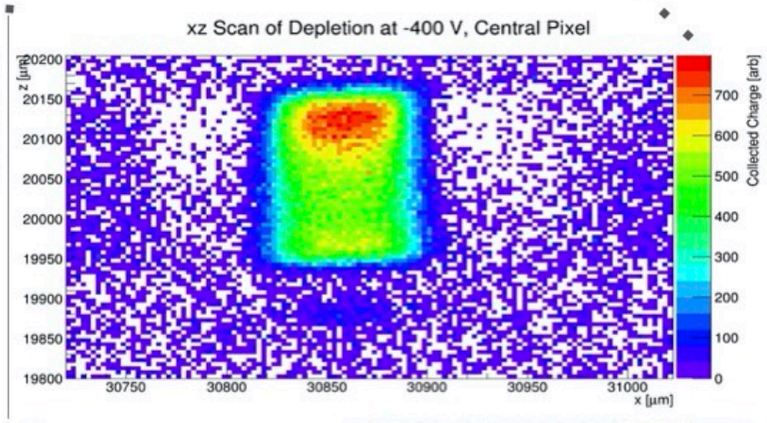
- Laser induces current at beam wait in Silicon
- Waveform of current recorded and 10 ns window around peak integrated
- Chip moved incrementally moved in 3 dimensions charge collection recorded and mapped
- Used to find optimal x and y points in central pixel for depletion depth measurement





Charge collection profiles in the yz and xz planes





Variation in collected charge is from misalignment of the chip