

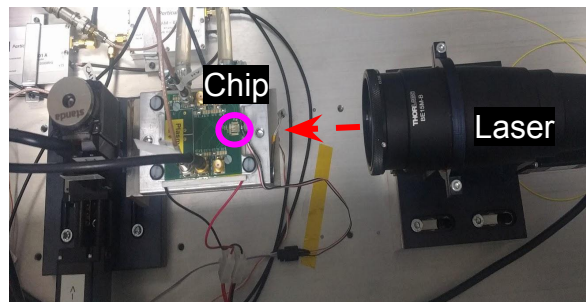
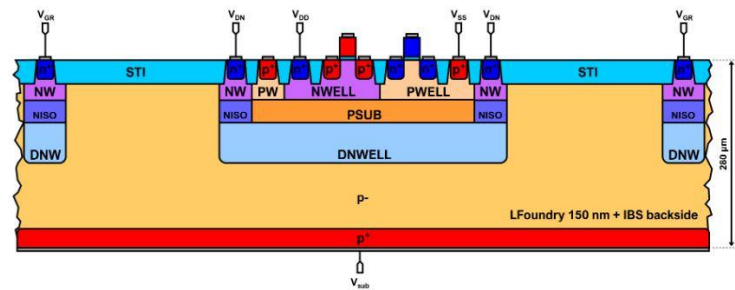
# Characterisation and implementation of HV-CMOS for high rate and high radiation environments:

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- TCAD simulations and experimental measurements of HV-CMOS chips
- Goal to increase radiation tolerance by high biasing voltages
- Currently performing edge Transient Current Technique (eTCT) characterise depletion region and substrate at varying irradiated fluences observing changes in resistivity
- First fully backside biased pixel to reach > 600 V breakdown
- Outlook: continue measurements and start TCAD

Merry Christmas?



Charge Collected In The Depletion Region With Reverse Bias

